Capacitance and IV measurement for HV-CMOS CHESS1 chip

Vitaliy Fadeyev, Zach Galloway , Herve Grabas
Alexander Grillo , Zhijun Liang , Abe Selden

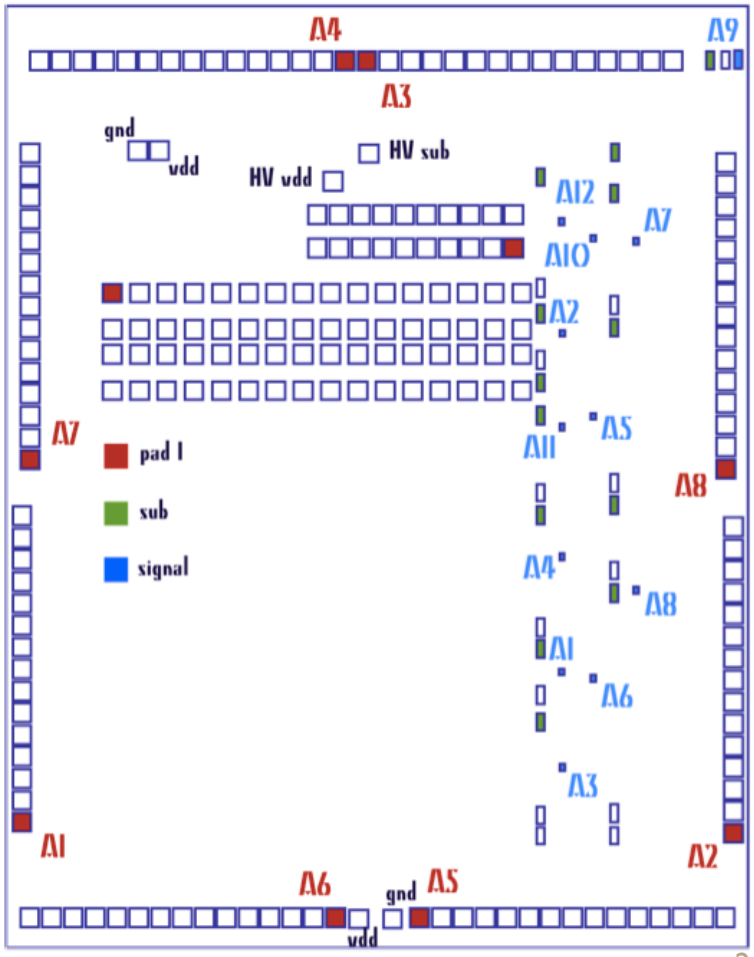
University of California, Santa Cruz

Introduction

- AMS CHESS1 HV-CMOS chip is available for testing
- Preliminary I-V and capacitance results :
  - I-V measurement
  - C-V Measurement

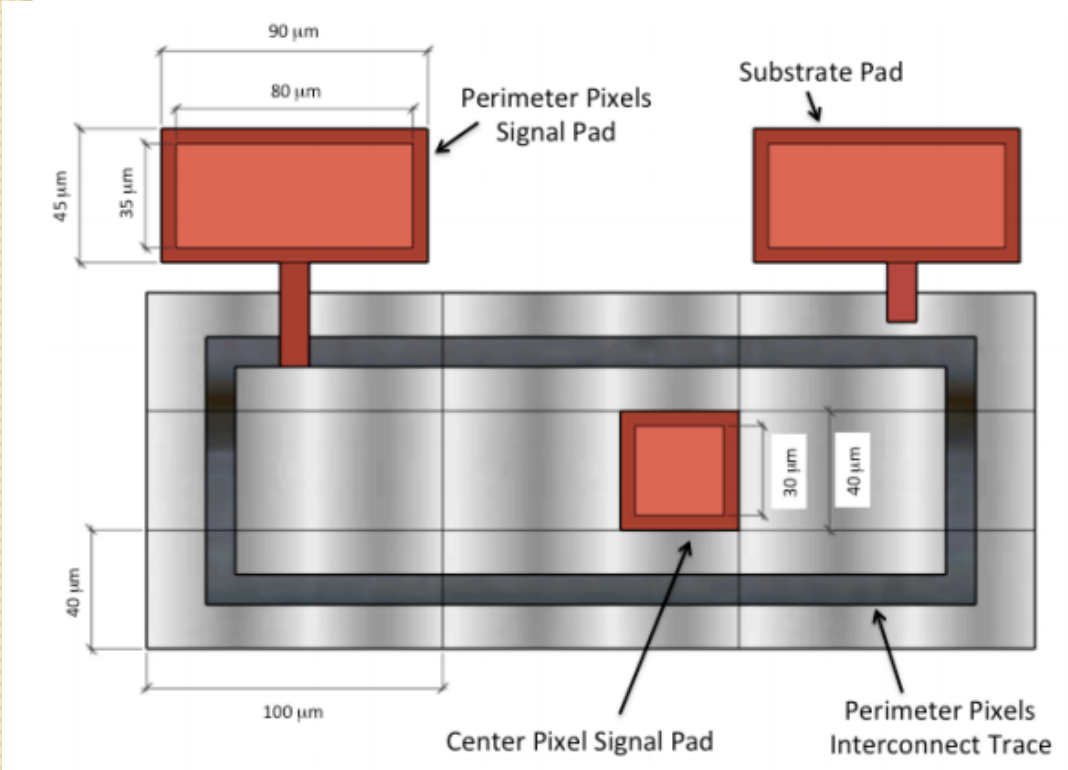
PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio	Extra circuitry
PPA01	45µm	100µm	30%	13.0%	
PPA02	45µm	100µm	50.4%	34.5%	
PPA03	45µm	200µm	30%	22.7%	
PPA04	45µm	200µm	50.4%	44.0%	
PPA05	45µm	400µm	30%	27.4%	
PPA06	45µm	400µm	50.4%	48.7%	
PPA07	45µm	800µm	30%	29.8%	
PPA08	45µm	800µm	50.4%	51.0%	
PPA09	45µm	100µm	30%	13.0%	Special bond pads for E-TCT
PPA10	45µm	200µm	30%	22.7%	Without contact ring around each pixel, but with contact ring around the entire array having a separate pad
PPA11	45µm	200µm	30%	22.7%	With contact ring around each pixel that violates the design rules by having a symmetric width. NOTE this pixel was added twice
PPA12	45µm	200µm	30%	22.7%	With contact ring around each pixel that violates the design rules by having a symmetric width. NOTE this pixel was added twice

Table 3.2-b Passive Pixel Array pad location



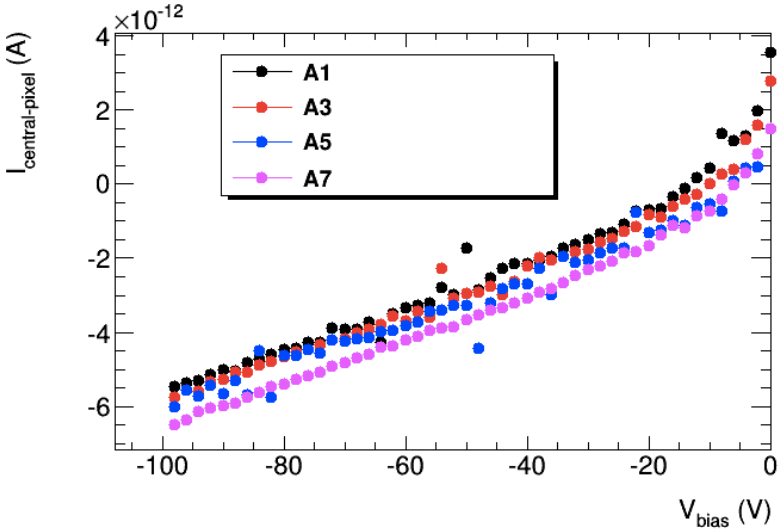
pixel IV measurement setup

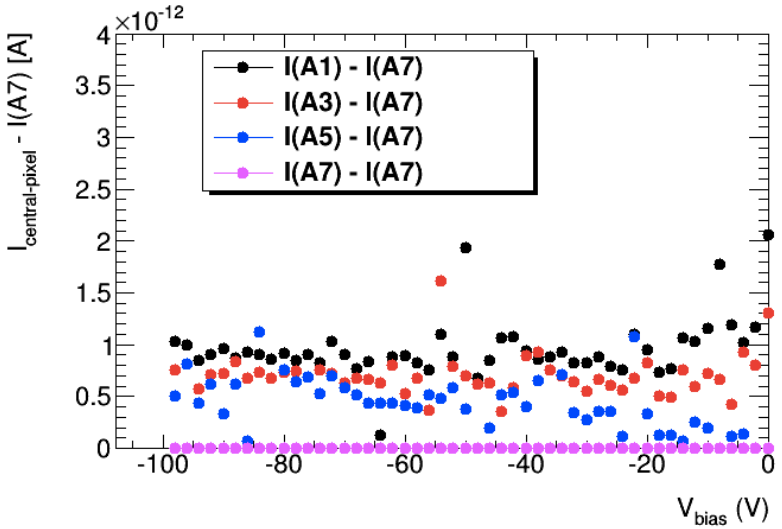
- Substrate: Biased at -HV
- Perimeter pixels: grounded
- Central pixel: grounded



I-V curve in CHESS1 chip

- No breakdown up to 100V bias voltage
- I-V curve in different pixel array is similar
  - Between different pixel size from 45X100um to 45X800um

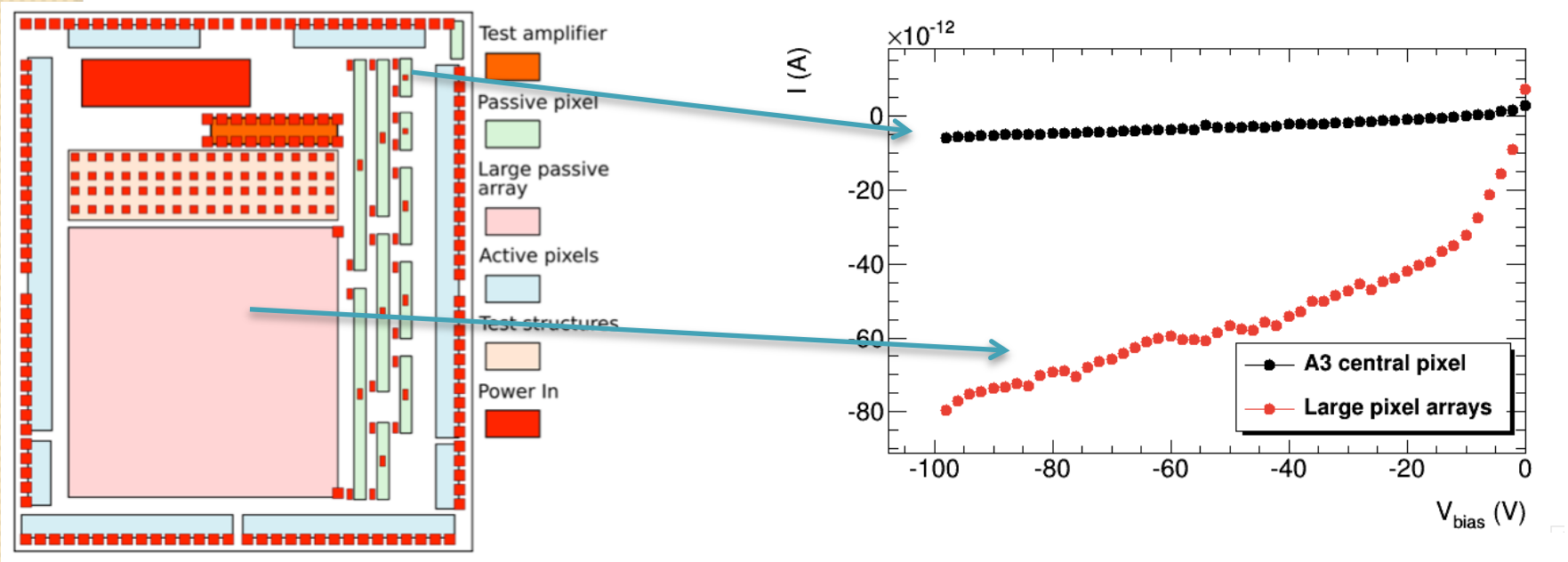




PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA01	45μm	100μm	30%	13.0%
PPA03	45μm	200μm	30%	22.7%
PPA05	45μm	400μm	30%	27.4%
PPA07	45μm	800μm	30%	29.8%

I-V (single pixel Vs pixel array)

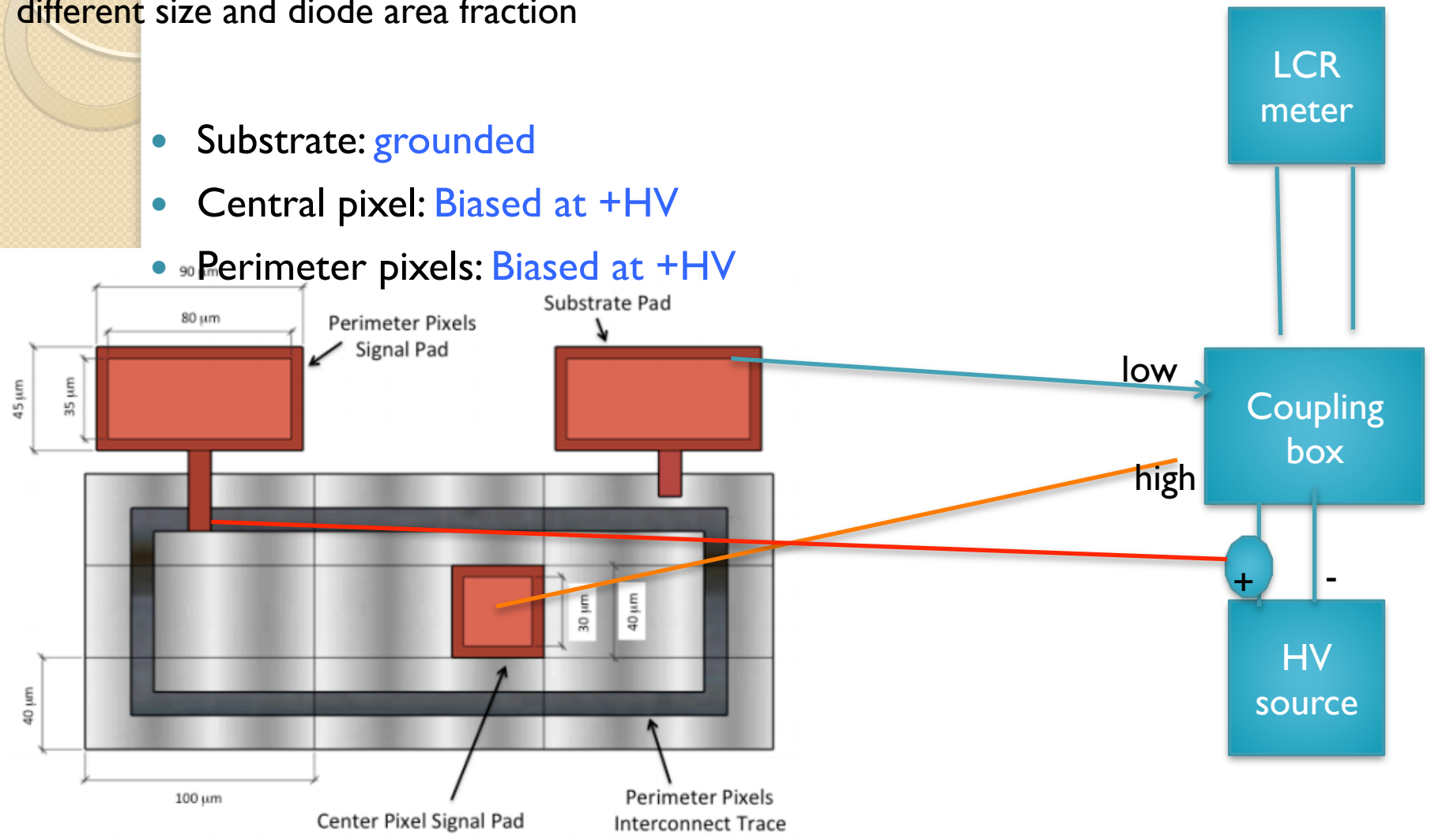
- A3 pixel :
  - 45X200um pixel , diode area fraction of 30%
- Large pixel array:
  - 45X200um pixel
  - diode area fraction of 40%
  - 2X2 mm^2



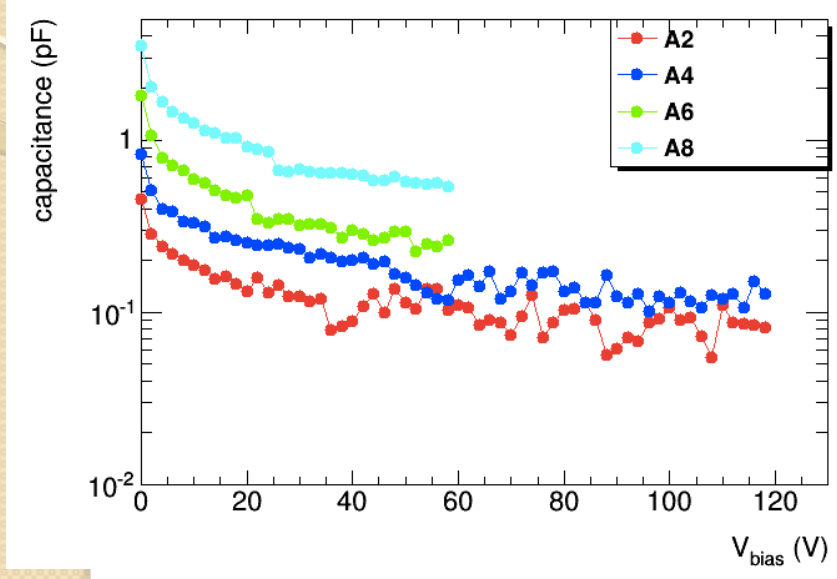
Setup for single-pixel capacitance measurement

One of CHESS1 submission is to measure the capacitance of passive pixel with different size and diode area fraction

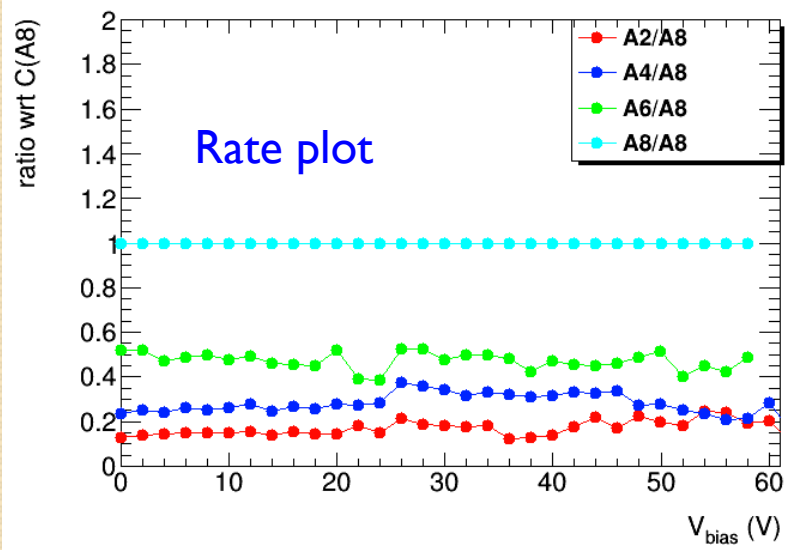
- Substrate: grounded
- Central pixel: Biased at +HV
- Perimeter pixels: Biased at +HV



Capacitance of central pixel array with different size



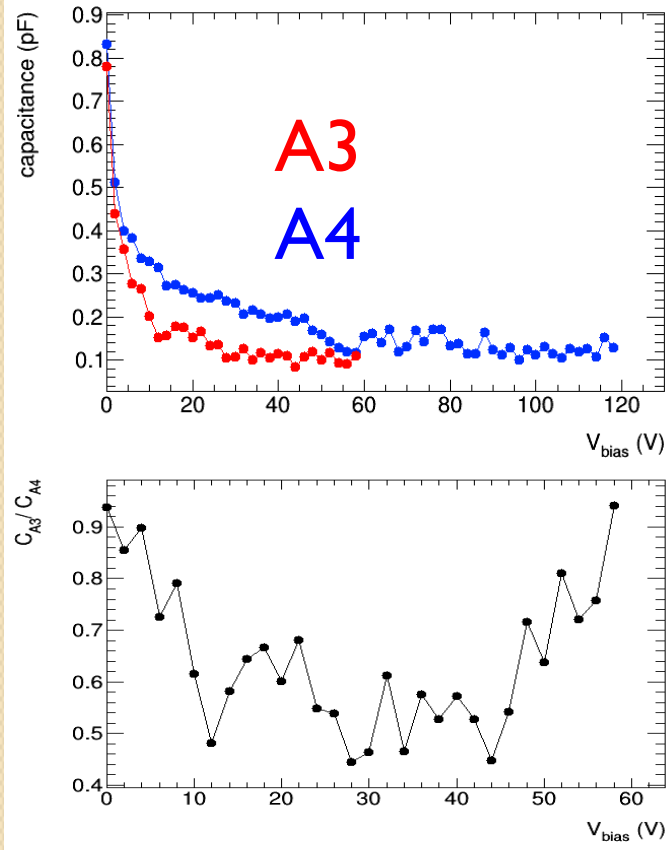
- At low bias voltage
- C(A4) is about 1/2 of C(A8)
- C(A6) is about 1/4of C(A8)
- C(A8) is about 1/8 of C(A8)



PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA02	45μm	100μm	50.4%	34.5%
PPA04	45μm	200μm	50.4%	44.0%
PPA06	45μm	400μm	50.4%	48.7%
PPA08	45μm	800μm	50.4%	51.0%

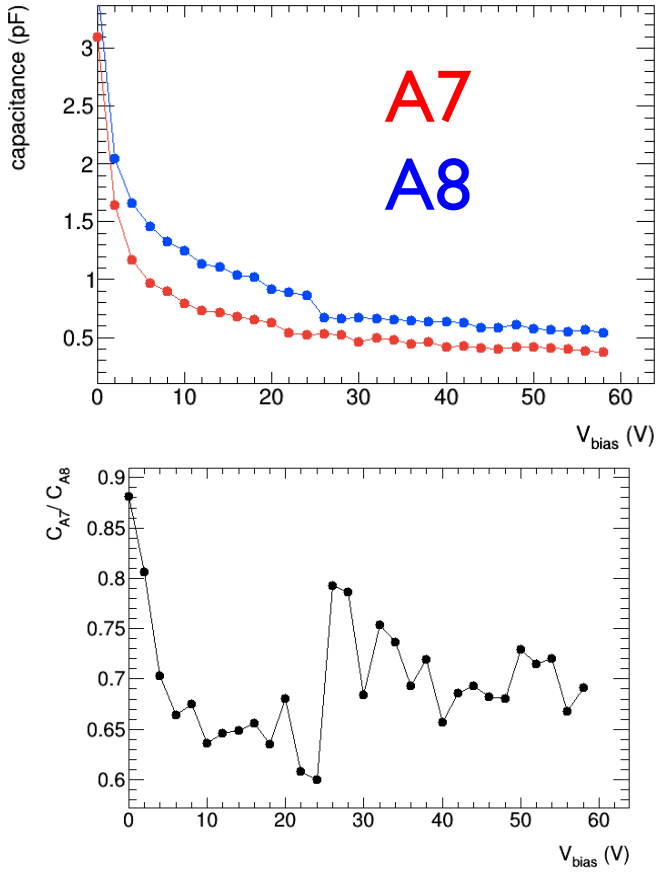
Capacitance of pixel array with different diode area fraction

PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA03	45μm	200μm	30%	22.7%
PPA04	45μm	200μm	50.4%	44.0%



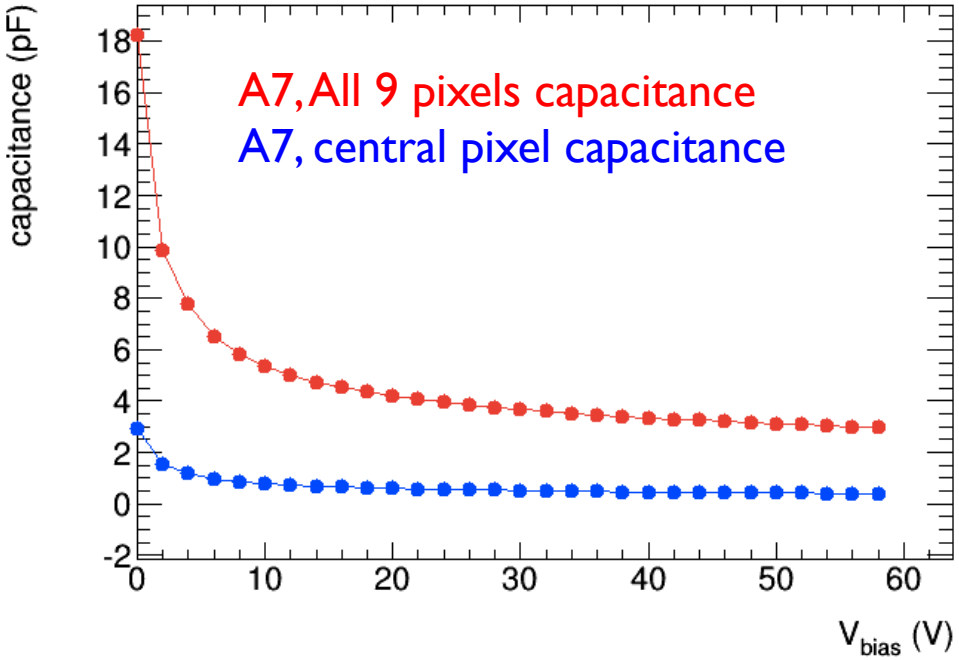
- C(A3) is about 50%~90% of C(A7)

PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA07	45μm	800μm	30%	29.8%
PPA08	45μm	800μm	50.4%	51.0%

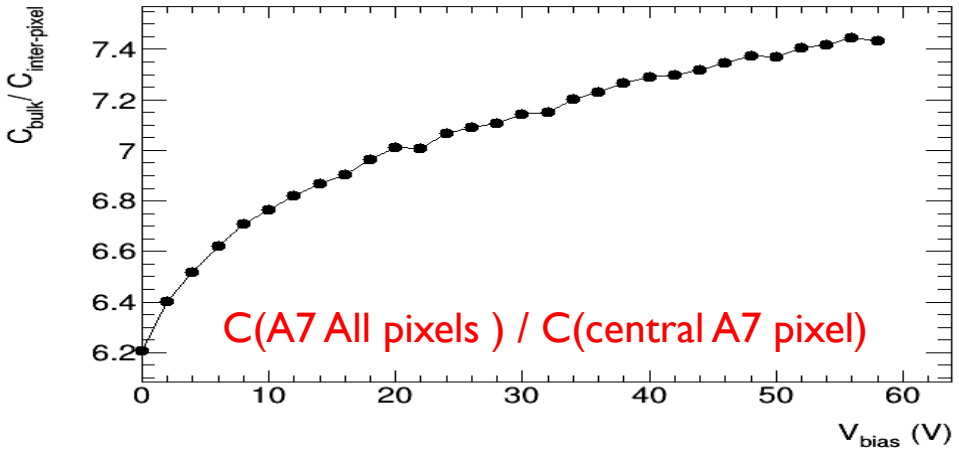


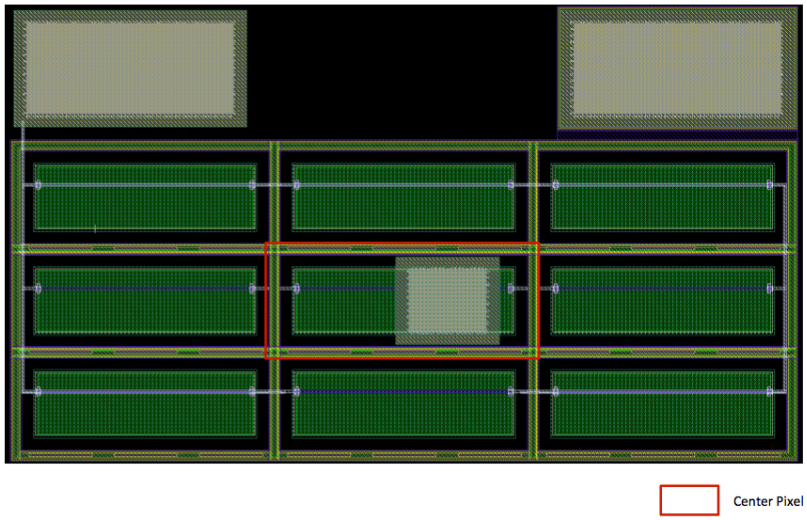
- C(A7) is about 70% of C(A8)

C(central pixel) Vs C(all pixels)



PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA07	45µm	800µm	30%	29.8%

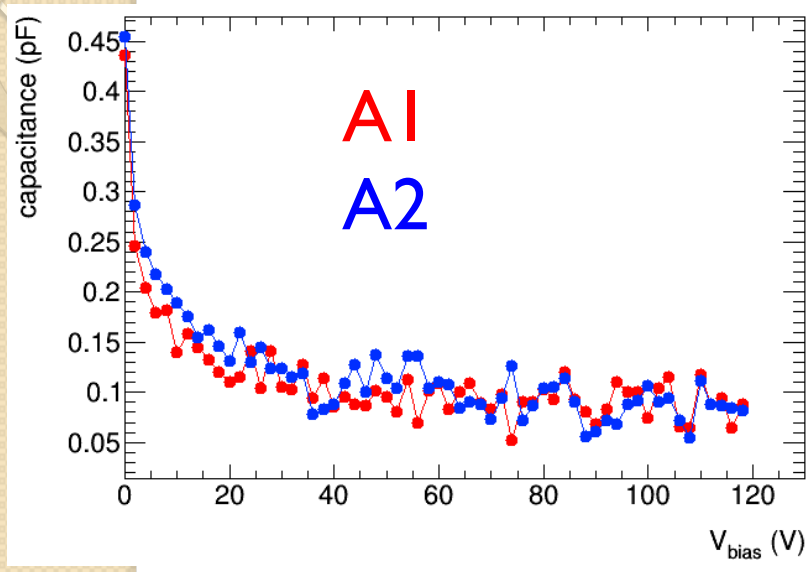




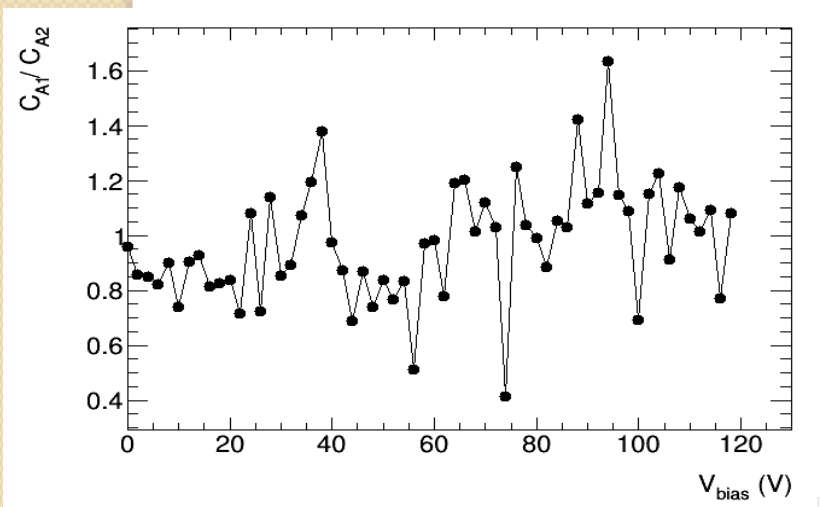
Summary

- Preliminary I-V and capacitance results for HV-CMOS CHESS1 chips
  - I-V measurement
    - Can Biased up to 120V without breakdown
    - Low leakage current (pA level)
  - C-V measurement
    - The central pixel capacitance at low bias voltage is roughly proportional to pixel size.
    - Observe lower capacitance for pixel with lower diode fraction

Pixel size=45X100um



- C(A1) is about 0.8~1.1 of C(A2)



PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA01	45μm	100μm	30%	13.0%
PPA02	45μm	100μm	50.4%	34.5%

Pixel size=45X200 um

- A3: 30% Nwell
- A4:50% nwell
- A10: 30%, without contact between pixel
- A11,A12: 30% with reduced contact between pixel