HVStripV1 Testing Status

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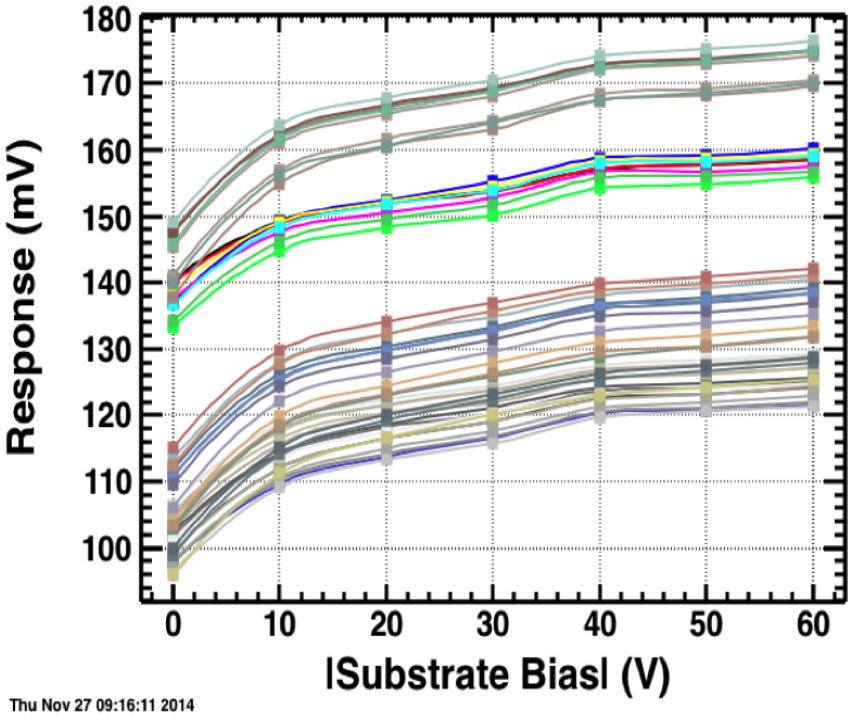
Previously

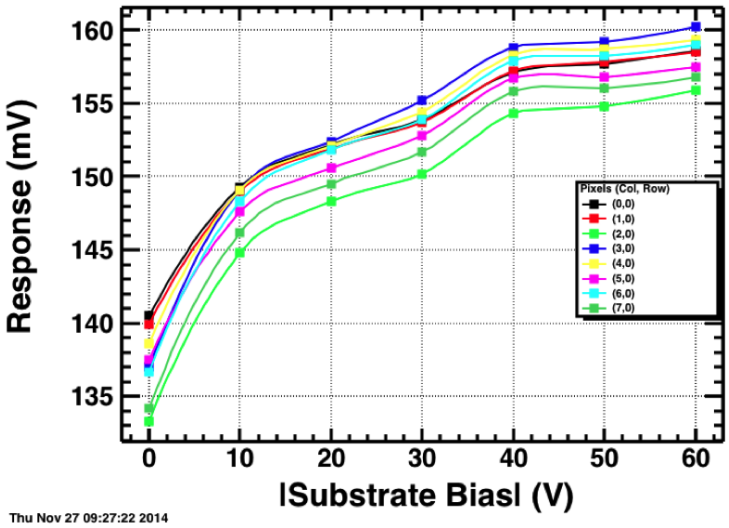
- Linearity of response investigation showed linear behaviour of the pixel matrix
- Different gain gradients were observed amongst certain pixel groups
- Change in gain as a function of applied bias was presented for a few pixels

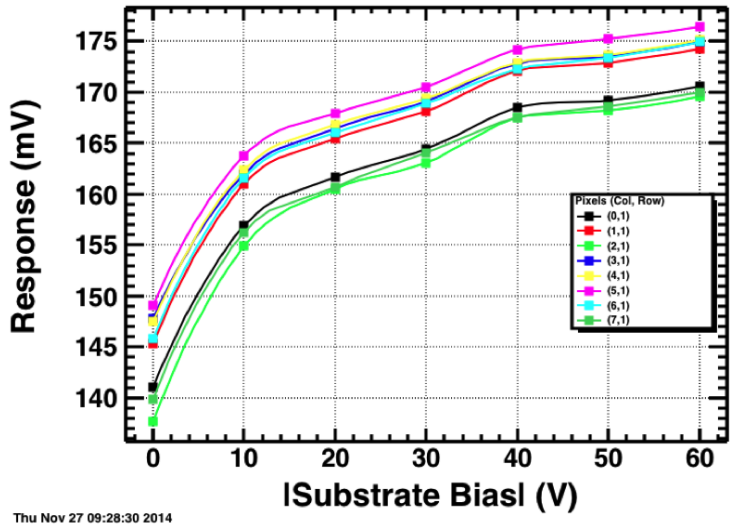
Bias Sweep Continued (1)

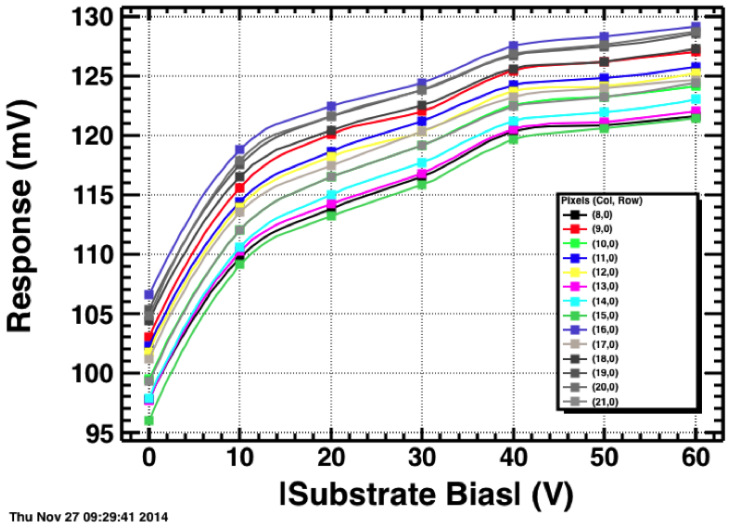
- Change in gain at constant charge injection as a function of bias voltage is observed in all pixels
- 1V pulses were used ($\approx 3120e^-$)
- Automation of data acquisition was achieved by implementing LabView VI

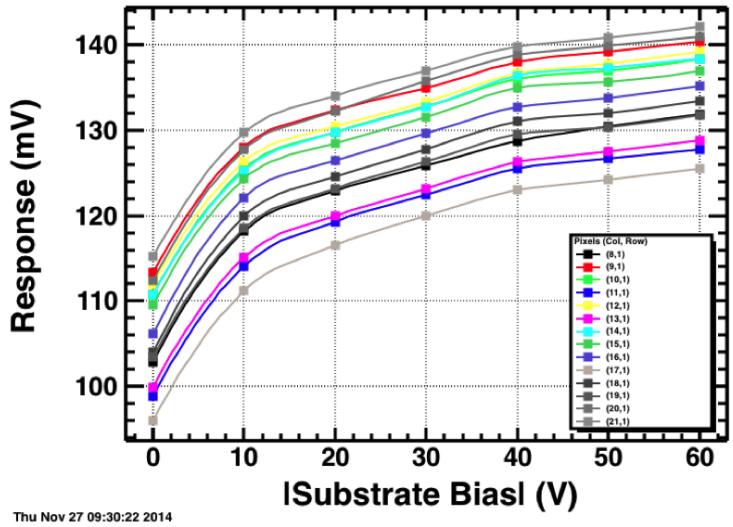


Bias Sweep Continued (2)



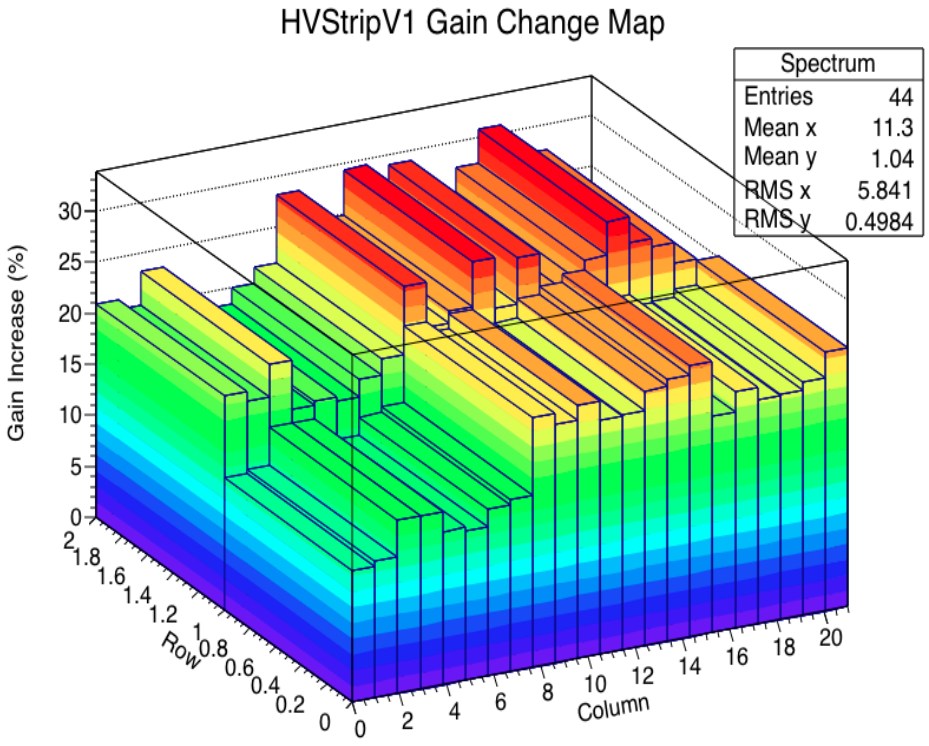




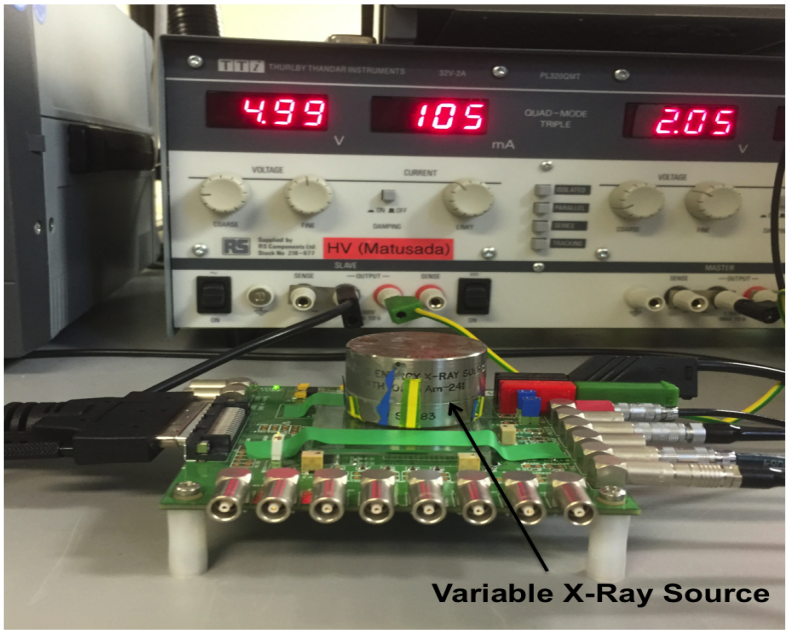


Bias Sweep Continued (3)

- Change in gain was compared between 0V and -60V bias voltages
- Average increase in gain among pixels is 22%, consistent with the increase observed at Oxford
- Pixels with enclosed feedback transistor exhibit bigger change (25% increase on average compared to 18% for pixels with linear transistor)

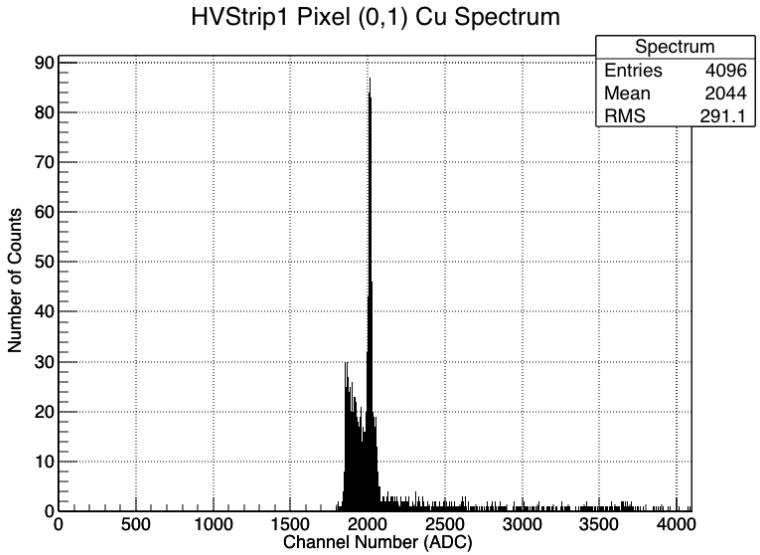


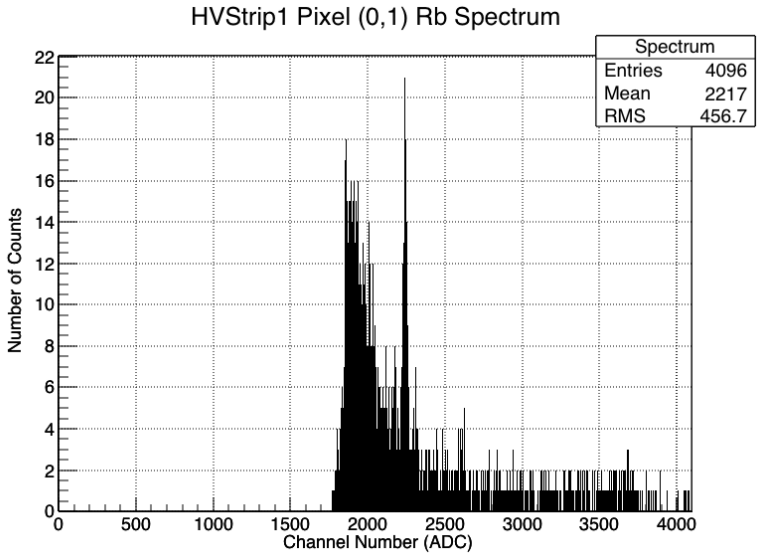
Source Scans (1)

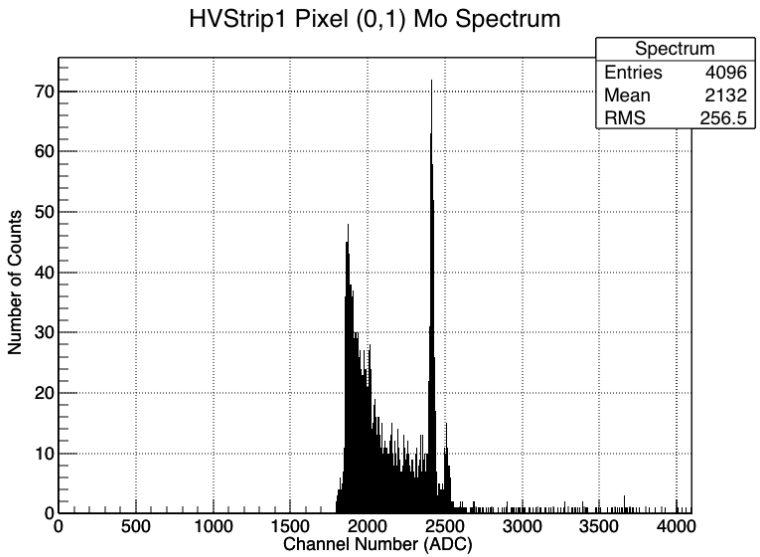


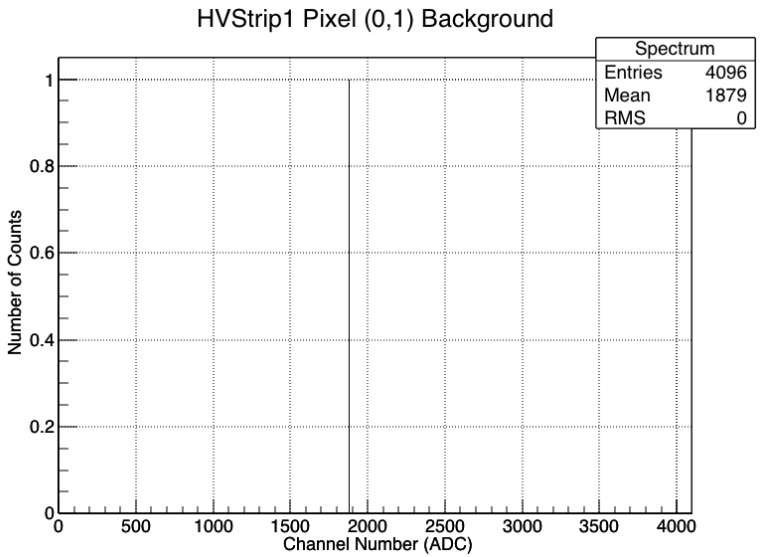
- HVStripV1 was illuminated with variable X-Ray source
- Spectra of Cu, Mo and Rb were taken from a single pixel $(0, 1)$
- Measurements were done with multi-channel analyzer MCA8000D
- Bias of $-60V$ was applied during all measurements

Source Scans (2)

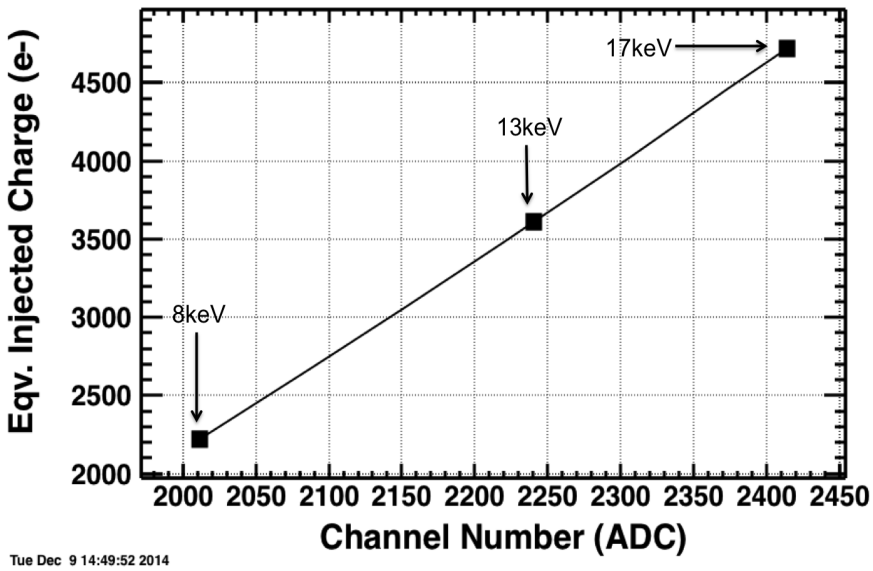








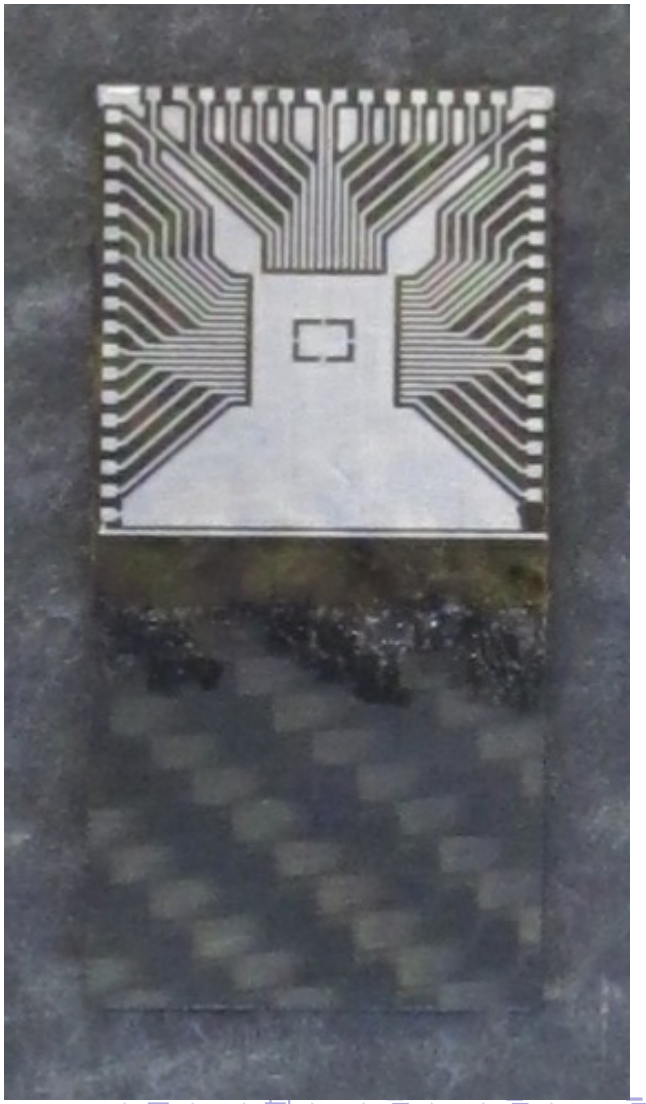
Source Scans (3)



- Cu, Rb, Mo characteristic lines correspond to $8keV$, $13keV$ and $17keV$ respectively ($\approx 2200e^-, 3600e^-, 4700e^-$)
- Linear behaviour observed as in charge injection tests

MOSFETs (1)

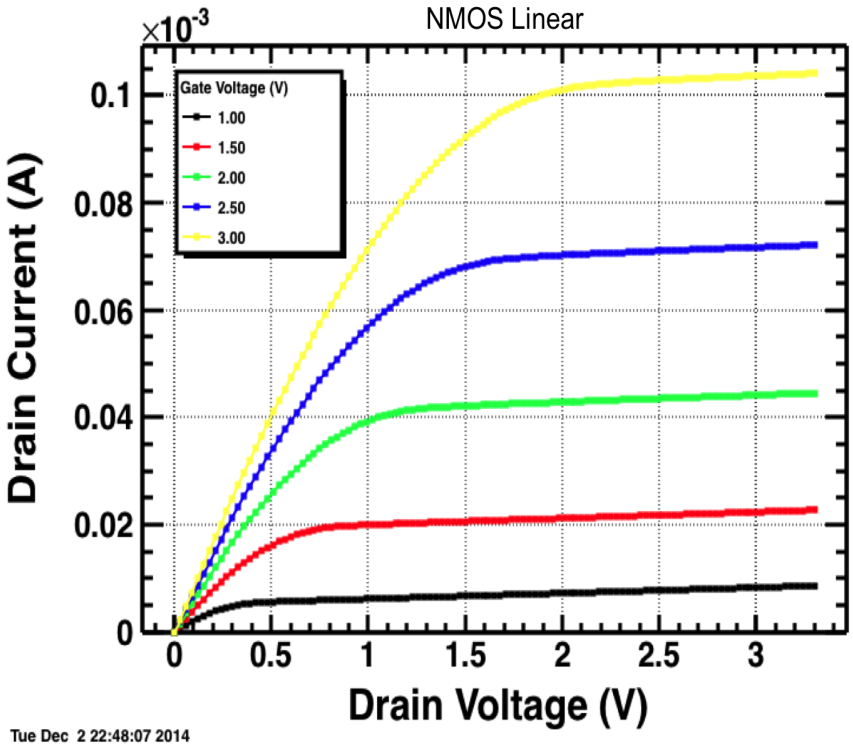
- HVStripV1 contains the following test MOSFETs – NMOS Linear, NMOS Enclosed, PMOS Linear
- NMOS source terminals are grounded, whereas PMOS source is always held at 3.3V (maximum). Drain voltages are set from an external power supply
- Gate voltages of all MOSFETs are controlled by Th1 terminal (range $0V - 3.3V$)

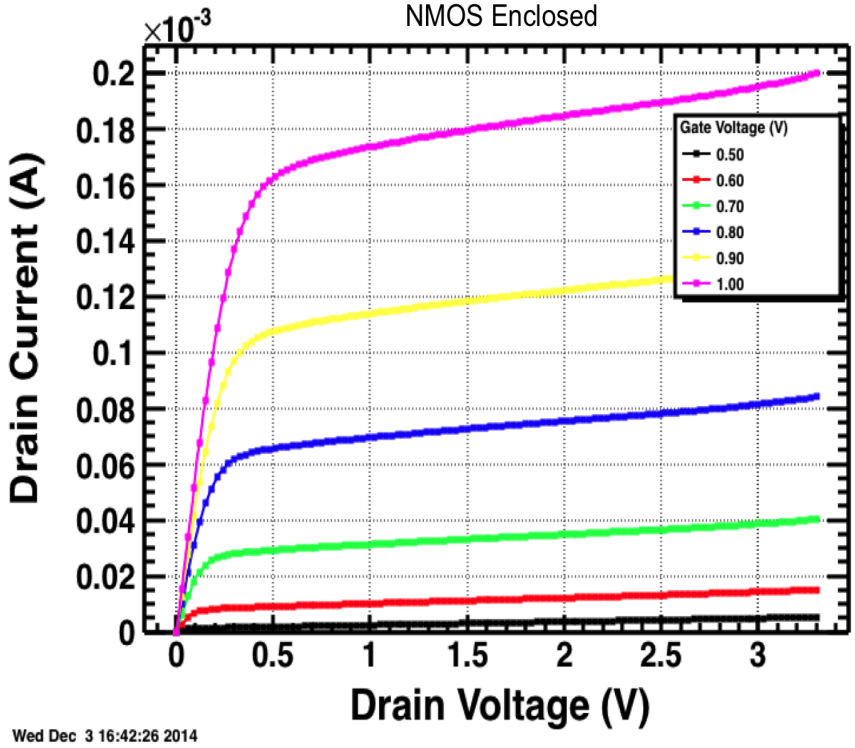


MOSFETs (2)

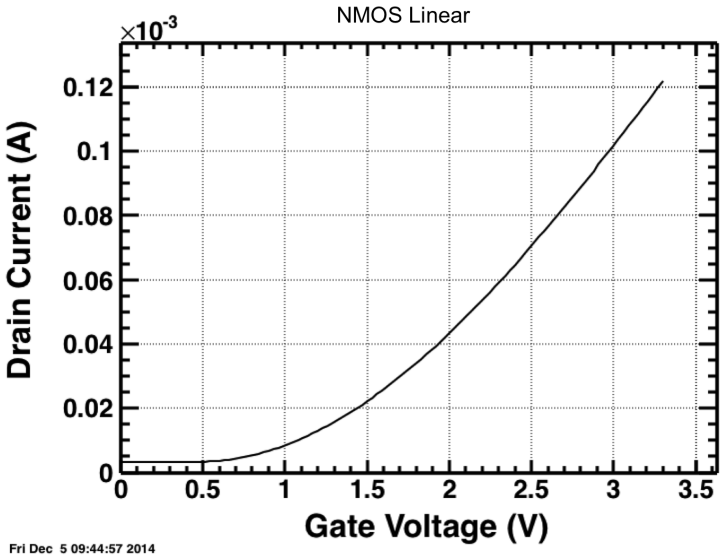
- Measurements of Drain Current vs. Gate Voltage, and Drain Current vs. Drain Voltage at various gate voltages were taken
- For Drain Current vs. Gate Voltage measurements the drain voltage was kept at max 3.3V to ensure operation in saturation mode
- Compliance currents were set to $350\mu A$

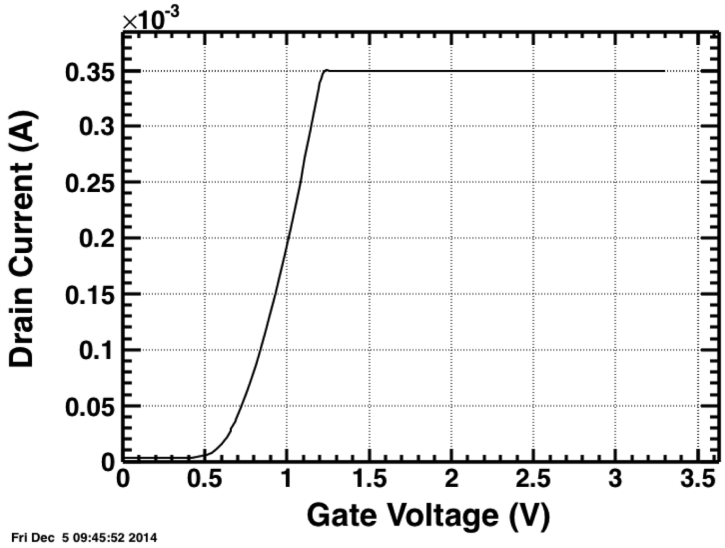
MOSFETs (3)

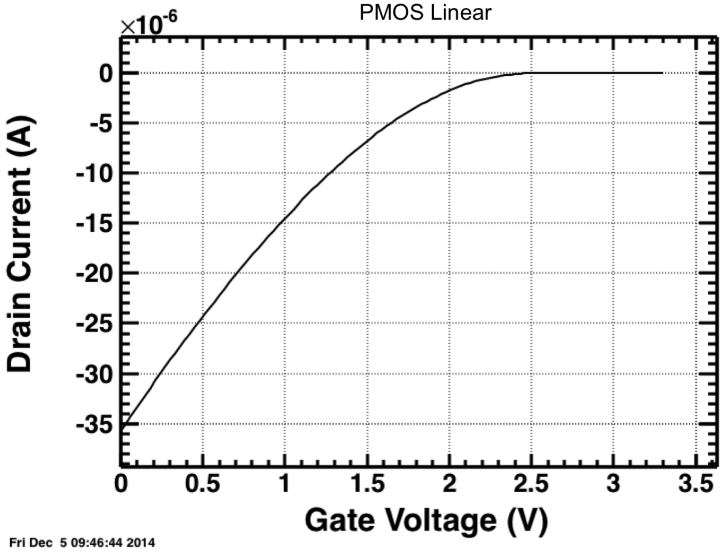

NMOS Linear
×10^-3
Drain Current (A)
Drain Voltage (V)
Gate Voltage (V)
1.00
1.50
2.00
2.50
3.00
0
0.02
0.04
0.06
0.08
0.1
0
0.5
1
1.5
2
2.5
3
Tue Dec 2 22:48:07 2014


NMOS Enclosed
×10^-3
Drain Current (A)
Drain Voltage (V)
Gate Voltage (V)
0.50
0.60
0.70
0.80
0.90
1.00
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
0.18
0.2
0
0.5
1
1.5
2
2.5
3
Wed Dec 3 16:42:26 2014

MOSFETs (4)


NMOS Linear
×10^-3
Drain Current (A)
Gate Voltage (V)
Fri Dec 5 09:44:57 2014


×10^-3
Drain Current (A)
Gate Voltage (V)
Fri Dec 5 09:45:52 2014


PMOS Linear
×10^-6
Drain Current (A)
Gate Voltage (V)
Fri Dec 5 09:46:44 2014

Further Plans

- Timewalk as a function of pulse height measurements
- Response to Fe-55 source as a function of bias voltage investigation
- C-V measurements of test structures