

Update on IV measurement in HVCOMS CHESSI chip

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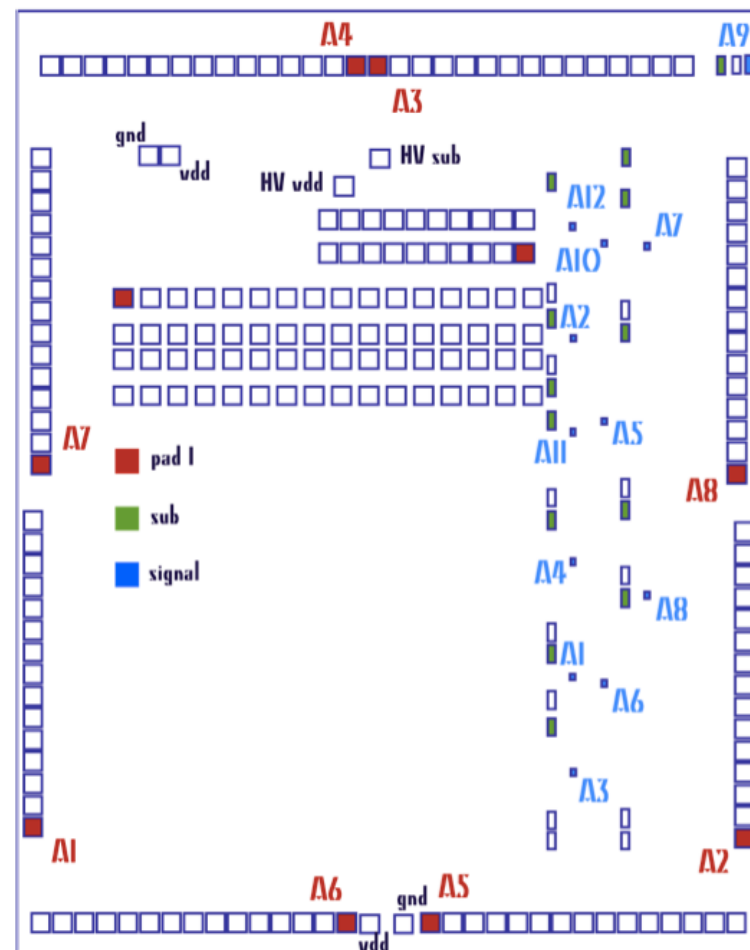
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Introduction

- AMS CHESSI HV-CMOS chip is available for testing
- Preliminary I-V and capacitance results :
 - I-V measurement
 - C-V Measurement

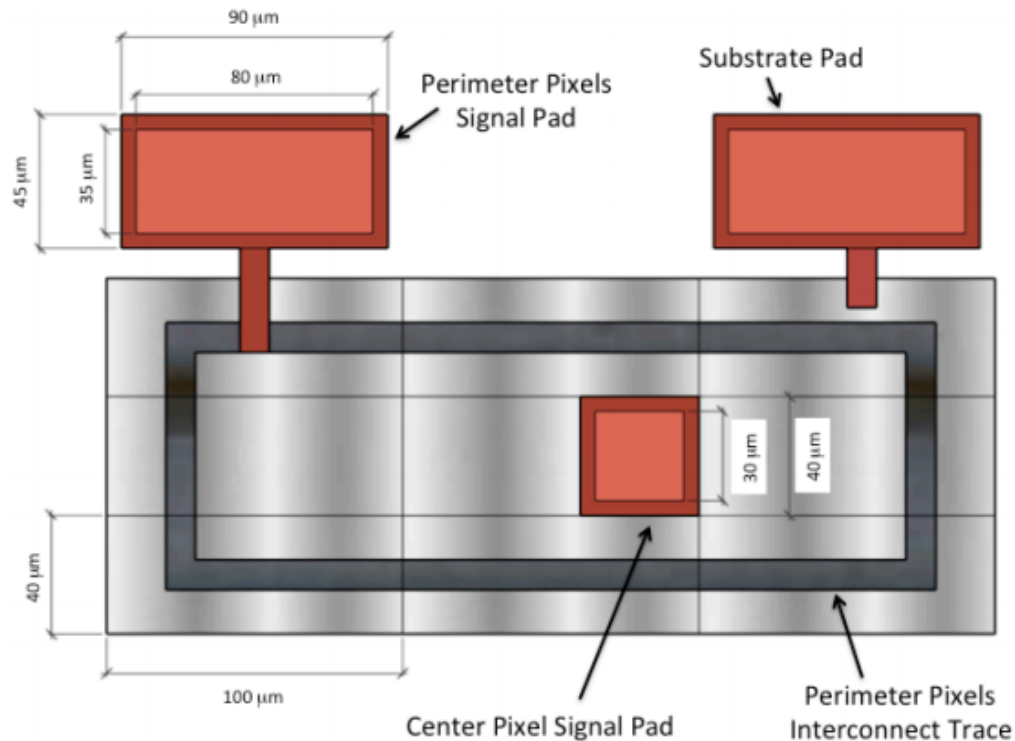
PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio	Extra circuitry
PPA01	45μm	100μm	30%	13.0%	
PPA02	45μm	100μm	50.4%	34.5%	
PPA03	45μm	200μm	30%	22.7%	
PPA04	45μm	200μm	50.4%	44.0%	
PPA05	45μm	400μm	30%	27.4%	
PPA06	45μm	400μm	50.4%	48.7%	
PPA07	45μm	800μm	30%	29.8%	
PPA08	45μm	800μm	50.4%	51.0%	
PPA09	45μm	100μm	30%	13.0%	Special bond pads for E-TCT
PPA10	45μm	200μm	30%	22.7%	Without contact ring around each pixel, but with contact ring around the entire array having a separate pad
PPA11	45μm	200μm	30%	22.7%	With contact ring around each pixel that violates the design rules by having a symmetric width. NOTE this pixel was added twice
PPA12	45μm	200μm	30%	22.7%	With contact ring around each pixel that violates the design rules by having a symmetric width. NOTE this pixel was added twice

Table 3.2-b Passive Pixel Array pad location



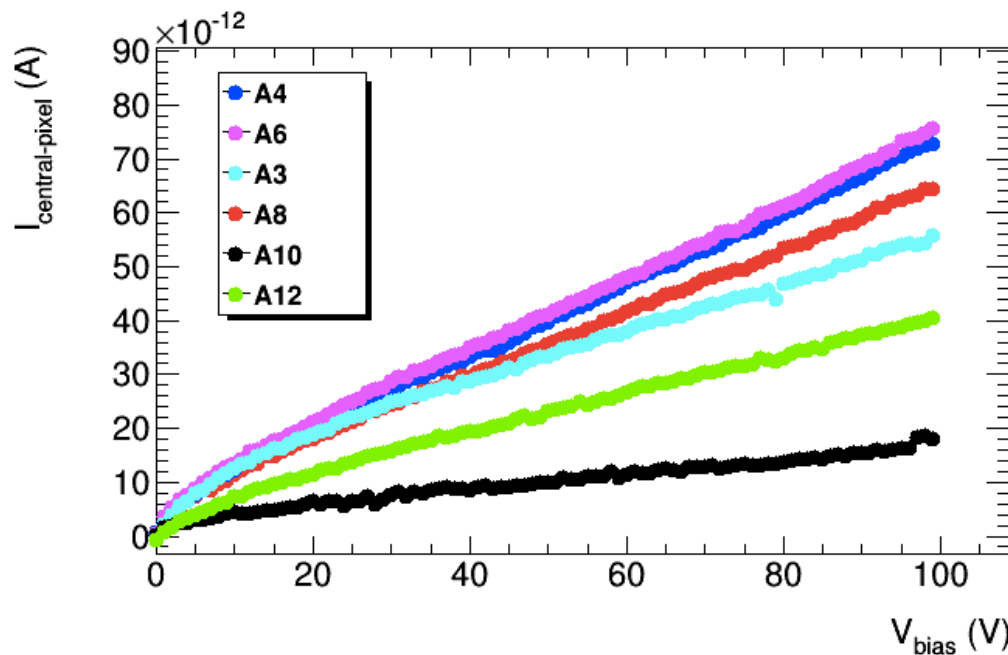
pixel IV measurement setup

- Substrate: grounded
- Perimeter pixels: +HV
- Central pixel: +HV



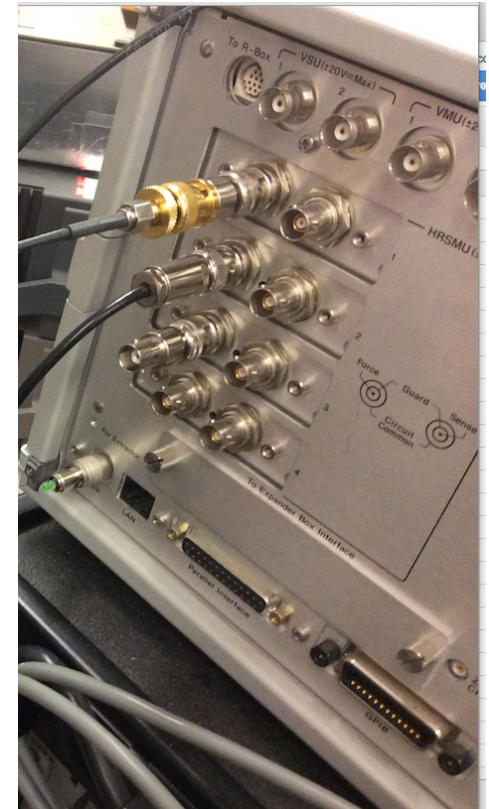
Old I-V results in Dec 1st

- Leakage current is up to 90pA
- Found very large noise contribution
- About ~50pA noise when it is open
 - Mainly due to BNC cable



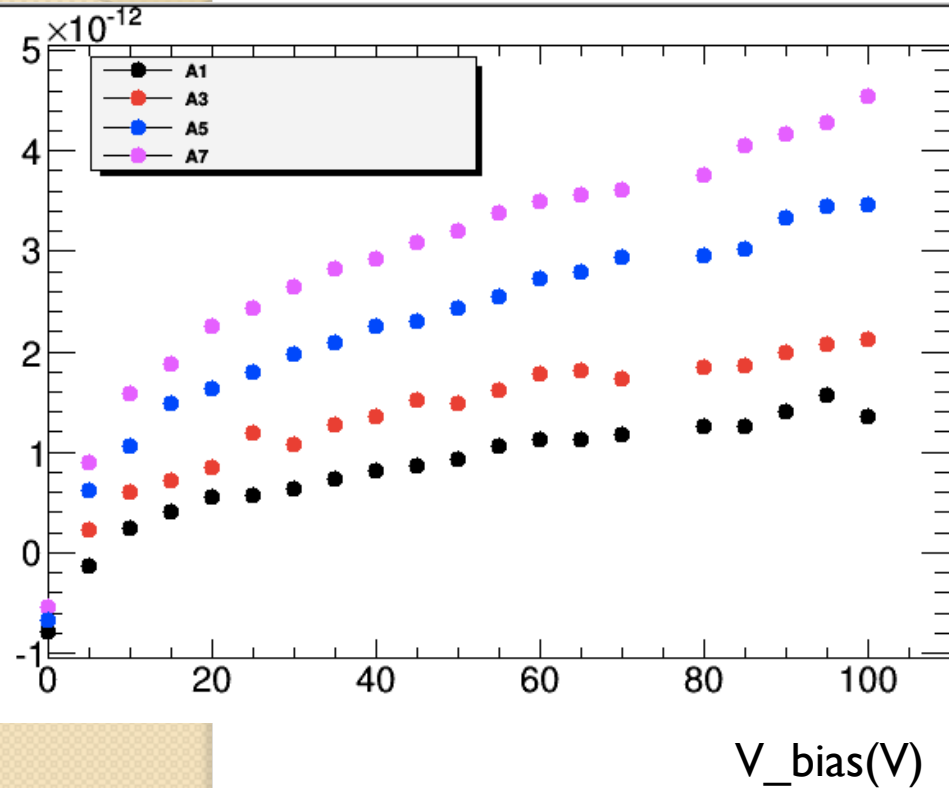
Low noise setup

- In order to measure low leakage current.
- We now used low loss SMI cable.
 - Noise level about 500 fA



Updated results on central pixel I-V

Leakage current(A)



PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA01	45 μ m	100 μ m	30%	13.0%
PPA03	45 μ m	200 μ m	30%	22.7%
PPA05	45 μ m	400 μ m	30%	27.4%
PPA07	45 μ m	800 μ m	30%	29.8%

Summary

- Updated results from I-V measurements.
 - Reduce noise using low noise setup.
 - I-V curve makes more sense now.
 - leakage currents scale with pixel size.