Minutes of Strip CMOS sensor progress report meeting, V.0

*2014-11-25*

*Present: A.Grillo, D.Benjamin, Glasgow People, I.Mandic, J.Dopke, J.Zhang, M.Warren, Oxford, P.Anne, R.Turchetta, R.Nickerson, S.Gnzalez Sevilla, V.Fadeyev, Z.Liang, D.Muenstermann* [taken from Vidyo listing of attendees]

*Apologies: M.Stanitski*

INDICO address: <https://indico.desy.de/conferenceDisplay.py?confId=11285>

*Engineering Run*

There was discussion of the possible engineering run in AMS H35. This encompassed possible joint submission with the pixel community, SLAC, RD50. The pixel group needs a large fraction of the reticule. The sum of the ATLASstrip, SLAC and RD50 can add up to a whole reticule and it was decided that further consultation with the pixel group should be undertaken to see if they can work with less than ¾. If not then the way forward is to have a submission separate from pixels and in collaboration with SLAC and RD50. Vitaily will pursue this. It is believed that the time scale for the SLAC and RD50 designs is compatible with the ATLASstrip programme.

*TJ Submission*

It was reported that the TJ chips had been submitted 2 weeks ago. A February delivery is anticipated, with early March being likely for the start of testing. Preparation for testing will start at RAL and Oxford.

*DAQ*

There was no explicit DAQ report, with it be noted that work was ongoing.

*Testing CHESS1*

Preliminary I-V and C-V measurements were reported with no breakdown to 120V. The maximum voltage is 120V because of design rules. It was suggested that higher voltages be tried, and this will be done when there are enough samples to be able to sacrifice them.

The leakage currents were low, at the pA level. At lower voltages the pixel capacitance is proportional to voltage and a lower capacitance is measured for pixels with a lower diode fraction.

*Testing HVStrip1*

Testing of HVStrip1 was reported using test pulse injection and readout via the amplified pixels. The gain depends on the bias voltage and there was discussion of the possible cause of this. It was conjectured that this might be simply charge sharing between the amplifier input capacitance and the sensor capacitance, which is bias dependent, but this was left to be considered after the meeting.

The noise was also observed to be bias dependent.

*Test Kit Status*

The stock of HVstripv1 hardware was reported and the plan to produce 100 more daughter boards and 25 motherboards to be assembled at Oxford was agreed.

The preparation for CHESS test boards was described and the proposal to produce a ‘snap off’ daughter discussed. Suggestions were made for the way to proceed. The primary issue was the size of the proposed daughter when irradiation facilities were considered.

*Further discussion*

There was discussion of the fact that irradiated NMOS transistors had been observed to leak and the way forward on that issue.