Upgrade of the ATLAS Level-1 Calorimeter Trigger for the sLHC

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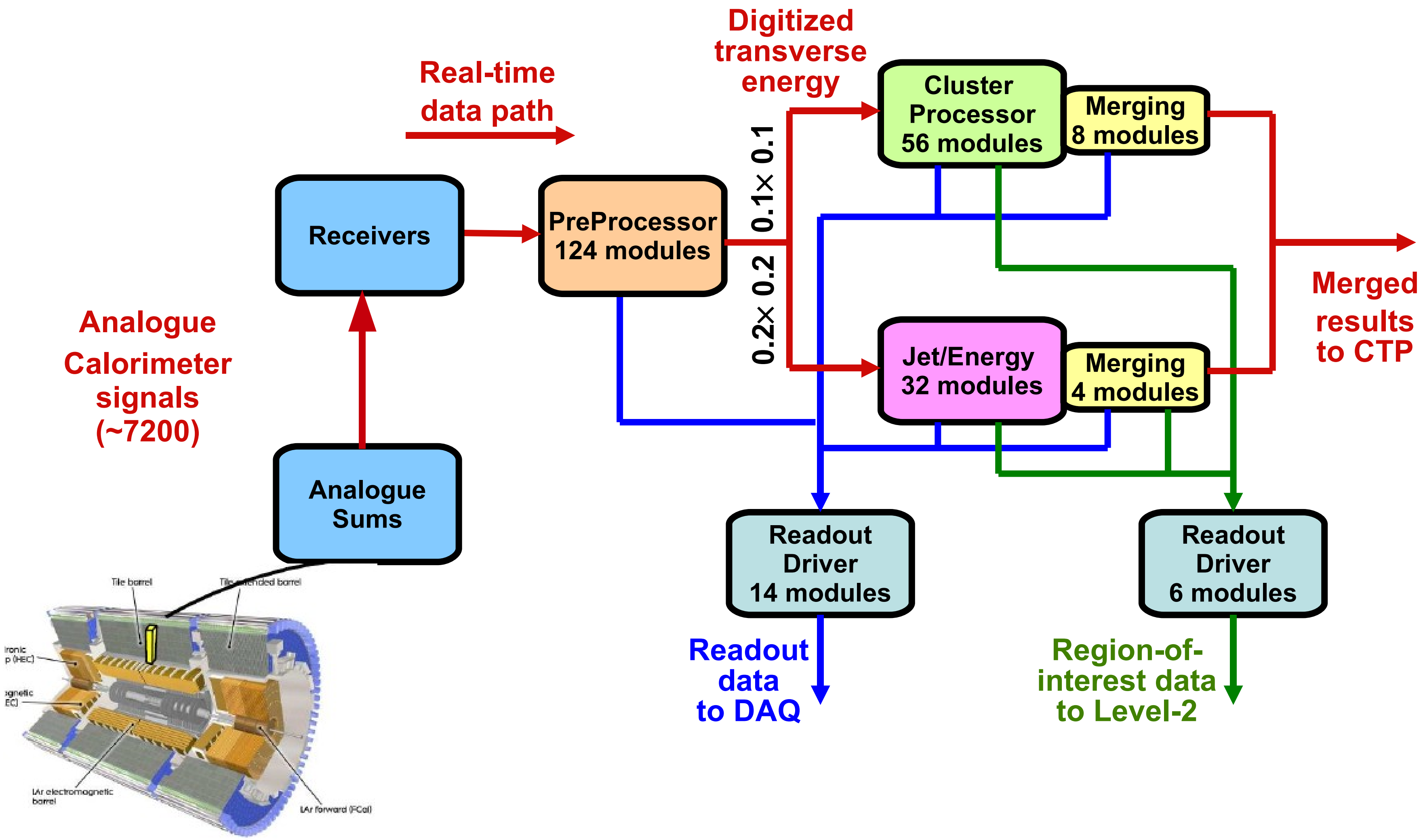
Outline

- Current L1Calo architecture
- Upgrade for Phase I
- Upgrade for Phase II

ATLAS Level-1 Calorimeter Trigger (L1Calo)



<u>Features:</u>

Real-time Path: Fixed Latency (~1μs); Pipeline processing; Massive parallelism; FPGA and ASIC based

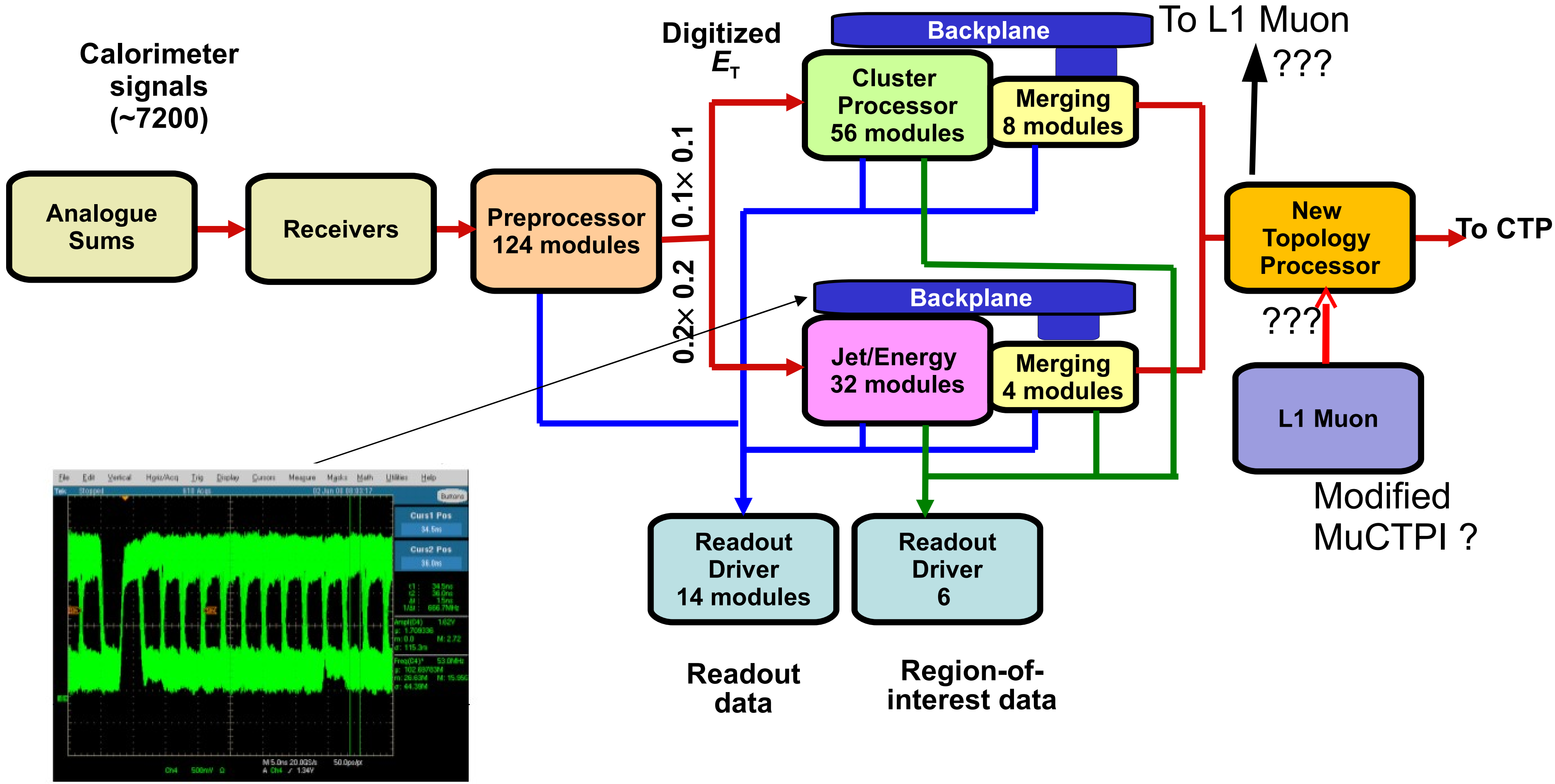
Conditions after LHC Upgrade

- Phase 1 (L: ~2-3*10^{34}; ~60-80 pile-up events; ~2013)
  - No change to Calorimeter and Muon detectors
  - Unchanged latency, TTC, ROD/S-Link data volume
  - Same LHC timing

- Phase 2 (L: ~10^{35};~400 pile-up events;~2017/2018;)
  - Major changes possible (and required)
  - New L1Calo, L1Muon, L1Track

- Idea is to keep the same (or similar) L1A rates

L1Calo Upgrade. Phase 1



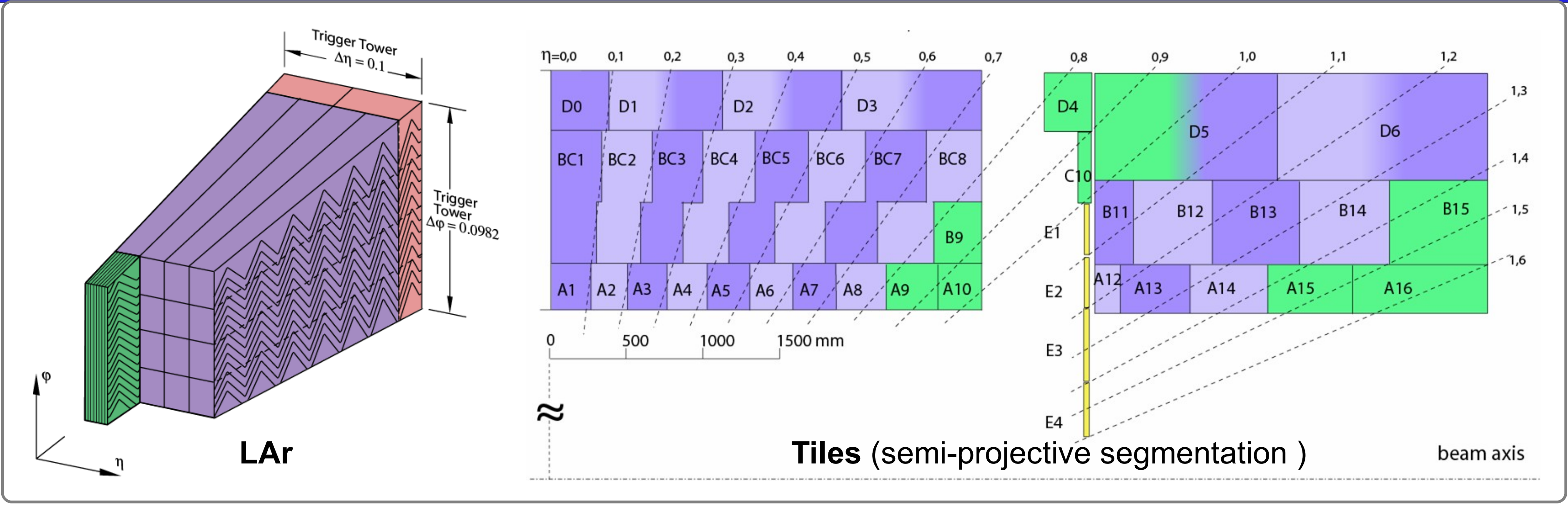
320 Mbits, CMOS 2.5V

- Add a new topological trigger and/or do more work in CTP
- Increase a number of “Trigger Menu Items”

L1Calo Upgrade. Phase 2

- Increase L1Calo data from 8 to ~12 bits
- L1A rate up to 100 kHz - but higher rate to be discussed with ID community
- Latency 5-6 μs. Current 2.5 μs will not be enough
- We should find and count clusters. Output data to contain details, e.g.
  - Flag to indicate one cluster or many
  - η position of the highest peak
    - If ATLAS uses track trigger at L1 or L1.5, it will be useful to match tracks to precise cluster η positions

L1Calo Upgrade. Phase 2



- Better selection algorithms:
  - Improve resolution and background discrimination
- Finer granularity inputs => "minitowers"
  - separate signals from each calorimeter depth, smaller area in η, φ:
    - e.g. 0.05 x 0.05 (middle)
    - 0.05 x 0.1 (front and back)

Data from Calorimeters

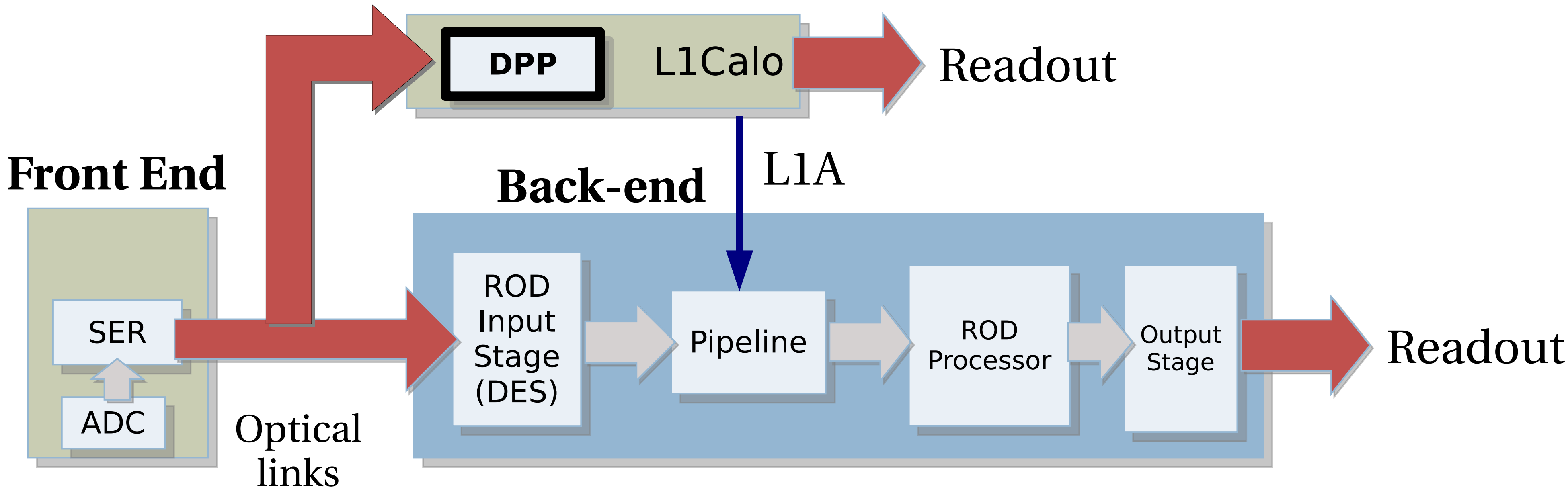
- Digitization at 40 MHz
  - No analogue pipelines
- Energy calculations and LVL-1 sums performed at beam crossing rate.
  - Analog trigger towers replaced with digital implementation
- For L1Calo: all cells contributing to a given minitower:
  - are brought to a common analogue phase and shape before digitisation
  - digitised by FADCs aligned with pulse peak and using a common clock
- Use FPGA:
  - Use dedicated FPGA DSP blocks (Multiply-Accumulate blocks)

New Detector (Tile and LAr) Electronics

- Common:
  - Digitization in FE. Transmission to BE at detector granularity at each BC.
  - Pipeline implementation in BE.
  - Data processing in RODs at L1 rate.
  - Control , monitoring and TTC interface.
- The different architectures depend on the placement of L1Calo Preprocessors
  - Off-detector
    - Next to RODs
    - Next to L1Calo
  - On-detector

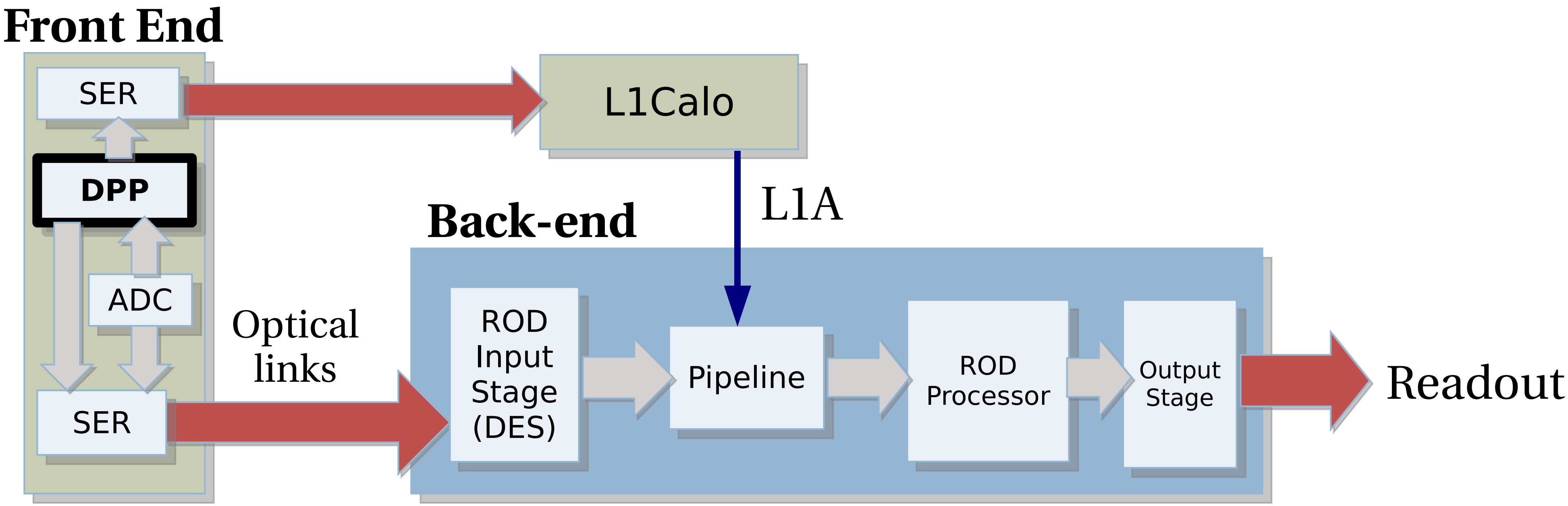
1a. Digital PreProcessor on Detector

- Same as current implementation, but:
  - Digitization in front-end
  - Digitized data transmission to back-end
  - Digitized data is transmitted to L1Calo
  - Independent detector and L1Calo readout chains



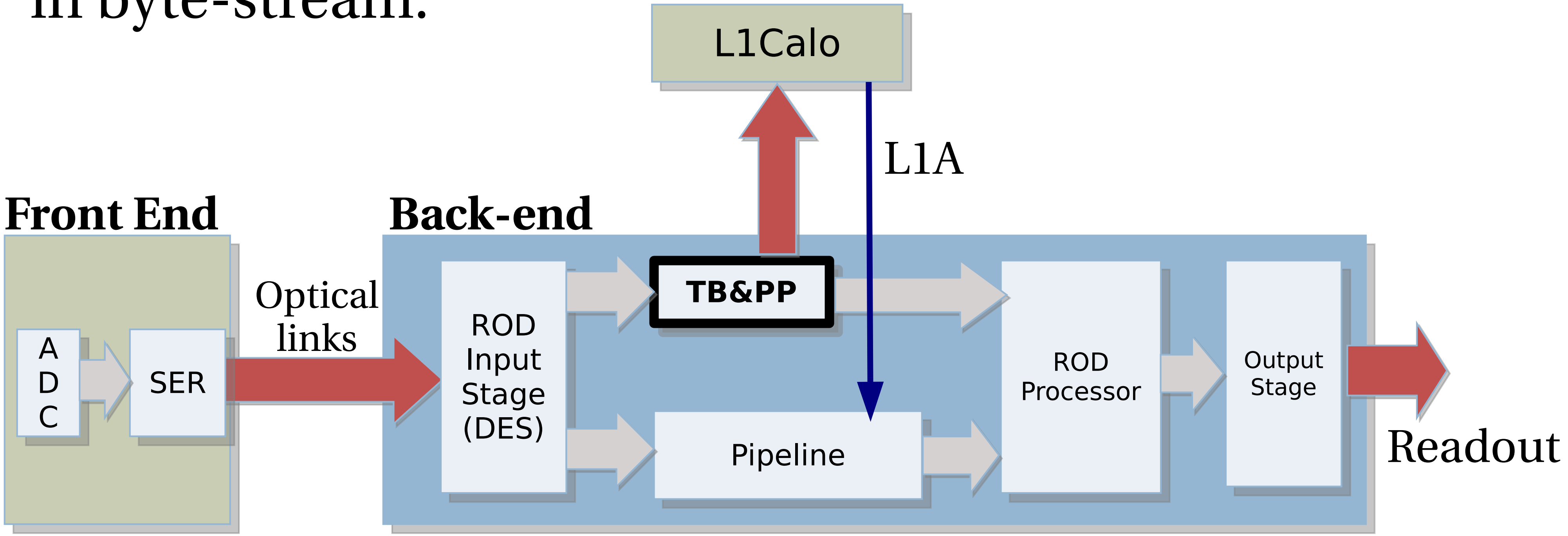
1b. Digital PreProcessor on Detector

- Similar to current implementation
- Digitization **and Tower computation** in front-end
- Digitized data transmission to back-end
- Digitized **and PreProcessed** data is transmitted to L1Calo



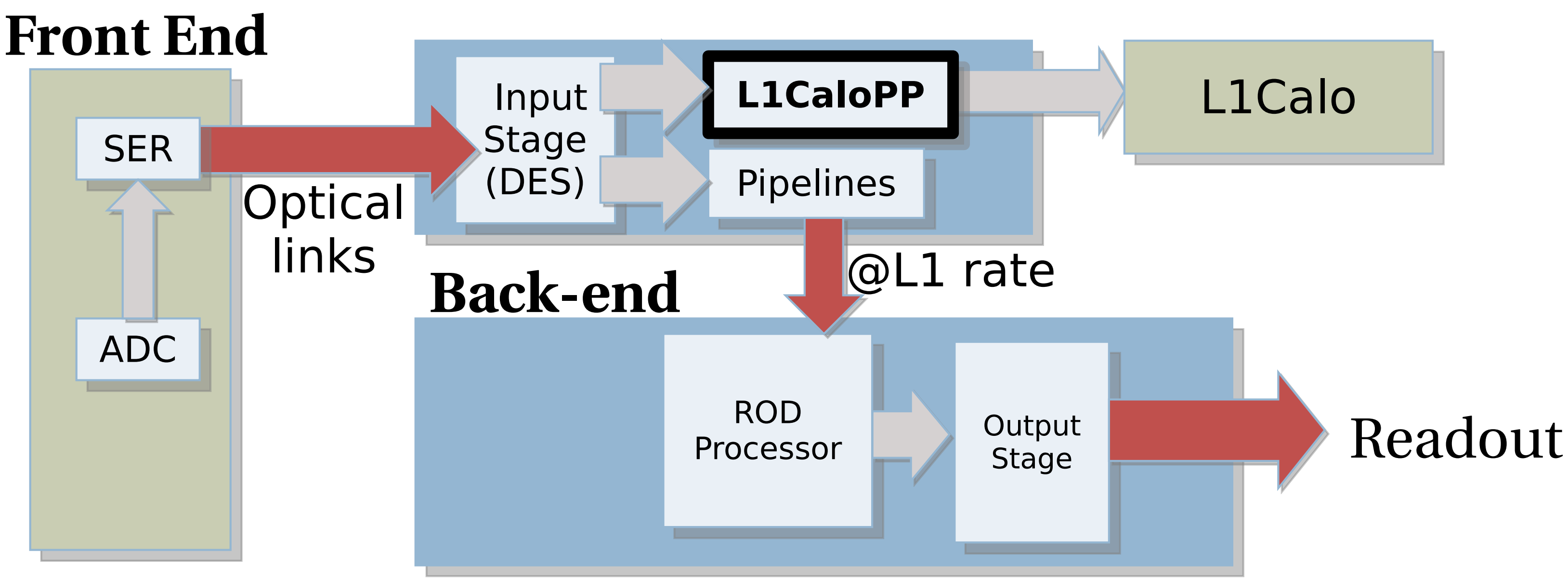
2a. PreProcessor next to ROD

- Larger paths to L1Calo. Larger fiber connections.
- Would need larger pipelines at ROD level (for ex. 6.4 us).
- Data processing concentrated in ROD allows multiple steps reconstruction.
- Further Tower processing in ROD Processor and inclusion in byte-stream.



2b. PreProcessor next to L1Calo

- Digitized data transmitted to L1Calo Preprocessor.
- Shorter paths to L1Calo.
- Pipelines next to L1Calo.
- Data transmission to ROD at L1 rate. ROD Upgrade?
- Tower processing in DAQ: Transmit them from PP to ROD. Further analysis in ROD before its inclusion in BS.



Monte Carlo Simulation

- New ideas and algorithms are not proven and needs checking with MC.
- Simulation with 60 and 400 event pileup and cavern background (validated) is **urgently** needed for studies
- Full simulation with high pile-up is **very** CPU intensive
  - Fully simulate signal events and min. bias events and mix them later
  - Simulate small no of events to develop/validate parameters to drive ATLFAST

Pile up - 1 event!

Pileup 30

(A. Abdesselam)

(hits from ~30 min_bias event are merged in a beam-crossing)

Pileup 50