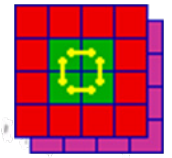


Report WP3: Trigger for sLHC

Terascale Workshop Aachen
Marius Groll
University of Mainz
27.11.2008

University of Heidelberg

JOHANNES GUTENBERG UNIVERSITÄT MAINZ University of Mainz

PHYSICS AT THE TERA SCALE
Helmholtz Alliance

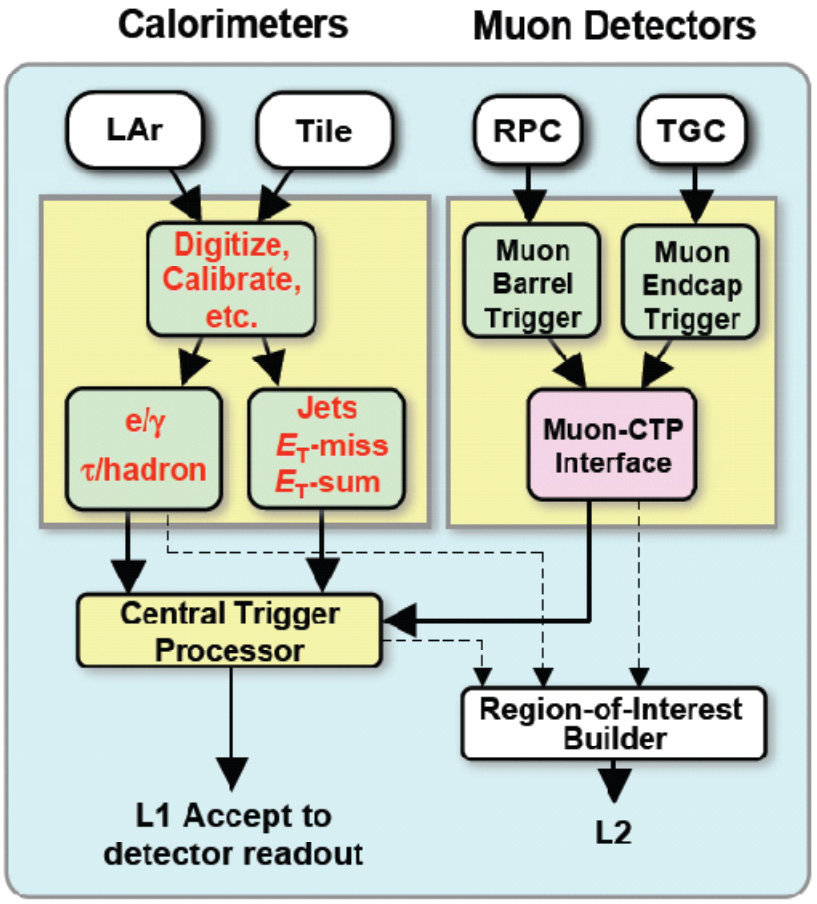
ATLAS Level-1 Trigger

WP3 proposal:

- "... cope with higher rates and adapt to new insights from the first years of LHC physics."
- Fast, integrated & configurable electronics

Level-1:

- **Fast custom electronics (ASICs & FPGA)**
  - ➔ synchronous
  - ➔ algorithms implemented in firmware
  - ➔ max. Latency: ***2,5 µs***
    - including transmission delays
- Calorimeter and Muon detectors
  - reduced granularity
- Input rate: ***40 MHz***
- Max. L1 accept rate: ***<100 kHz***



Trigger objects:

- ***High p_T electrons/photons, tau, muons, Jets, EtSum, Etmiss and EtJet***

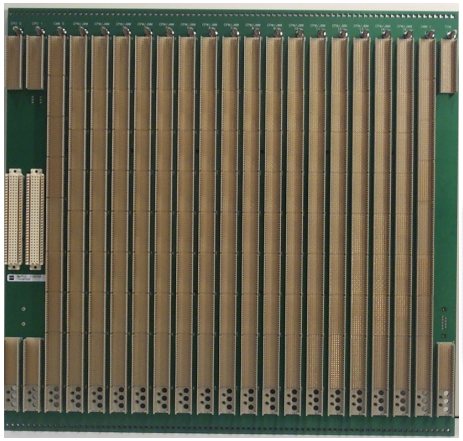
➔ ***handling high multiplicities and high-ET objects (beyond SM)***

➔ ***Higgs measurements – triggering on W/Z decays***

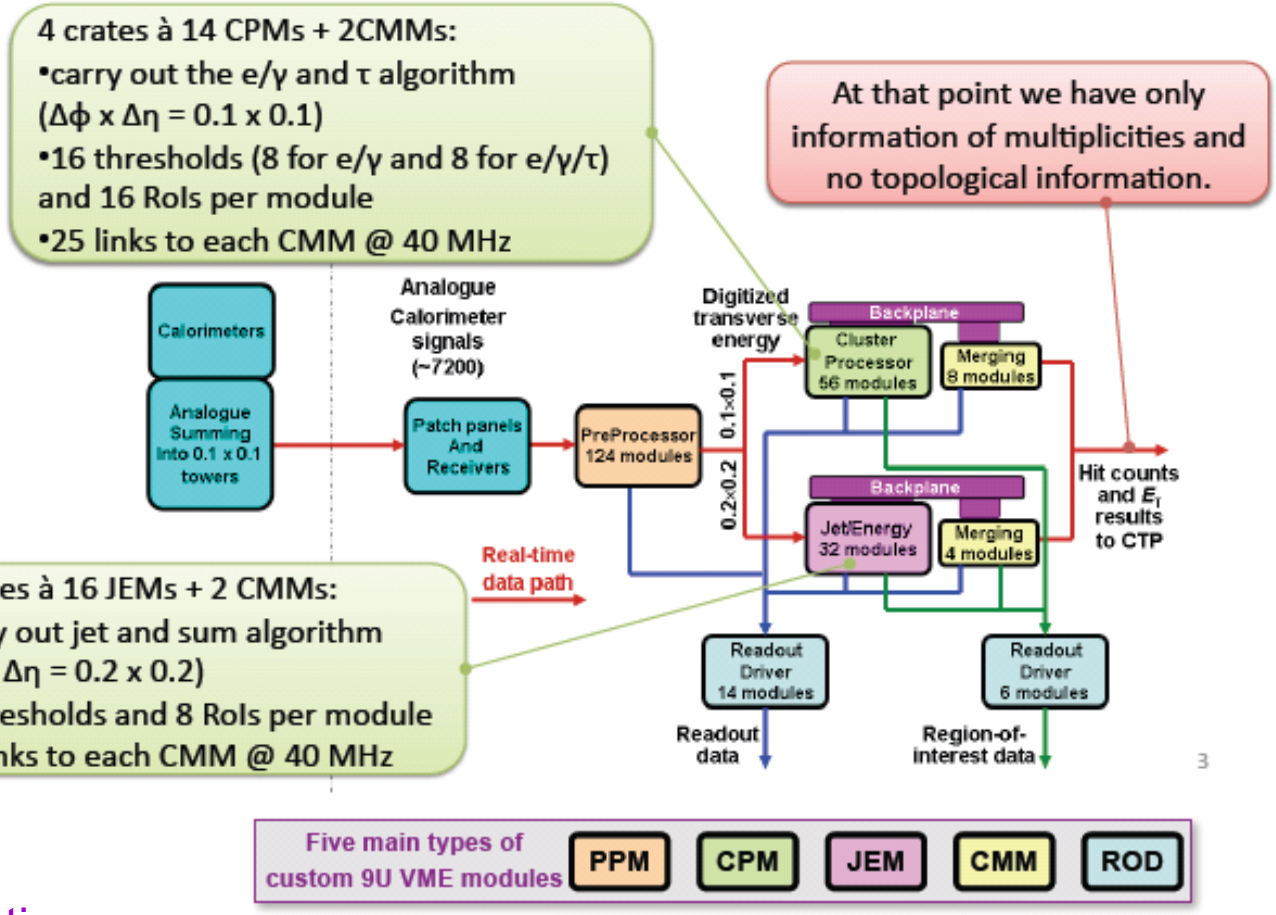
ATLAS L1Calo today

Major HW challenge: data movement

- Massive parallelism
➔ 300 GByte/s input
- Complex connectivity
➔ overlapping sliding window algorithm
➔ High-density backplane

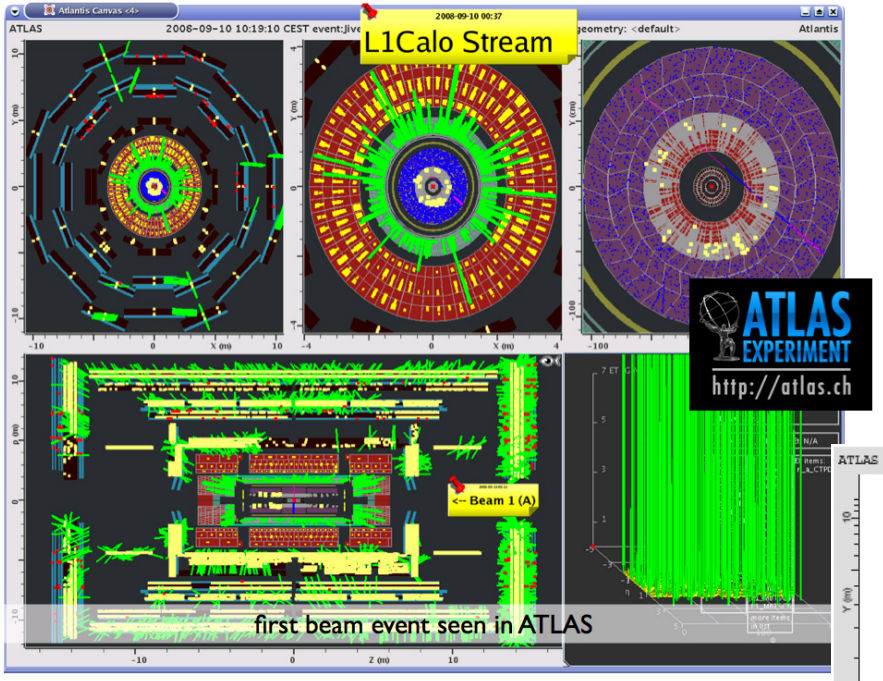


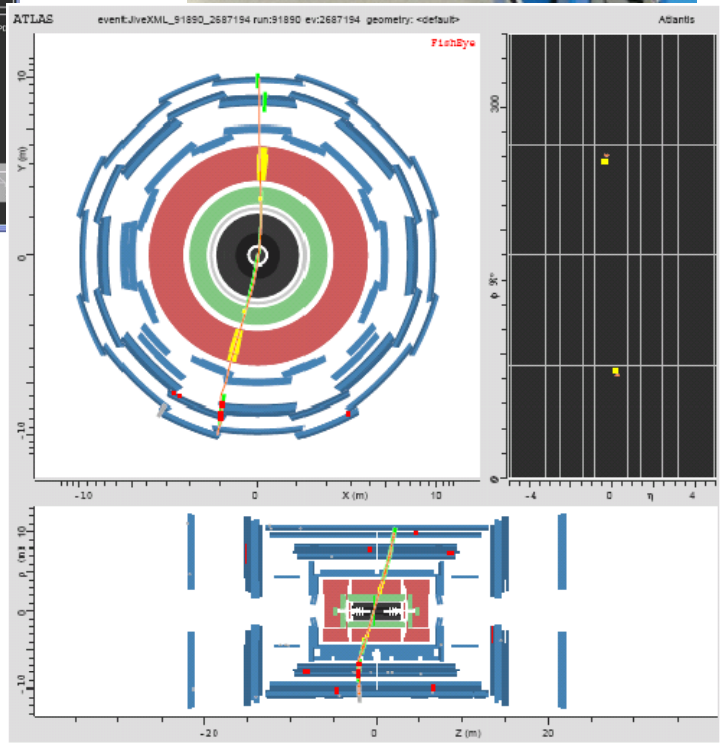
22000 pins



- 1 μs for decision / calculation
- CTP decision based on the ***multiplicities of (high) p_T objects and energy sums***

ATLAS L1Calo today





- L1Calo fully installed since 2007
- small amount of problems: problematic channels & calibration
- L1Calo is able to trigger on cosmics & beam splashes

Luminosity Upgrade

LHC: **Phase I / 2013:** 2-3 x 10^{34} / 40-60 interactions/BC / 6-8 months shutdown
Phase II / 2018: 10^{35} / ~300 interactions/BC / 12-18 months shutdown

Impact of increased lumi on the trigger:

- depending on: **bunch crossing frequency, number of p/bunch etc.**
- detector occupancy increases : 4-20 x (with the same granularity)
- Pile-up: up to ~400 interactions/BC **(50 ns bunchspacing and $10^{35}s^{-1}cm^{-2}$)**

➔ degradation of trigger algorithms (isolation, fake signals)
➔ increased trigger rates for fixed thresholds and efficiencies

Phase I:

- Level-1 output rate still < 100 kHz
- Acceptance should still be as high as possible
- Increase of trigger thresholds is not an option: electroweak triggers are needed

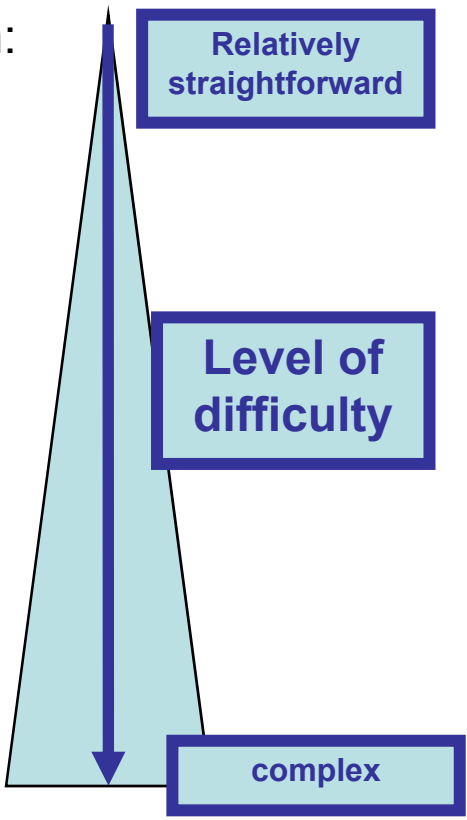
➔ compensation by **more granular data** and/or **refined algorithms** by using topological / ROI information

- improve electron ID against background and pileup
- multiplicities with more thresholds & topological information
- retain good BCID filter efficiency with more pileup

Topological trigger

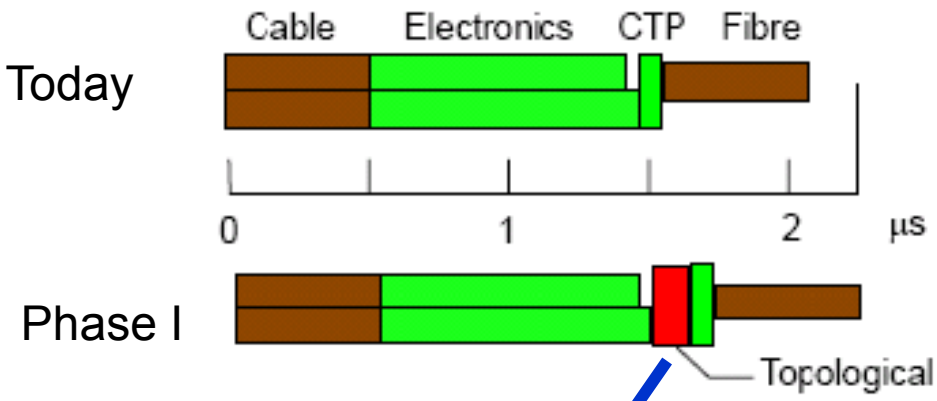
Possible selection criteria on L1 by using topological / RoI information on CTP level:

- **exclusive trigger** combinations beyond multiplicity combination: distinct separation between em and jets at different thresholds
- **Azimuthal "back-to-back" criteria**
  e.g. Selection of Higgs production
- **Forward-Backward correlation** in rapidity gap in η
  e.g. VBF processes
- definition of **isolated muons** by using calorimeter energy
- tagging of **b-jets** by soft muons
- calculation of **mass/transversal mass** of object pairs or even more objects
- **Etmiss correction** by using pT of muons, identification of jets directing to cracks or Etmiss



Phase I: Latency @ Level-1

Tune thresholds & algorithms

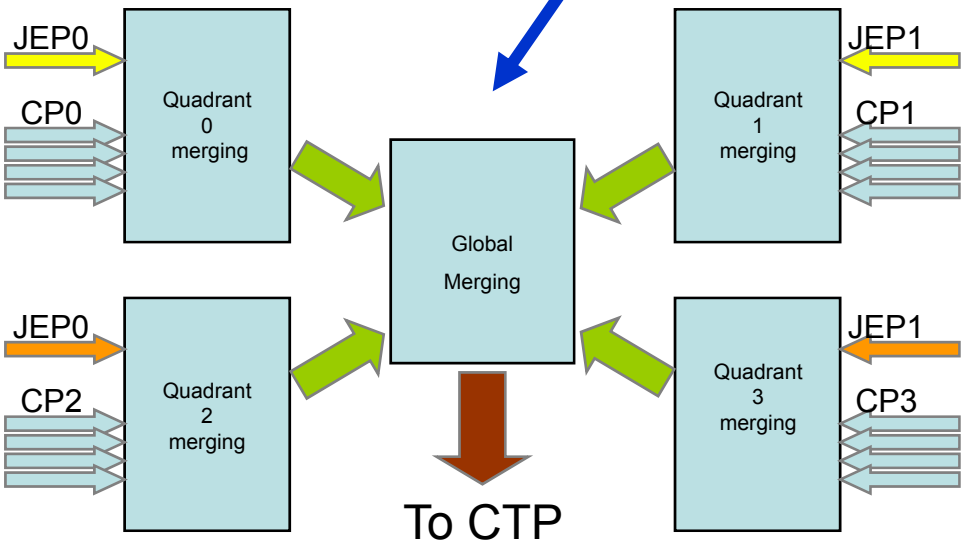


Max. L1 latency was defined as **2500 ns (100 BCs)**

- Muon trigger: max. 1493 ns
- Calorimeter trigger: max. 1465 ns
- CTP + TTC: max. 653 ns
- Total L1 latency: 2146 ns (86 BCs)

➔ ~350 ns (14 BCs) available up to design latency

➔ **Topological triggers & more thresholds?**



HW changes:

- Backplane has to transport more data
- CMM has to deal with topological information
  ➔ replacement
- New additional processor between L1Calo and CTP
  ➔ depends on the upgrade of CTP
  ➔ max. Topological Ansatz: perform correlation at CTP incl. Myon information
- High density data transfer between Merger and new Processor
  ➔ fast optical links Gbps

Topological trigger @ LVL1 - RoI

What additional data could we use?

Today: **50 bits/JEM** = 3 x 8 bits (ET, Ex, Ex)
+ 3 x 8 bits (Multiplicities / threshold)

Phase I: 8 RoIs per JEM, 2 location bits per RoI,
8 threshhold bits per RoI

➔ 8 x (2 + 8) bits = **80 bits for the RoIs per JEM**

• Maybe ET, Ex and Ey with better precision + 36 bits

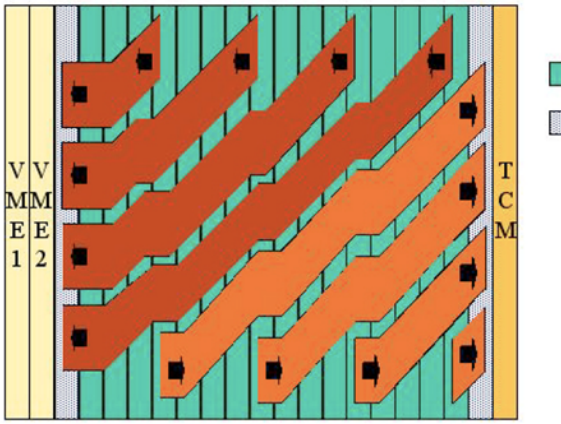


Figure 3: Conceptual layout of a merging layer of the PB (1 of 4). View from front of crate.

Total data per JEM:

➔ 116 bits have to be sent per JEM each 25 ns
With 50 links on the backplane to the CMMs
➔ data rate needed: 4 x 40 Mbps = 160 Mbps

50 bit @ 40 MHz ➔ 25 bit of jet data
100 bit @ 80 MHz ➔ 75 bit of jet data
200 bit @ 160 MHz ➔ 175 bit of jet data
400 bit @ 320 MHz ➔ 375 bit of jet data

➔ **new CMM is needed:** gather and transmit all crate-level data over high-speed optical links to a new global merger system
The global merger: current algorithms + topological triggers

Backplane rate test

Backplane rate test on the longest JEM data line to CMM

➔rate limit on the backplane ist about **160-320 Mb/s**

➔Detailed signal transmission test has to be done

- full crate setup with CPM and JEM
- correct signal termination for high rates
- **bit error rate test**

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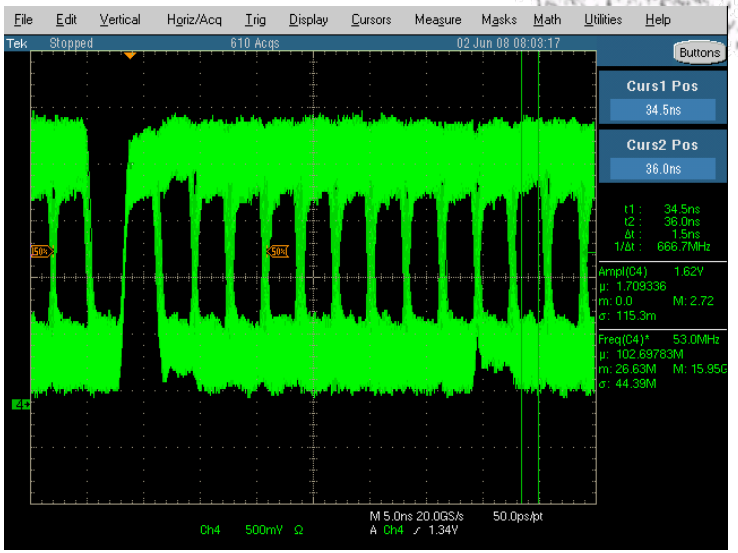
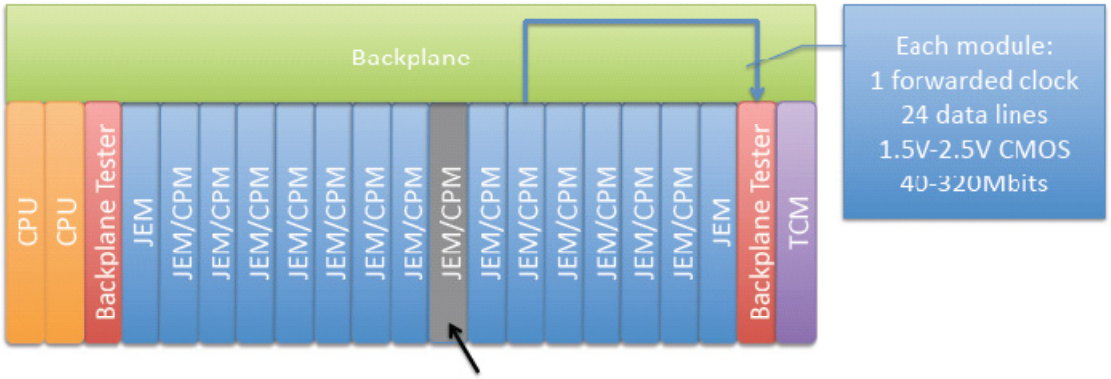


➔ Build backplane tester based on recent FPGA family providing both termination and time calibration for each line

- schematics ongoing
- will be build in 2-3 months
- test pattern sent by JEM/CPM
- FPGA compares received with expected signal
- bit errors are calculated and send by VME



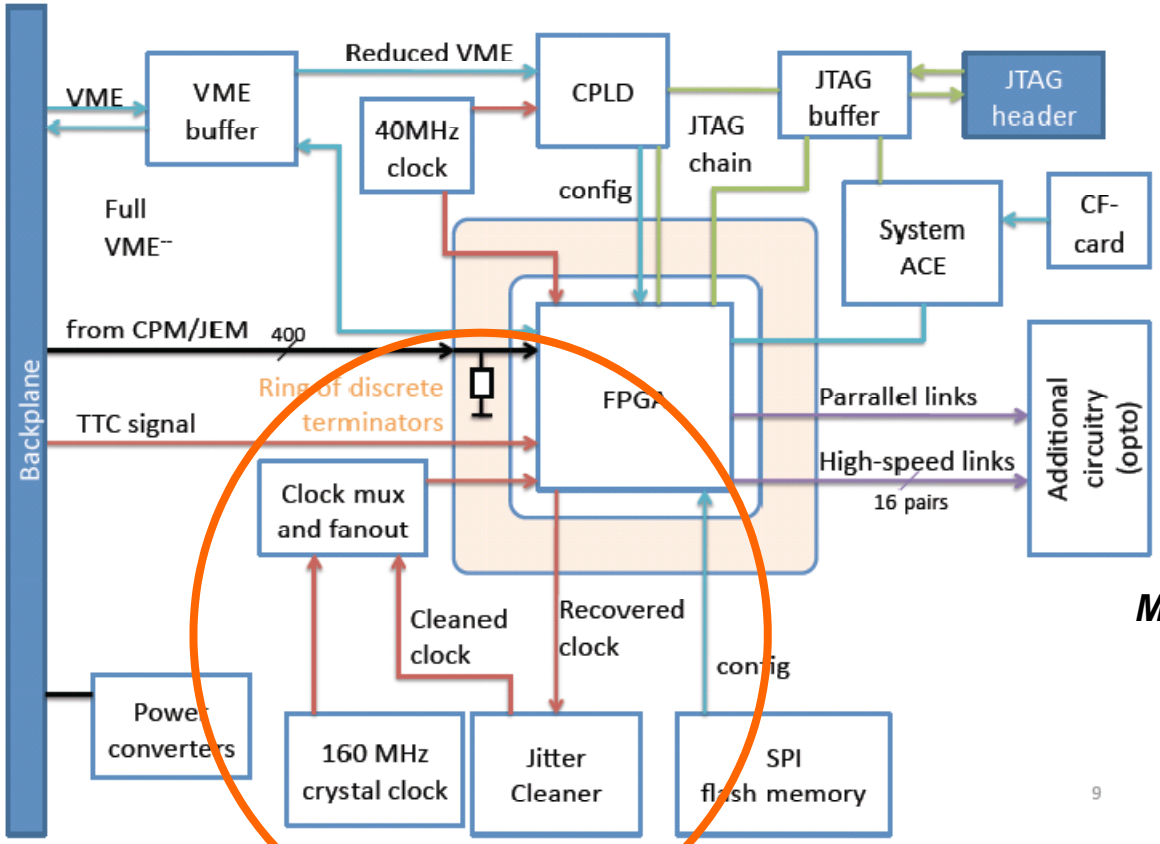
JEM/CPM can be placed in one crate ➔ in between one empty slot needed

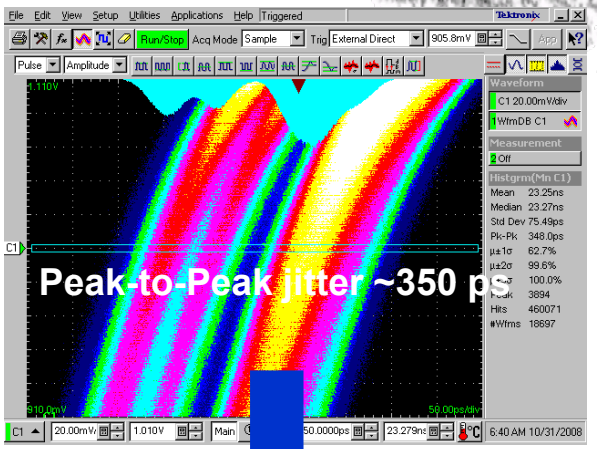
Backplane tester board

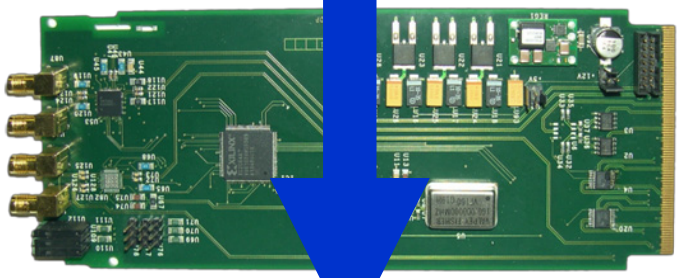
- **LHC / TTC** clock is not clean enough

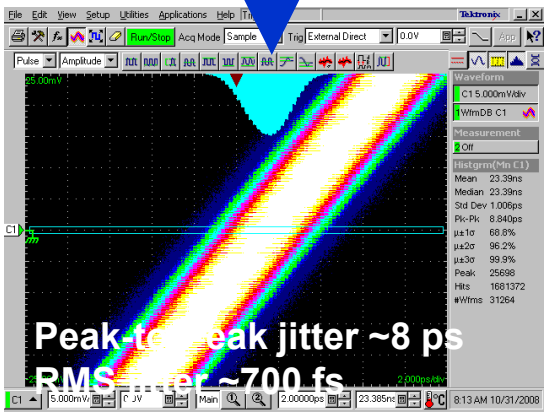
➔ **jitter cleaner needed**

➔ Tested already on stand-alone board









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➔ **Sufficient to run 6.5 Gbps**

Environment Assumptions for 10^{35} Phase II

- **New L1Calo system** with maybe different latency
- Level-1 depends on the **LHC Bunch crossing interval 25 or 50 ns**
- **Limit of L1A rate?**
  - events have greater detector occupancy so will be bigger and harder to analyze at LVL2, EF and offline
  - i.e. **faster transmission** & recording will be needed for the same L1A rate
- including **finer eta-phi segmentation** in the electromagnetic calorimeters for better electron selection, and multiple depth samples for shower profiling

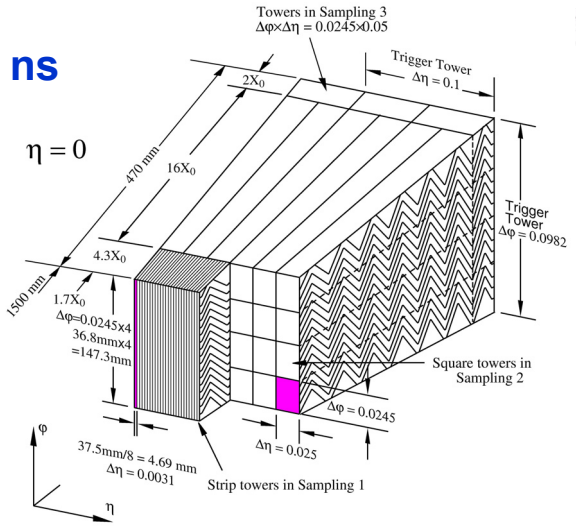
➔ digitisation combined in new **Calorimeter FEE**

➔ digital / **optical fibre** connection

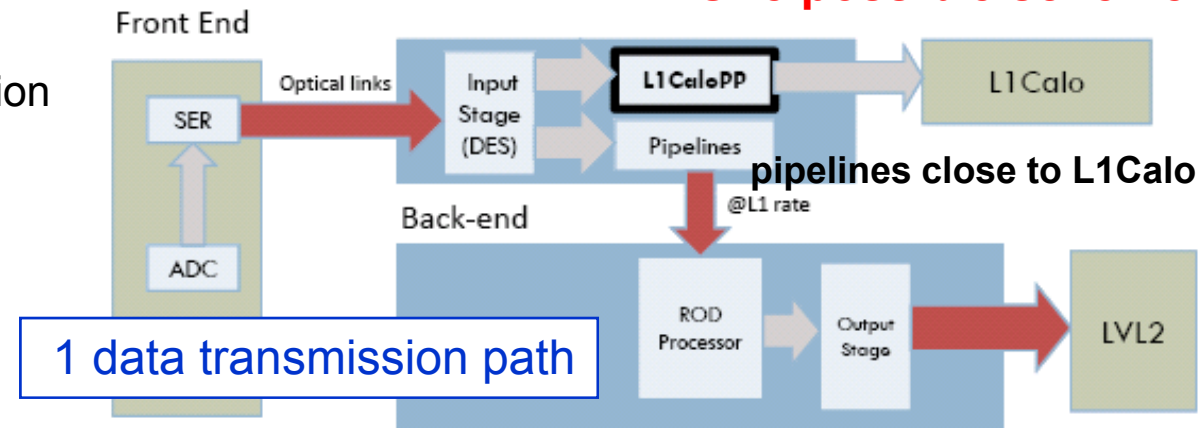
➔ Optimal Granularity / **TT size**

➔ Evaluate the implementation of algorithms at **BC latency**

More details by Andrei Khomich



One possible scheme

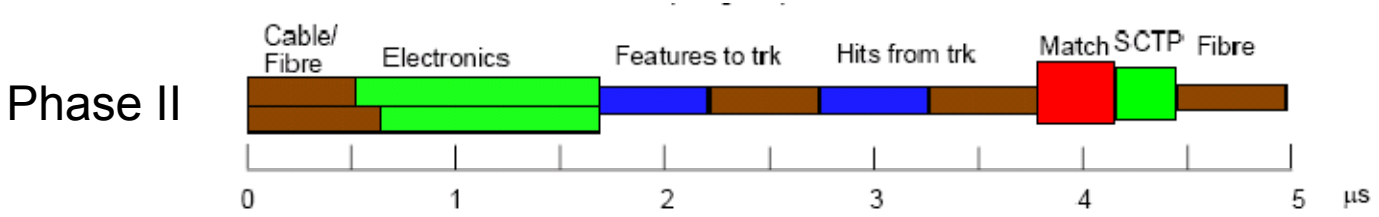


no latency advantage in case of track trigger

Phase II

- **Improved timing distribution system** – better link stability – separated from other signals to be distributed (trig type, resets…)
- **SCTP capable of processing Features:** correlation between the calorimeter, muon, and possibly a tracking trigger (rejects π^0) is being discussed

Latency and L1 Track Trigger:



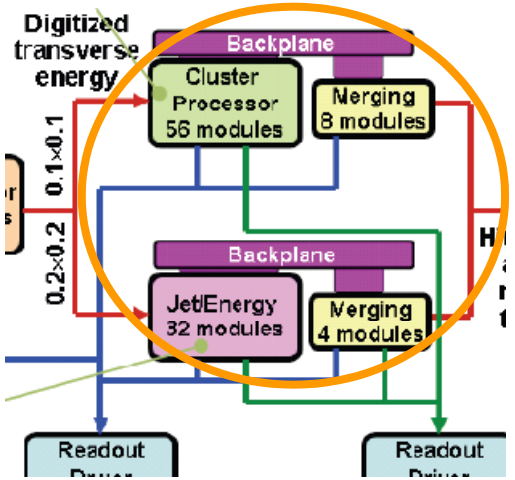
L1 track trigger could be seeded by "L0A" (Calo,Muon) features at ~1.5 - 2 μs

- Input signal changes require changes in the processors (JEP/CP)

➔ **merge both processor module to one JCM**

- **perform CP & JEM tasks in one Module or use the same Module with different Firmware**

➔ **active R&D**



JCM

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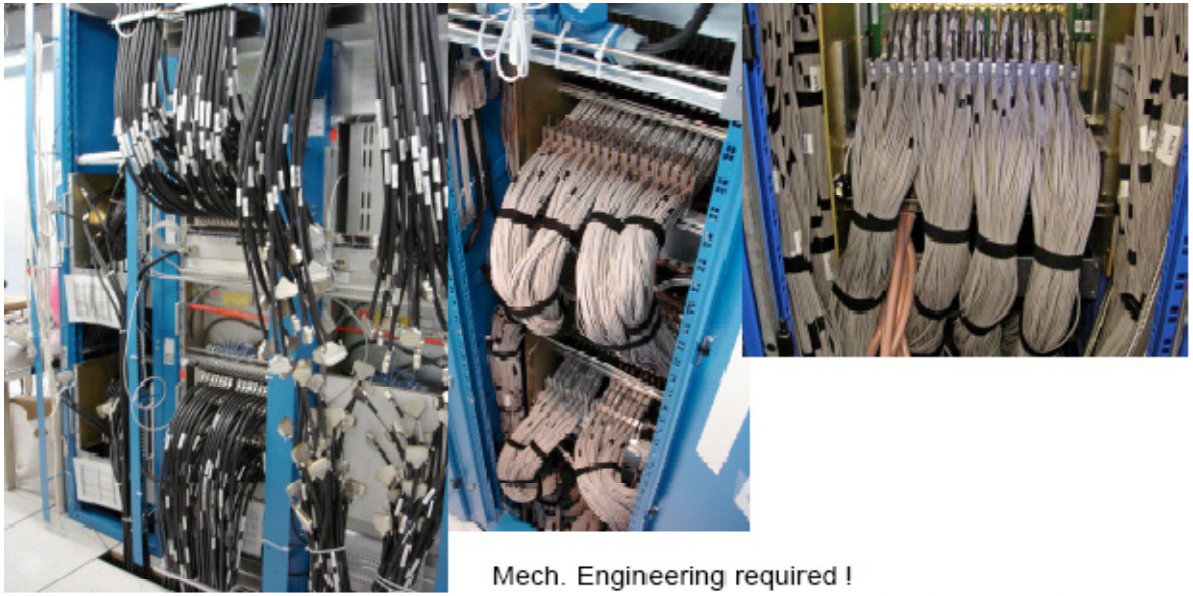
Transmission Technology

Optical transmission for higher density



Mech. Engineering required !
This is **THE LIMIT** for cable-installation density on **Input / Output** (at least electrically) !

Study possible link technologies:

- TileCal raw DAQ data rate from the drawer would be about 46 Gb/s plus slow Control
- using state-of-the-art optical transceivers (SNAP 12: 120 GBps)

- **Phase I:**

JEP/CP with 160 MHz
➔ 64/124 Gb/s

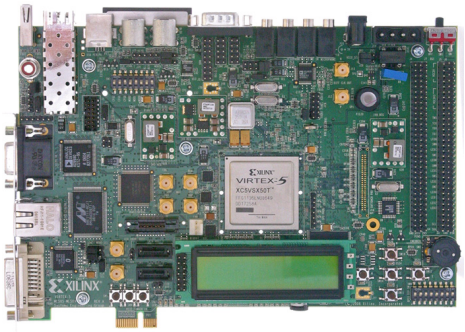
on-detector digitisation allows to go to optical transmission:

- optical fibres
- larger bandwidh
- immune to crosstalk & ground loops
- Multiplex of many channels / less cables
- converters needed

➔ check influence on latency & costs

Phase II: R&D topics

- Need to establish Algorithms and Architecture
  - Strong need for Monte Carlo studies
- Need details of Environment
  - Need for dialogue with Calorimeters, CTP, DAQ and HLT, TTC groups
- Initial Technology R&D:
  - High-speed backplanes (e.g. connectors to run to n x 10^8 Hz) & links
  - PCB technologies – learning
    - e.g. Advanced Telecom Computer Architecture standard, µATCA
    - Design / manufacturing rules for very fast boards
  - new crate communication systems to replace the VME protocol
    - µATCA provide higher data transmission
  - Low-jitter clocking; built-in high-speed instrumentation
  - Investigate capabilities of new FPGAs
    - more logical units, more inputs...
    - Communication to new buses with broad bandwidth
- Overall cost, effort, complexity ~present L1Calo



Summary

- **WP3 defines a challenging effort for the trigger upgrade**
- **Make existing L1Calo system work** – to learn as much as possible for the optimisation of algorithms and the system
- **Phase I:** Upgrade to the Processor system to allow topological trigger
- **Phase II:** New system is needed to deal with the new environment
- Timescale of developments: **tight**
- Need some **TDAQ organisation** to bring LVL1, HLT, CTP & Timing upgrades together
- **Monte Carlo studies** are needed and essential to provide justification inside ATLAS and for funding
- **HGF contribution**:
  - Andrei Khomich / HGF Fellow in HD
  - Kim Temming / HGF PhD in Mz (start in dec. 2008)

  infrastructure improvement: signal analyser in Mz