# Low-Noise Amplifier Probe

UCSC/SCIPP

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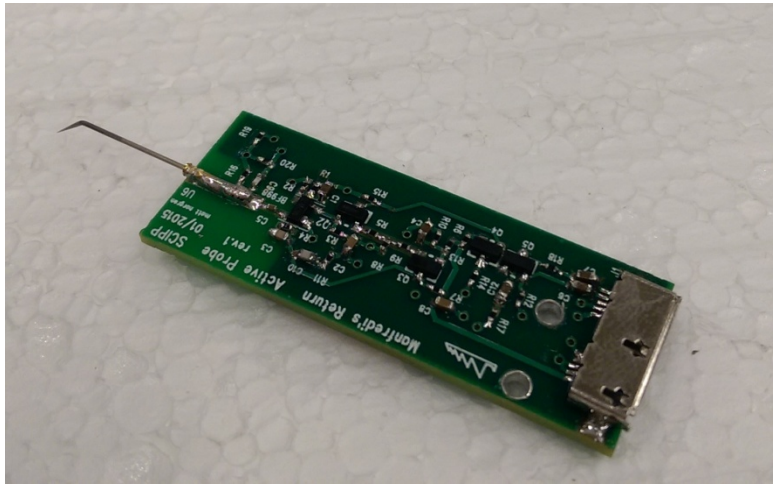
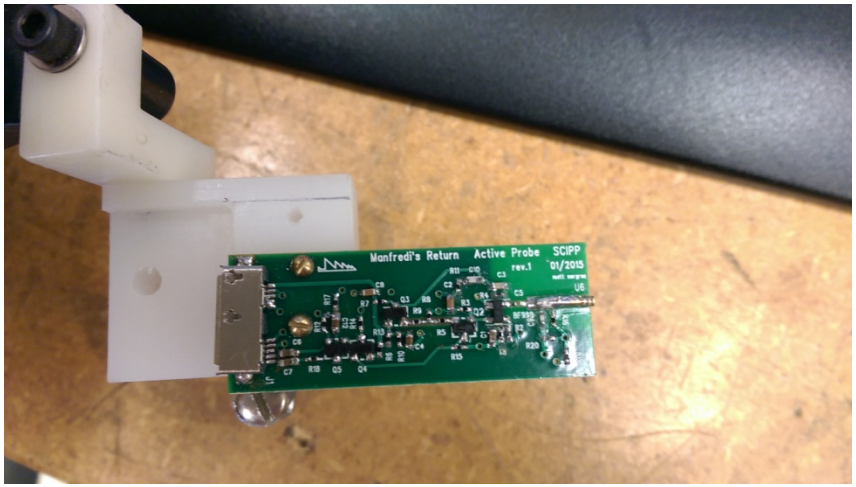
# Motivation and Goals

- Develop an amplifier that can be used to measure signals from the passive pixel arrays of the CHESS1 chip.
- Detect signals as small as 1/3fC
- Shaping time around 20ns
- Easy to use.

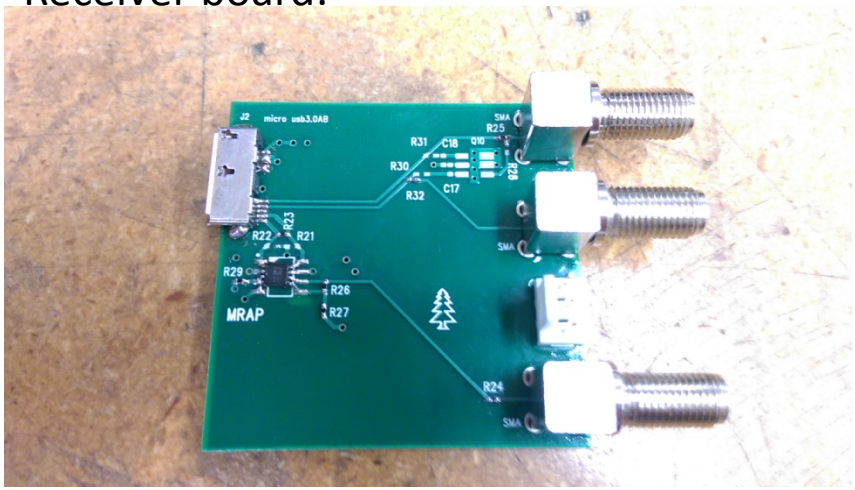


# Active Probe Board

Probe board:

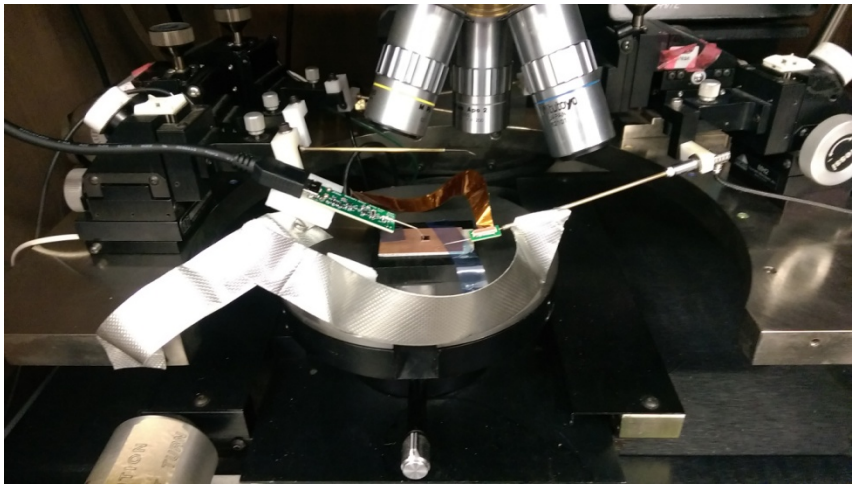


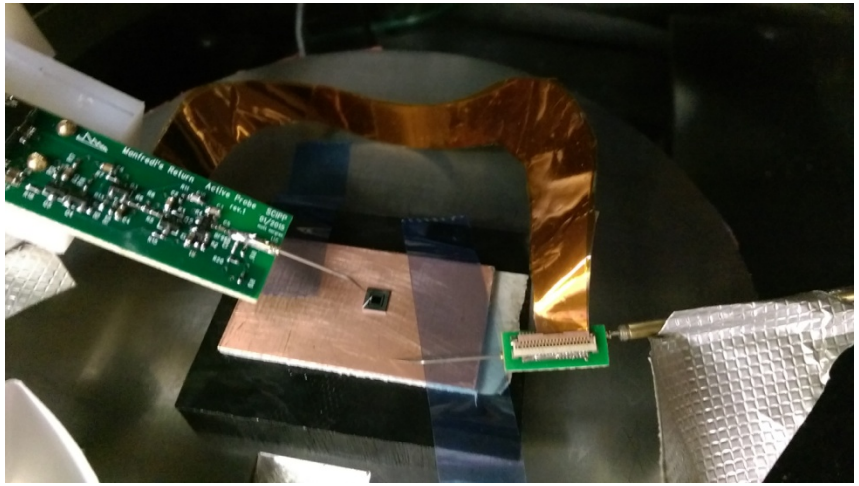

Receiver board:




- Dual-gate mosfet first stage, with second stage differential output.
- AC coupled input.
- Socket mount for probe tip.
- Board dimensions - ¾’’x 1¾’’
- Board mounts to micropositioner.
- USB3.0 data cable supplies all necessary IO to probe board.
- Receiver board contains interfacing for calibration signals and power. Converts differential signal to single ended.
- Custom PCBs designed at UCSC.
- Manufactured as single PCB, which is cut into probe, receiver, and HV supply board.
- PCB manufacturing $70 + parts cost $30-50 = $100-120 USD total cost.

# ATLAS07 sensor test

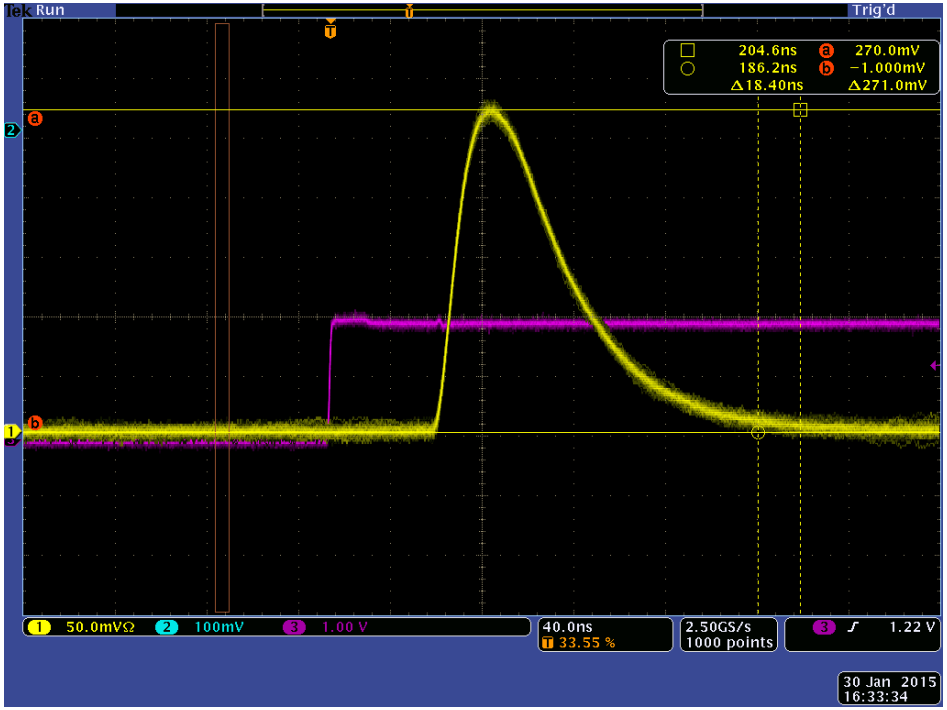




- Test chip - ATLAS07-P-SSD-Series2
- 2.5pF load at -300V substrate bias.
- HV bias is supplied through second probe tip, which is held by the HV supply board.
- Kapton ribbon provides small signal path.
- Shielding tape provides ground return for HV source.
- Geometry and grounding configuration of small signal loop, back plate holding die, and other metal in probing station greatly influence EMI and noise performance. Proper ground referencing of possible EMI sources is necessary for good function of the probe.

# ATLAS07 sensor test

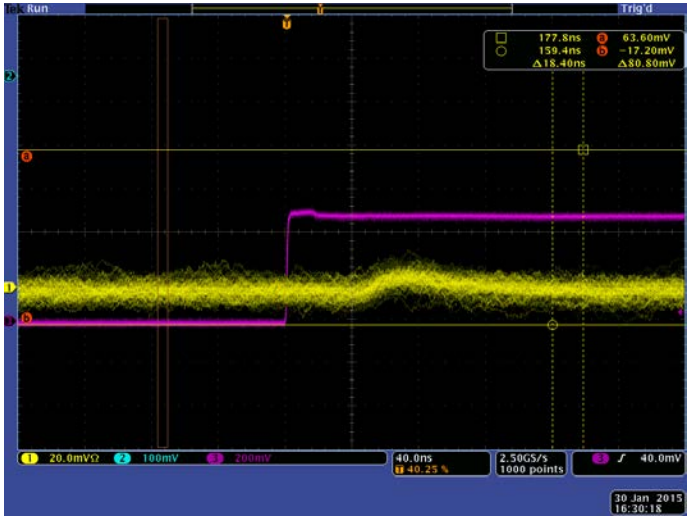
10fC input to front end




- Rise time: ~25ns
- Gain: 27.464 – 29.149mV/fC
- Noise: 0.076-0.099 fC – referred to input.
- With no load on amplifier input, noise is ~0.05fC.

# ATLAS07 sensor test

0.25 fC input to front end





- Briefly tested on very small calibration signals of 0.25fC.
- Amplifier gain appears to be linear response to input charge.
- Uncertainty in gain and noise values stem from measurement uncertainty and issue with an amplitude step of the calibration signal (this step is unrelated to the board).

# Next Steps

- Still in the early stages of testing the amplifier.
- Next step is to test the passive pixel arrays of the CHESS1 chip.
- Increasing the biasing to the first transistor may enhance performance – easily done by adjusting resistor values.
- Setup could be optimized to possibly further reduce noise – shorter probe tip, shorter HV and HV ground return loop.
- Detailed documentation of setup and use requirements will be available shortly.