**Project Specification**

**Project Name: CHESS-2**

**Test Chip: CMOS (HV/HR) Evaluation for Strip Sensors-2**

**Version: V 0.3**

***Abstract***

This document lists the target specifications for the test chip, which will be fabricated and tested in order to investigate the read-out architecture options of HV/HR-CMOS technologies for use as a silicon strip sensor. This submission follows the CHESS-1 submission. Two representative foundries will be used.

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| --- | --- | --- | --- |
| ***Revision History*** | | | |
| ***Rev. No.*** | ***Date*** | ***Pages*** | ***Description of Changes*** |
| 0.1 | 2015/01/19 |  | Initial draft |
| 0.2 | 2015/01/29 |  | Added the CMOS pixel performance section. Some formatting and turn on Changes Tracking. |
| 0.3 |  |  | Formatting, wording improvements |

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# SCOPE

This document lists the target specifications for the test chip, which will be fabricated and tested in order to investigate the read-out architecture options of HV/HR-CMOS technologies for use as a silicon strip sensor in place of the traditional planar silicon strip sensors. This submission follows the CHESS-1 submission. Contrary to the HV-CHESS1 submission, which was a multi-project run, this second chip will be manufactured as an engineering run. This allows to be able to pick the substrate resistivity anywhere between 20 to 1000Ω\*cm[[1]](#footnote-1). For HV CMOS the reticle will be divided in three independent sub-regions:

* The first part dedicated to HV-CHESS-2 itself.
* The second part dedicated to SLAC designs for ILC and/or photon science.
* The third part to an RD50 project.

The complete size of the die and of each part is described in Table 1‑a

Table 1‑a Size and allocation on the reticle.

|  |  |  |
| --- | --- | --- |
|  | Width | Height |
| Size of the die | 2.5cm | 2cm |
| Size allocated for CHESS2 | 2.5cm | 0.67cm[[2]](#footnote-2) |
| Size allocated for the SLAC project | 2.5cm | 0.66cm |
| Size allocated for the RD50 project | 2.5cm | 0.66cm |

The rest of this document will only describes and refer to the CHESS part of the reticle. All three parts will be designed independently and placed in such way that they can be cleaved from each other and tested separately.

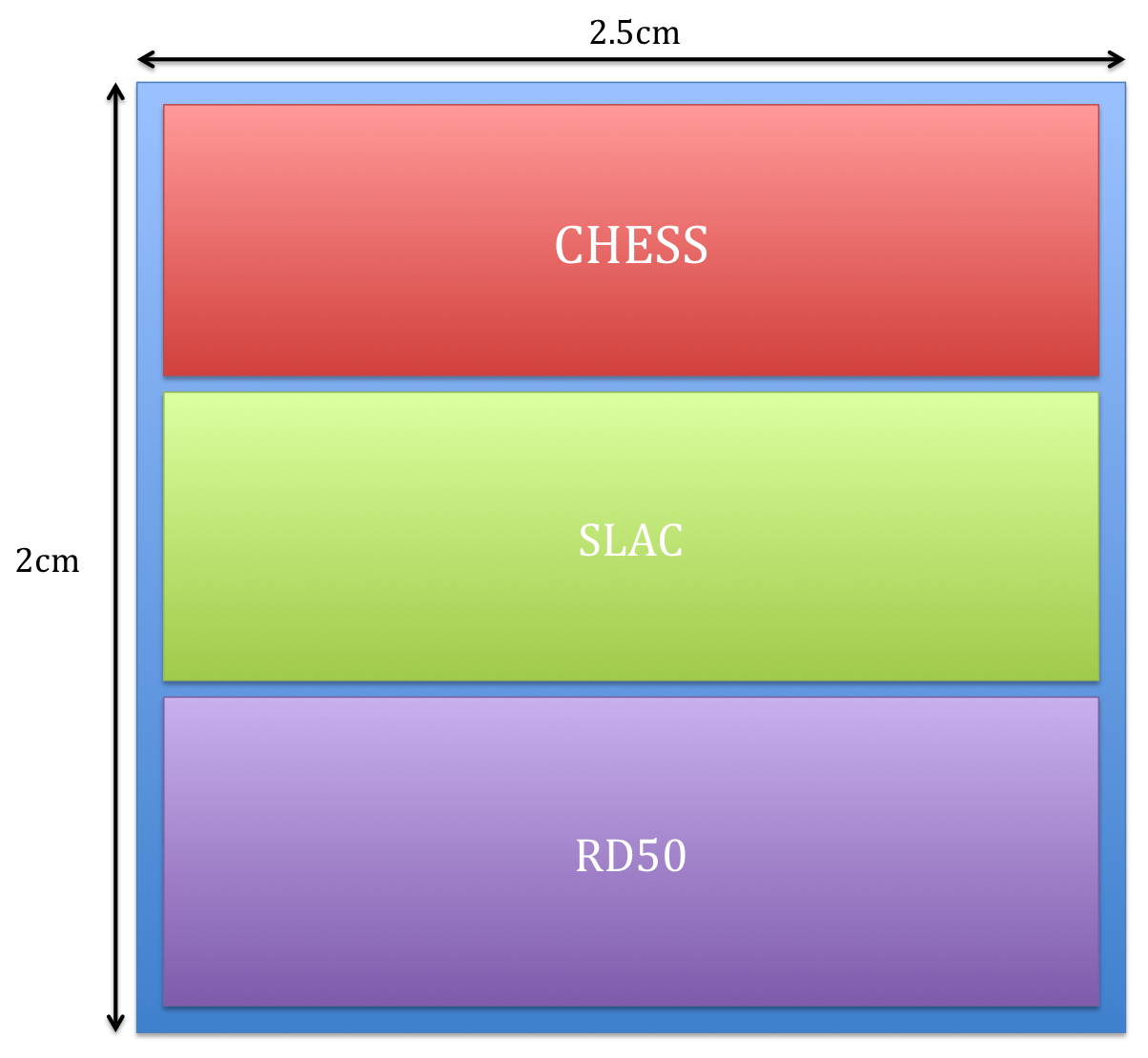


Figure 1–1 Layout of the 3 different ASICS in the reticle

# Foundries

Two foundries will be targeted at this time based upon the current understanding of the available technologies and their appropriateness for strip sensors. The two technologies are Tower-Jazz TJ180 and Austria Micro Systems AMS-H35.

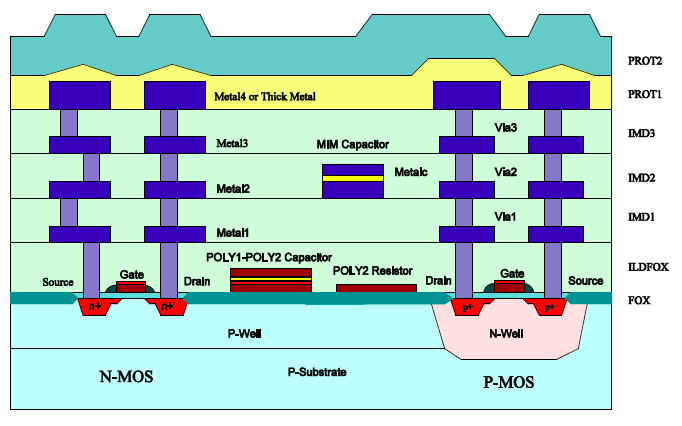


Figure 2–1 Wafer cross-section of the AMS-H35 process

# Physics case

The full strip detector is to be installed in replacement of the present ATLAS strip detector after the LHC upgrade for higher luminosity. The upgrade of the detector is necessary because the present detector will have reached the end of its lifetime due to radiation damage and to cope with the higher number of interaction per bunch crossing and therefore higher number of tracks in the strip detector. The HV-CMOS technology is being investigated as a possible alternative to the more conventional silicon planar strip sensor, which is the baseline technology for the strip detector replacement.

## Occupancy numbers

The occupancy of this strip detector is calculated from GEANT4 simulation of the strip detector.

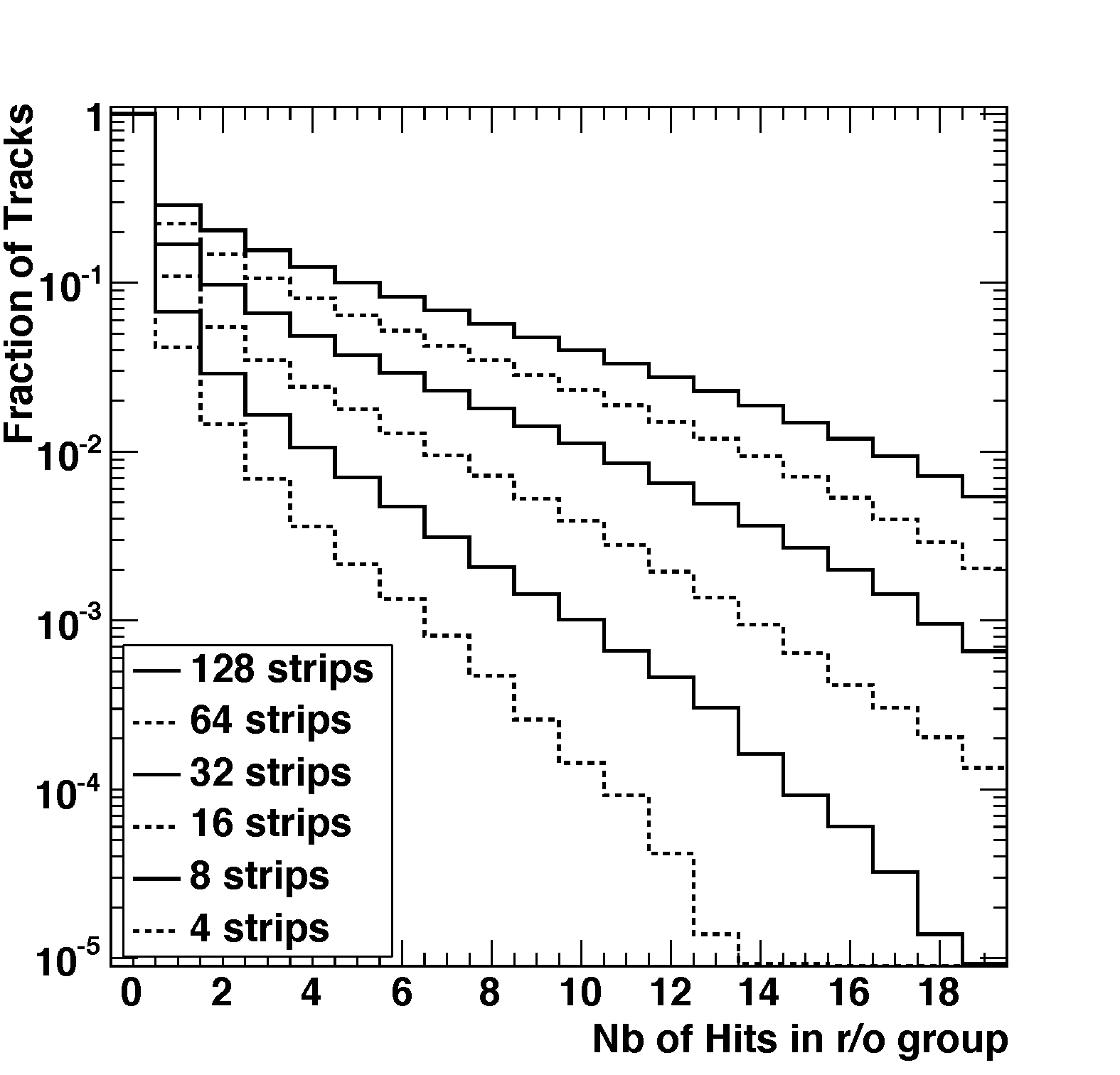


Figure 3–1 Fraction of tracks seen in the layer 1 of the strip detector in the case of h -> bb with Higgs pT > 200GeV and b jet pT > 150GeV.

## Hit retention in the strip detector

In order to cope with the occupancy numbers for HL-LHC the number of hits that will be read out per strip and per reticule is specified in Table 3‑b.

Table 3‑b Specifications of number of hits in CHESS-2

|  |  |
| --- | --- |
|  | Specifications |
| Number of hits per strip | 1+ flag |
| Maximum number of hits per 128 strips | 8 |
| Format of the data output | 5bits + 1bit + 7bits |

# Detector performances

The performance of the pixel arrays in CHESS2 chip has been measured in the previous submission (CHESS1 chip). In this section, the measured capacitances of the pixels are shown, and the expected signal to noise ratio of the different pixels for a MIP signal are also listed.

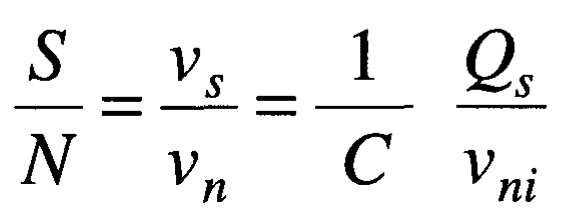
The measured capacitances of the single pixel in CHESS 1 chip are shown in Table 4-a.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Array name | Size | Diode area fraction | Cap. (fF) @ 60V | | Cap. (fF) @120V |
|  |  |  | **Measured** | **Simulated** | **Measured** |
| A1 | 45x100 µm | 30% | 86.8 | 62.9 | 51.9 |
| A2 | 45x100 µm | 50.4% | 94.5 | 62.9 | 65.8 |
| A3 | 45x200 µm | 30% | 87.5 | 117 | 59 |
| A4 | 45x200 µm | 50.4% | 123 | 117 | 88.1 |
| A5 | 45x400 µm | 30% | 128 | 227 | 107 |
| A6 | 45x400 µm | 50.4% | 240 | 227 | 129 |
| A7 | 45x800 µm | 30% | 244 | 445 | 195 |
| A8 | 45x800 µm | 50.4% | 349 | 445 | 251 |
| A10 | 45x200 µm | 30% | 93 | 117 | 58.8 |
| A11 | 45x200 µm | 30% | 121 | 117 | 92.0 |
| A12 | 45x200 µm | 30% | 88.3 | 117 | 76.2 |

Table 4-a : Measured capacitance of passive pixel array in CHESS1 chip {Might be good to add a comment column to specify how A10-A12 are different from A3.}

The expected signal to noise ratio of a single CMOS pixel for a MIP signal can be calculated using Equation 1, where Qs is the collected charge in a CMOS pixel from a MIP signal , and C is the capacitance of the CMOS pixel, and vni is the input noise to the amplifier.

Equation 1 The expected signal to noise ratio can be calculated from the the capacitance of the CMOS pixel, the input noise to the amplifier, and the collected charge from a MIP signal in a CMOS pixel.



The Qs has been measured from the Ljubljana group as shown in Figure 4-a. Collected charge from a MIP signal can come from drifting or diffusion. As shown in the Figure 4-a blue solid curve. one can collect about 1000 electrons even when there is no bias voltage on CMOS sensor. This contribution is mainly from diffusion. The Drifting contribution proportional to the bias voltage. We measure Qs=1500 electrons at bias voltage, V\_bias=120V and Qs=720 electrons at V\_bias=60V.

To estimate the upper limit of input noise vni Figure 4-b shows the waveform of a typical event of MIP signal injection after amplification. The output noise measured to be x.xxmV. . Assuming input noise should be less than output noise for an amplifier, we get vni =x.xxmV.

Based on Equation 1, we compute the expected signal to noise ratio (S/N) of the CMOS pixel for a MIP signal and report it in Table 4-b. The S/N are also calculated for different substrate resistance (R\_sub) and for different V\_bias. The MIP signal amplitude is expected to be proportional to sqrt(R\_sub).

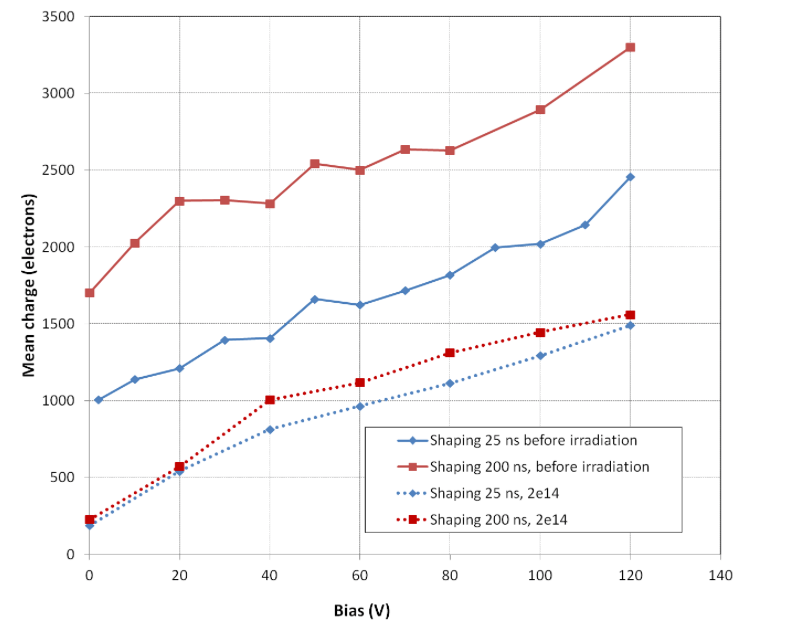


Figure 4-a : Measured collected charge as a function of bias voltage from Ljubljana group.

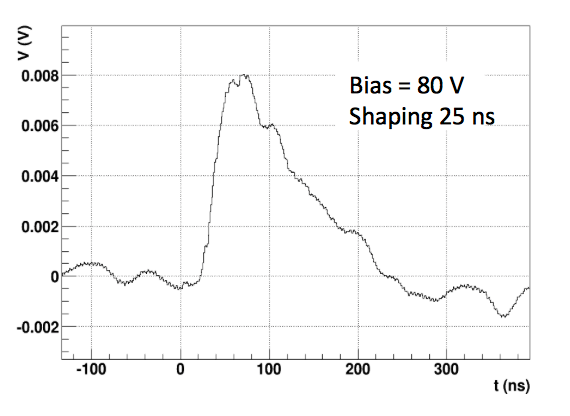


Figure 4-b : Measured signal waveform after amplifier and shaper (from Ljubljana group).

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Array name | Size(µm) | Diode fraction | S/N  @60V | S/N  @120V | S/N  @60V | S/N  @120V |
|  |  |  | **Sub=10 Ohm** | | **Sub =100 Ohm** | |
| A1 | 45x100 | 30% | 3.3 | 11.5 | 10.4 | 36.4 |
| A2 | 45x100 | 50.4% | 3.0 | 9.1 | 9.5 | 28.7 |
| A3 | 45x200 | 30% | 3.3 | 10.2 | 10.4 | 32.2 |
| A4 | 45x200 | 50.4% | 2.3 | 6.8 | 7.3 | 21.4 |
| A5 | 45x400 | 30% | 2.3 | 5.6 | 7.3 | 17.7 |
| A6 | 45x400 | 50.4% | 1.2 | 4.6 | 3.8 | 14.5 |
| A7 | 45x800 | 30% | 1.2 | 3.1 | 3.8 | 9.8 |
| A8 | 45x800 | 50.4% | 0.83 | 2.4 | 2.6 | 7.6 |
| A10 | 45x200 | 30% | 3.1 | 10.2 | 9.8 | 32.2 |
| A11 | 45x200 | 30% | 2.4 | 6.5 | 7.6 | 20.5 |
| A12 | 45x200 | 30% | 3.3 | 7.9 | 10.4 | 24.9 |

Table 4-b : expected signal to noise ratio from CMOS pixel for MIP signal before amplifier.

# Architecture of the chip

Due to the limited space available on the reticle and to minimize the design effort, the CHESS-2 chip is designed to be a demonstrator of a subset of a full strip sensor, which will comprise only 127 strips.

The specifications of a full sensor and the CHESS-2 are described in Table 5‑c

Table 5‑c Specification of the strip sensor and the CHESS-2 chip

|  |  |  |
| --- | --- | --- |
|  | Strip sensor | CHESS-2 |
| Number of strips | 512 | 127[[3]](#footnote-3) |
| Strip pitch | 40µm | 40µm |
| Strip length | 2.5cm - periphery | 2.5cm - periphery |
| Number of segments per strip | 32 | 32 |
| Size of the active sensor area | 2x2.5cm | 0.5x2.5cm |

In order to readout and process the hits coming from the strips some space is required at the periphery of the strips to include readout logic and output drivers. Therefore, the total length of a strip will be slightly less than 2.5cm to accommodate this additional space, see 5.1.

## Top level layout of CHESS2

The top-level layout of CHESS2 can be seen on Figure 5–1.

Strips

Strips

Strip encoding

Hit encoding

SPI interface

LVDS interface

Masking, Threshold

and Calibration

Figure 5–1 Layout blocks of CHESS2

The chip is made of 6 major blocks, which are described in details in the sections below.

It comprises:

* A strip array. It is the active part of the sensor housing 127 strips
* The strip encoding. It is meant to encode the position of the hit for each strip.
* The hit encoding. It is meant to encode the position of the 8 selected hits within the 127 strips.
* LVDS interface. It is meant to send the data out of the chip synchronized with the readout chip/FPGA.
* SPI (Serial Programming Interface). It is meant to do all the slow control and register programming of the chip.
* Masking, threshold tuning and calibration. Programmable memory block for each pixel to tune the threshold, mask hot pixels and enable calibrating signals.

### Global specifications of the chip

The global specification of the chip, derived from the physics case and geometrical constraint of the reticle are summarized on Table 5‑d.

Table 5‑d Global CHESS2 specifications

|  |  |
| --- | --- |
|  | Specifications |
| Size of the chip | 0.6cm x 2.5cm |
| Pixel size | 40µm x ~800µm |
| Number of strips | 127 |
| Number of pixels per strip | 32 |
| Readout speed | 320MHz |
| Output buffers | LVDS with tunable signal amplitude |
| Maximum number of hit per strip | 1 + overflow flag |
| Maximum number of hits in strip array | 8 |
| Size of data output | 13 bits |
| Latency | Fixed latency |

## Strip array

The strip array of CHESS2 will be made of 127 strips. Each strip is subdivided in 32 segments. The size of the segments will be adjusted to the available space across 2cm.

This strip array is subdivided in two groups; the first group, Group 1, of strips contains pixels without an internal discriminator while the second group, Group 2, will contain a discriminator in each pixel. The discriminators for Group 1 pixels will be located on the periphery. Groups are shown on **Error! Reference source not found.**.

The goal of having these two types of pixels in to investigate the noise increase in the pixel due to the presence of active digital circuitry and the amount of cross-talk with analog signals sent to the periphery.

Table 5‑e Subvision of the pixels array in two groups

|  |  |  |
| --- | --- | --- |
|  | Group 1 | Group2 |
| Pixels internal circuitry | Active amplifier | Active amplifier + discriminator |
| Number of strips | 64 | 63 |
| Localization | Strips 1 to 64 | Strips 65 to 127 |

The subdivision is made such as:

* Each strip of Group 1 will output an analog signal from each of the 32 amplifier outputs of its pixels.
* Each strip of Group 2 will output a digital signal from each of the 32 discriminator outputs of its pixels.

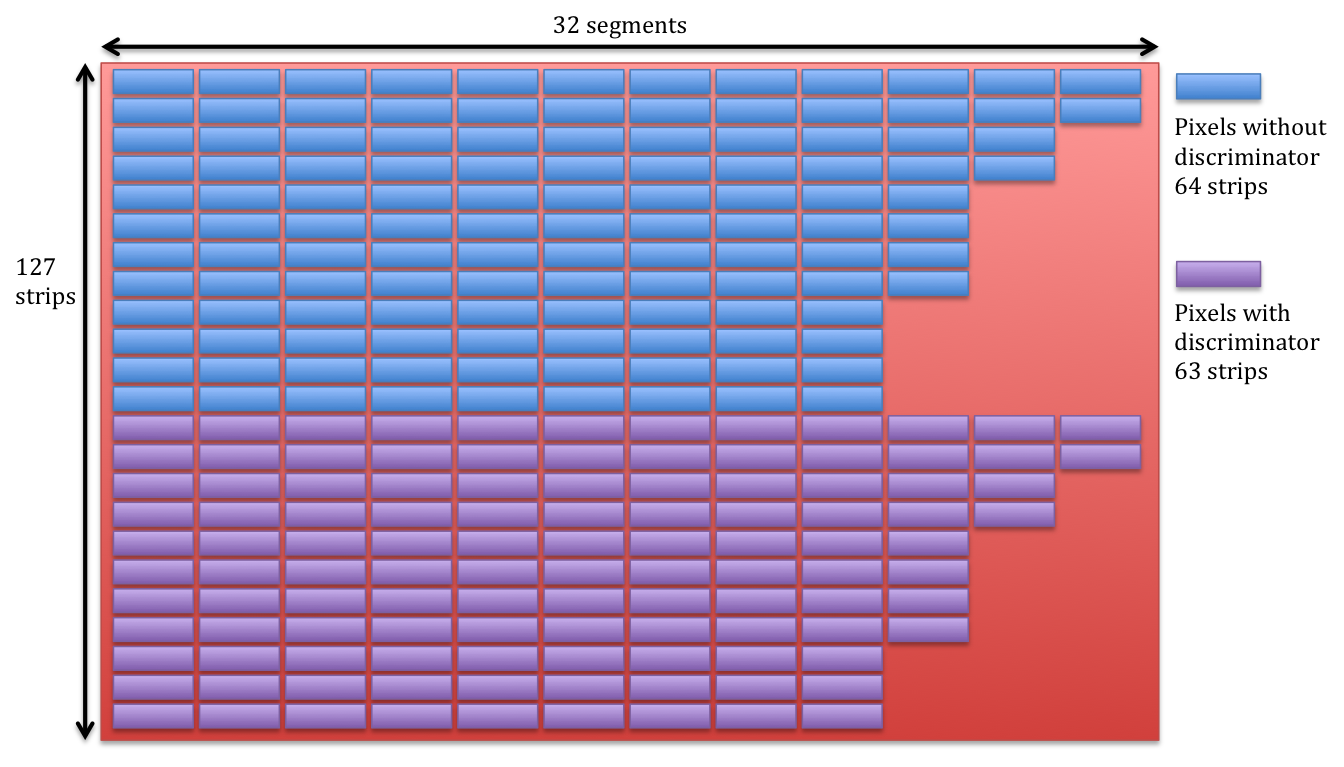


Figure 5–2 Details of the layout of the strip array

### Details of the strip array

Each strip is made of 32 independent pixels. A similar design to the one that was used in CHESS1 is used:

* 120V design rules.
* 8 connected sub-segments of size ~100µm.
* 30% diode area fraction.

Improvements:

* 40µm wide pixels
* Reduced size of p-implant between pixels

Simulation by Julie Segal and models bu AMS show that the pixel capacitance is a large function of the periphery

Therefore: remov

### Details of the amplifier

Each pixel houses an amplifier based on the same design as implemented in CHESS1. In addition it will house:

* Capacitor to allow charge injection for calibration.
* Masking scheme for hot pixel and power down the amplifier.
* A 25ns windowing circuit in order to avoid multiple triggering over several bunch crossing in case of wide pulses.

### Details of the discriminator

Depending upon which group the strip is in, the discriminator will be inside the pixel or at the periphery. The schematic and layout of this discriminator will be based upon Ivan’s design integrated in HVstripV1.

The discriminator is designed so that the chain of amplifier and discriminator is fast enough to be latched in a 25ns clock cycle. At the end of each clock cycle the state of the discriminator is latched at the periphery of the strip for all 32 pixels.

Amplifier

Discri.

Threshold

trimming

Latch

25ns Ck

In pixel

Pixel or periphery

Periphery

Figure 5–3 Schematic and location of the amplifier and discriminator

## Strip encoding

A strip encoding structure services each strip. Its purpose is to scan and select the first pixel that was hit. The scan starts from the left-most pixel and finishes at the right most, it is done in parallel for all 127 strips. The position of the first hit pixel is encoded in a 5-bit address.

Additionally, if more than one hit can be found on the strip a 6th bit, called flag, is raised to 1 to indicate the presence of additional hits on the strip.

At the end of the scan, a 7th bit, HIT, custom for each strip, is computed and indicates whether the strip was hit or not.

Some examples:

Table 5‑f Example of the strip encoding for different cases

|  |  |  |  |
| --- | --- | --- | --- |
|  | 5 bit address | Flag | HIT |
| No hits | 00000 | 0 | 0 |
| Single hit on first pixel | 00000 | 0 | 1 |
| Hit of the first pixel and somewhere else | 00001 | 1 | 1 |

The HIT bit is only used internally to distinguish strips with no hits from strips with a single hit on the first pixel. During the readout phase of the chip only the 5-bit address and the Flag bit are sent out externally. In total 6 bits are necessary to encode the hit positions on the strips.

### Details of the strip encoding

The strip encoding is done at the periphery of the chip. Each encoding structure is fed by the 32 memory points storing the state of the discriminators. A sequential scan across the 32 is performed in 6ns.

Table 5‑g Details of the encoding within a strip

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Digital states for increasing pixel number | | | | | | | | | | |
| Hit | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Prev | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| State | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

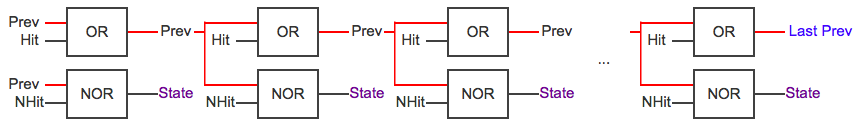


Figure 5–4 Schematic of the strip encoding scheme

### Details of the Flag raising

The flag is raised separately from the scanning using a current comparator. This is done in parallel for all pixels in a strip. Each discriminator output controls a current source all tied together to a FLAG line. The current on the FLAG line is compared to a reference current. If the current is higher than the one of a single current source the FLAG is raised.

Details is shown on Figure 5–5 FLAG raising scheme

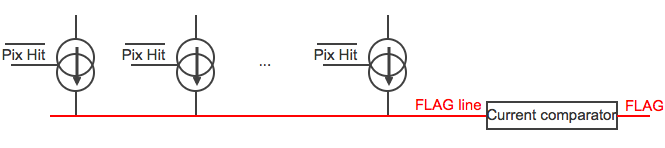


Figure 5–5 FLAG raising scheme

## Hit encoding

The hit encoding structure services all of the 127 strips. Its purpose is to scan and select 8 strips that were hit, to do so the 127 HIT bits produced at the end of the strip encoding are used. The scan start from a predefined, firmware programmable strip, STRIP\_INIT, selected amongst the 127. After each scan the position of that initial strip is incremented with a constant defined step.

A hit-encoding scan consists of finding the first 8 strips that were hit starting from STRIP\_INIT. Additional strip hits are simply discarded.

Once selected, the position of each of the 8 strips are encoded in 7 bits and sent to the LVDS output register along with the 5 bit address + Flag of the hit in that specific strip.

If less than 8 strips were hit the rest of the LVDS output register is filled with a 7-bit address corresponding to the 128th strip.

Some examples out data output:

Table 5‑h Case of 1 single hit in the first strip with no double hit.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 5bit pixel adr. | | | | | f | 7bit strip address | | | | | | |
| 1st word | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2nd word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3rd word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4th word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 5th word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 6th word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 7th word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 8th word | x | x | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 5‑i Case of 8 hits with some double hits.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 5bit pixel adr. | | | | | f | 7bit strip address | | | | | | |
| 1st word | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2nd word | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 3rd word | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 4th word | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 5th word | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 6th word | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 7th word | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 8th word | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

### Details of the hit encoding

The principle of the hit encoding is the following.

Strips are grouped in groups of 8; there are in total 16 groups of 8 strips. For each group, the number of hits are summed together in 3 bits. We call these sums the **8-strip sums**. This takes 25ns.

The second step is to form 16 **intermediate sums** by cumulatively adding the 8-strip sum of each group to the intermediate sum of the previous group, with the first group’s intermediate sum set to zero. This takes 25ns.

The third step is to scan each of the 16 groups in parallel. For each strip containing HIT=1 increment the intermediate sum of that group and store the number in the **hit number** memory including the **carry** as well. This takes 25ns.

The fourth step is to scan the **hit numbers** from 1 to 8 that have a HIT = 1 and **carry** = 0 and put the corresponding pixel address + flag and strip address on a 13 bits output bus. This takes 25ns.

In total the hit encoding takes 100ns, therefore this step will be time interleaved.

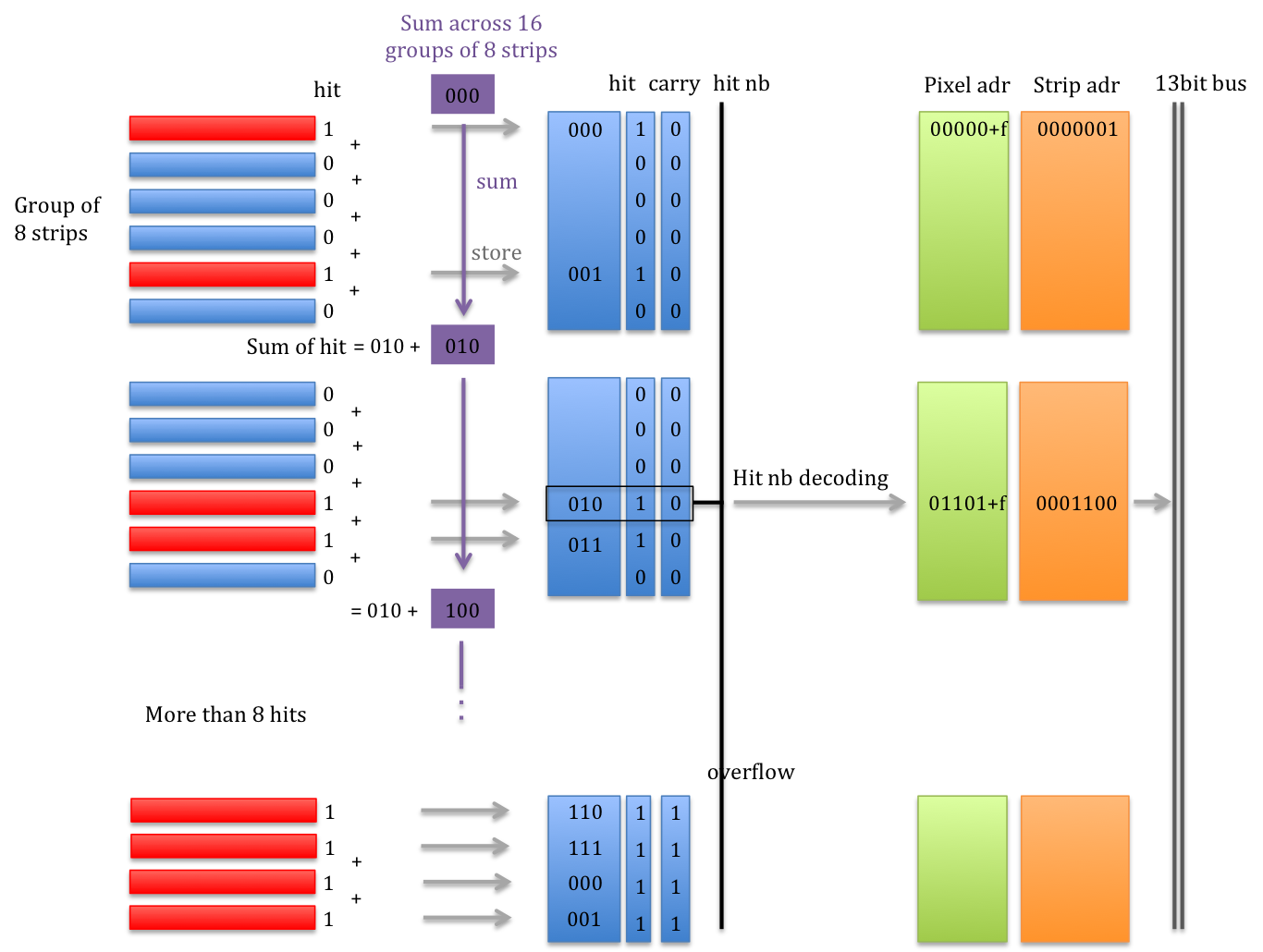


Figure 5–6 Prosposed encoding scheme for CHESS2

## Calibration – Masking – Threshold

Each pixel will also house 3 configuration registers that allow one to program:

* Selection of a pixel for calibration.
* Masking of hot pixels.
* Adjustment of the threshold of the discriminator for each pixel.

## LVDS output

The output of the chip works at 320MHz of 13bits with allows us to send out 8 hits of the detector every 25ns.

## SPI interface

# References

1. M. Havranek, et al., “Measurement of pixel sensor capacitances with sub-femtofarad precision”, *NIM A714*, 83-89 (2013).

1. Ivan Peric – Email correspondence with AMS [↑](#footnote-ref-1)
2. The minimum size required for 128 strips is 40µm x 128 = 0.5cm [↑](#footnote-ref-2)
3. Please refer to the rest of this documentation for a justification of this number [↑](#footnote-ref-3)