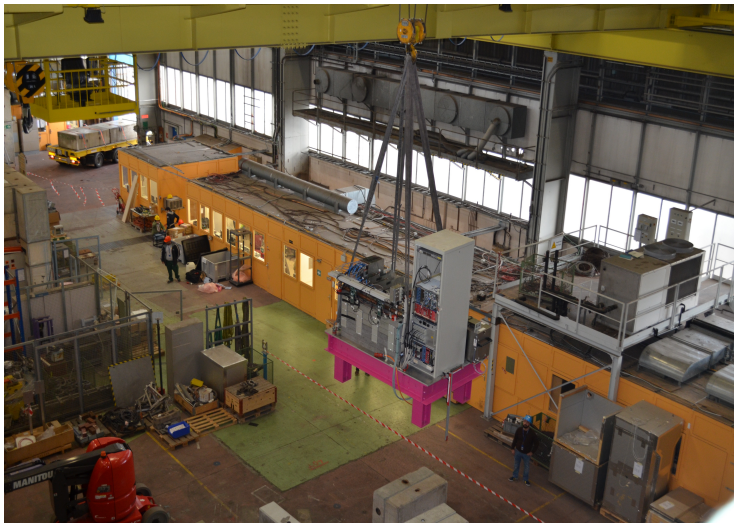
Status of the CALICE AHCAL Engineering prototype.

DPG Wuppertal 2015.

- Introduction
- Status :
  - Mechanics and Electronics
  - DAQ
  - Software
- Data Monitoring
- Commissioning phase
- Conclusion & Outlook



Eldwan Brianne
DPG-Frühjahrstagung
10.03.15, Wuppertal

Calorimeter for ILC

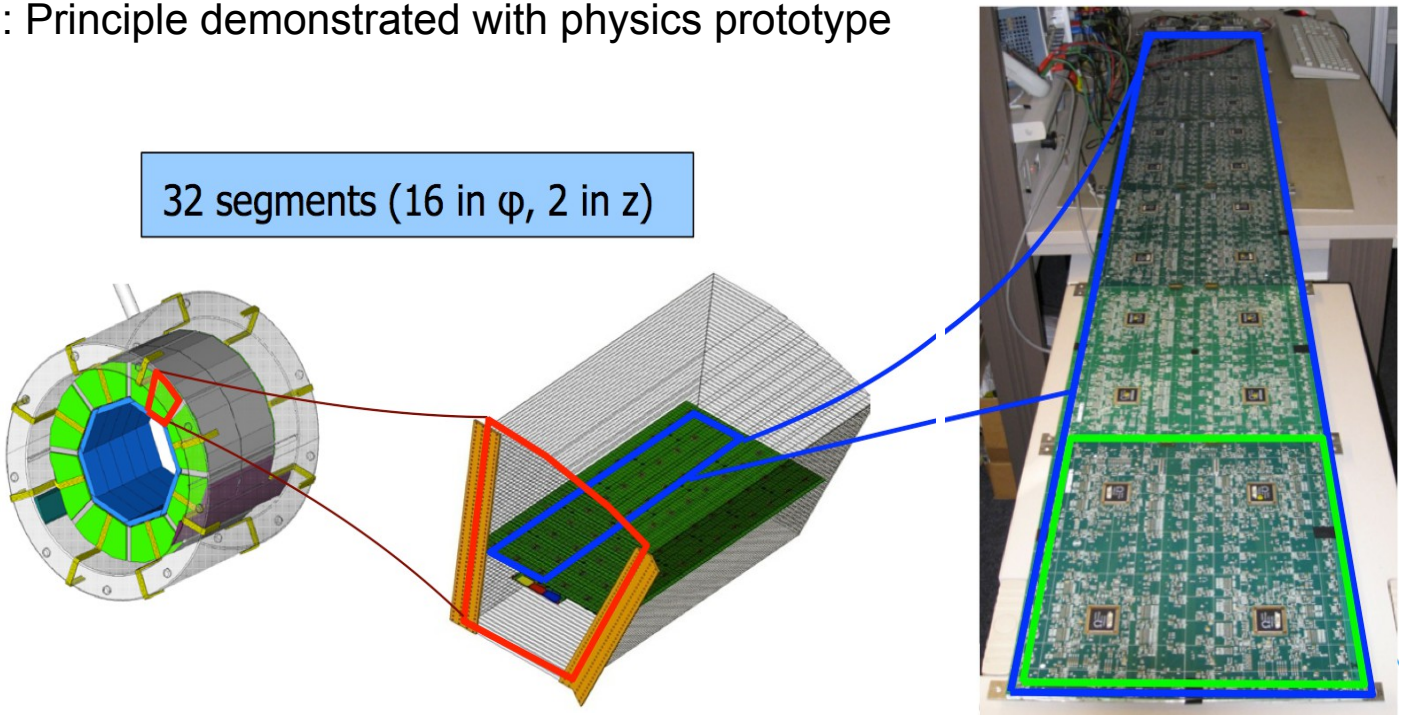
Collaborative Research Centre 676
Particles, Strings, and the Early Universe
The Structure of Matter and Space-Time

Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

DESY

The Analog Hadronic Calorimeter for ILD

- Sandwich calorimeter based on scintillator tiles (3x3 cm2) using Silicon photomultiplier readout.
- Hcal Base Unit (HBU) : 36x36 cm2 → 144 channels
- Embedded front end using ASICs (36 channels per ASIC → 4 ASICs per HBU)
- Full ILD detector : 8 millions channels → big challenge for particle flow detectors!
- Physics : Principle demonstrated with physics prototype



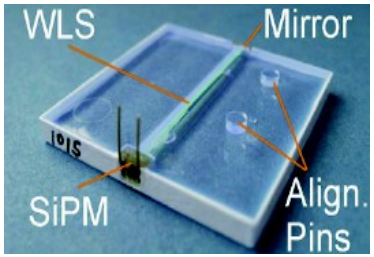
Engineering prototype

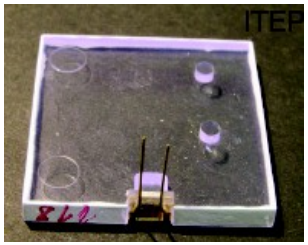
- Goals of the technological prototype :
  - Going towards full 1m3 prototype
  - Scalability to full ILD detector
  - Control and understanding of the electronics
  - Flexibility with fast SiPM technology development
  - Test of several board designs and SiPM (best suitable)
  - Physics : Timing development of hadronic showers (comparison between steel and tungsten absorber), Energy calibration validation
- Past Testbeam periods :
  - DESY January 2014 (First test of DAQ fast commands via HDMI, readout via USB)
  - CERN PS : October 2014 (First try with DAQ – fallback on USB readout due to kernel problems)

    November 2014 (DAQ with 2 mini-xLDAs working stable – full HDMI)
  - February 2015 : DESY with Airstack configuration in tungsten frames (channel-wise MIP calibration – 2x2 HBU configuration – 5 layers)

Hardware diversity

Old ITEP tiles with WLS fiber
800 px

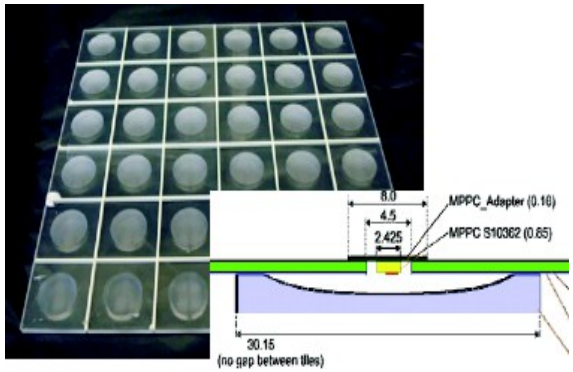




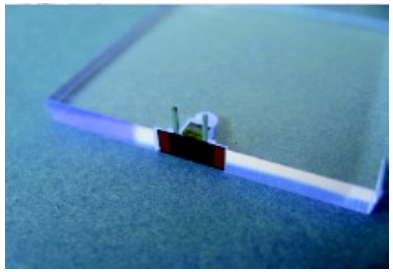
New ITEP tiles
Ketek 12k px

EBU strip
Hamamatsu 10k px - 3600 px

Very Complex system!!



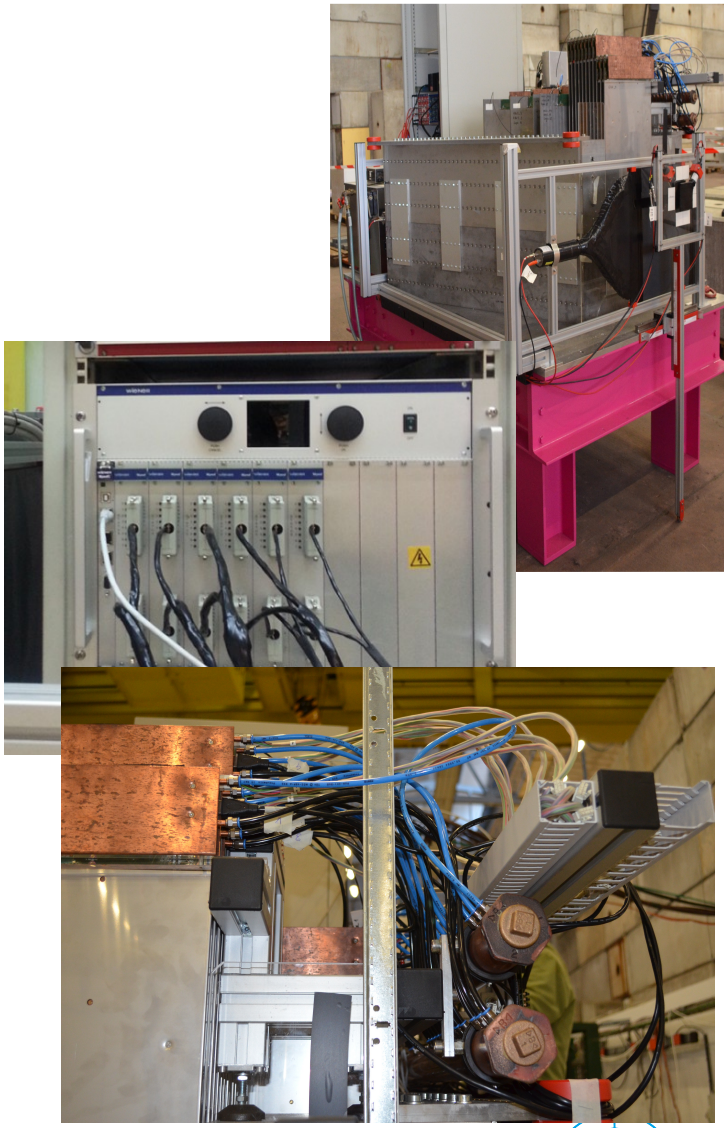
NIU megatile SMD
MPPC 1600 px (50 µm)
MPPC 25 µm



UHH + Heidelberg tiles
Ketek 2300 px
SenSL 1300 px

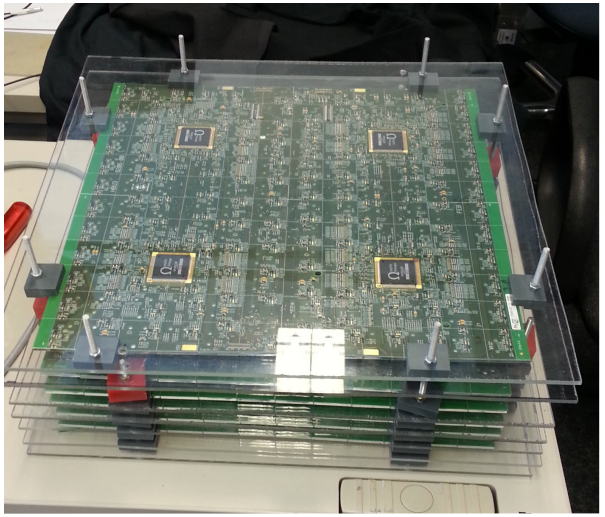
Status : Mechanics and Electronics

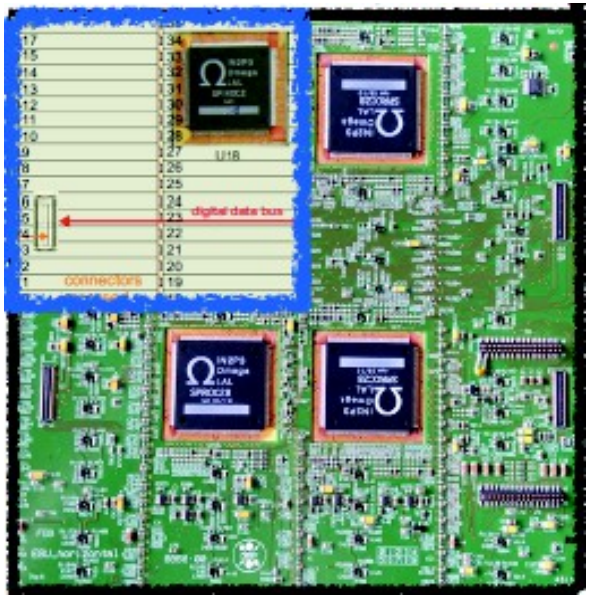
- EUDET Absorber structure :
  - Principle validated at DESY and CERN PS
  - Craning without any problems
- Power supply :
  - Now : Scalable commercial system – channel wise power distribution (3 voltages : electronics, LED calibration system, SiPM HV). Up to 16 layers, upgradable to 48 layers.
  - Future : Power supply developed at Dubna : low-cost, scalable to full ILD size.
- Cooling :
  - First test of active cooling during last TB at CERN PS → success
  - Mechanically not easy, not much room to insert layers into the stack
  - Improvements needed in cooling plate / power board coupling

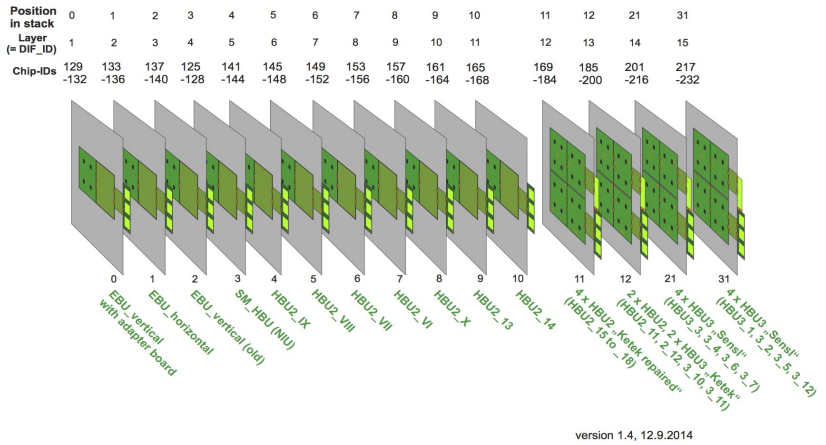


Status : Mechanics and Electronics

- Electronics :
  - Different HBU generations : HBU2, HBU3 and SMD
  - Several new HBUs arrived last summer from Heidelberg, UHH, NIU
  - Several EBUs from Japan (Shinshu, Tokyo)
  - New SMD HBU from Mainz (Feb 2015)
  - Commissioning of the boards was made at DESY (further in my talk)

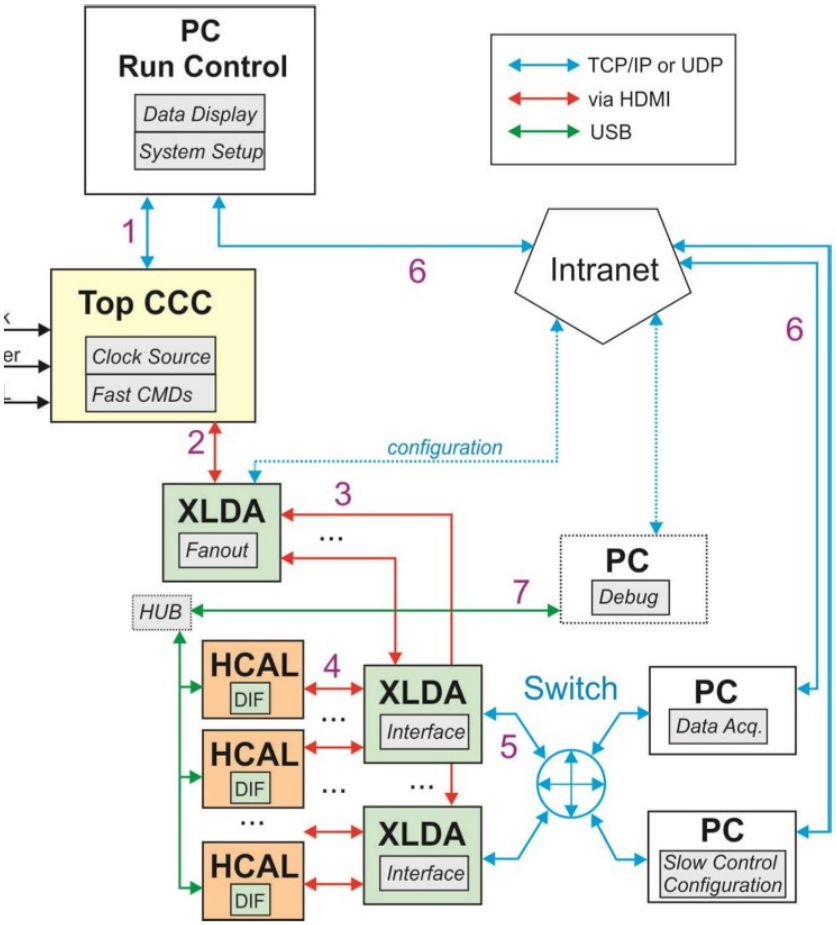






Status : Data Acquisition System

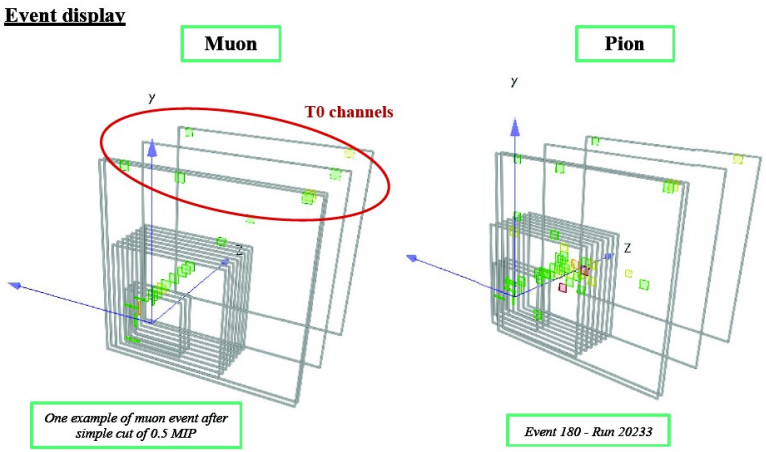
- New full HDMI based DAQ tested and fully working
- Wing LDA not useable yet : design problems. Received new Wing LDA last January → in progress concerning firmware development (Kintek-Zync link)
- Instead using 2 mini-xLDAs (based on Zedboards) : maximum 10 layers per xLDAs.
- Combined runs with Si-ECAL at CERN PS
- First step toward full DAQ integration : EUDAQ used for Run Control at PS



@ Ali Ebrahimi
AHCAL Main Meeting 2014

Status : Software

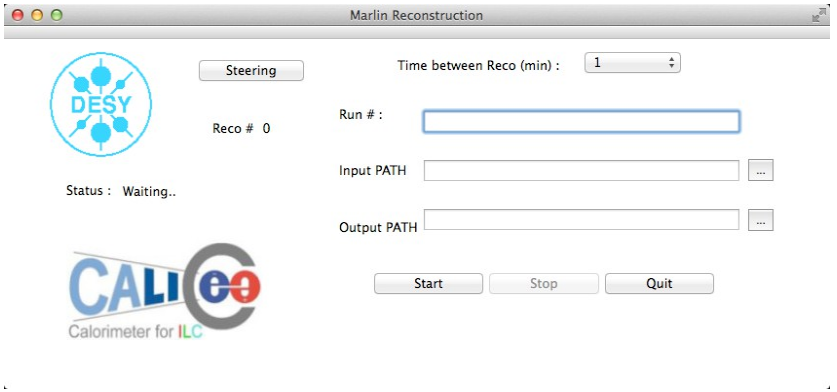
- Very challenging due to hardware diversity → needs in flexibility and scalabilty
- Use of the knowledge gain from the past and Commissioning for data monitoring and control of the electronics
- Event display required for geometry and data validation
- Achieved :
  - Proper reconstruction chain + GUI done
  - Database containing all information needed : Light yield, Pedestal, SiPM Gain.. Still need more work concerning user interaction
  - Online Monitors : 2 types for raw information and reconstructed data
  - Event Display set up

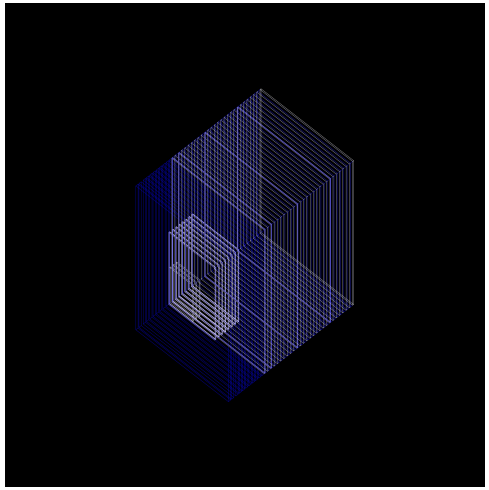


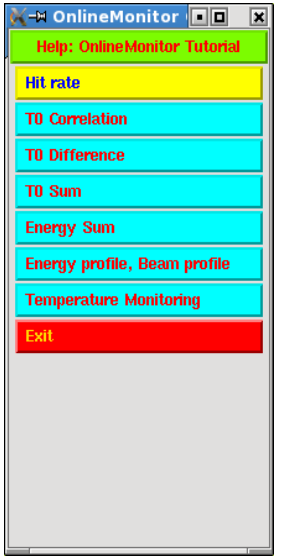
@ Lan Tran
CLIC Workshop

Software : Data monitoring

- Reconstruction GUI being developed
- Event display GUI : mapping/geometry validation
- Online Monitoring : Raw information already available + first version for reconstructed data (root-based client) → going towards a Qt GUI server / client
- Goal : Check physics performance of the detector based on few plots
- Needs :
  - Scalability : More layers = more data. Idea of servers looping over the data and sending the plots to a client (from anywhere)
  - Flexibility : Can add any kind of variable one want to look at
  - User-friendly : Development of a GUI needed (Qt or root)
- Many more software aspects :
  - Simulations
  - Digitization

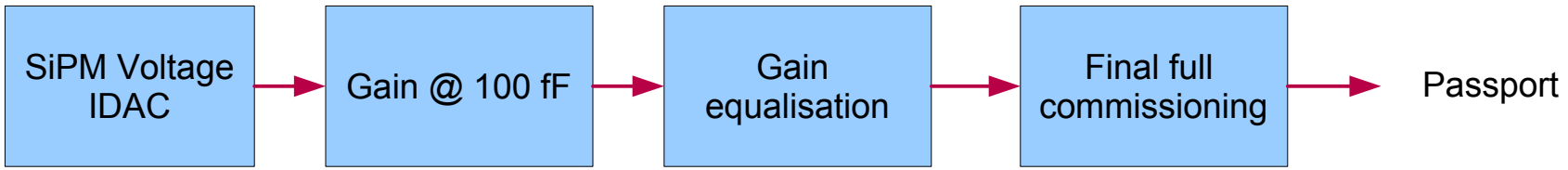






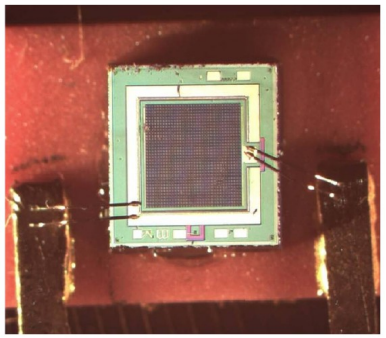
Commissioning phase

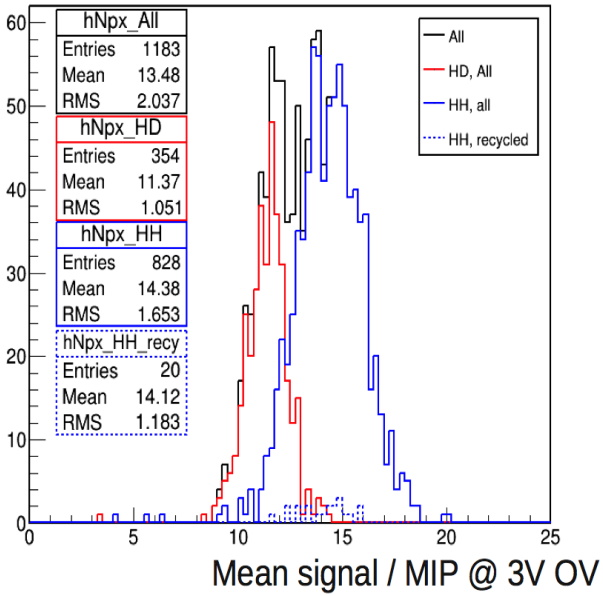
- Before last TB at CERN, many new boards were received → need to characterize them and calibrated them
- Old boards : Reuse of SC files, only full run (already calibrated - crosschecks)
- Commissioning :
  - Set up bias voltage for SiPMs
  - First characterization of the board (Gain measure)
  - Gain equalization
  - Final characterization
  - Assembly into cassette and insertion into stack
- Few Numbers :
  - CERN PS TB Setup : 15 layers (27 boards) including around 15 new HBUs/EBUs boards
  - ~ 3.800 channels to calibrate!!! With different SiPM types and geometries (SMD, Megatiles, EBUs..)



SiPM Voltage

- Chosen a posteriori by light yield measurements
- For SMD : generally no LY measurement → Estimate noise @ supplier over-voltage and gain measurements. Setup for light yield measure in development at Uni Mainz (P. Chau).
- SiPM diversity → Very different bias voltage per layers (each layer is unique)





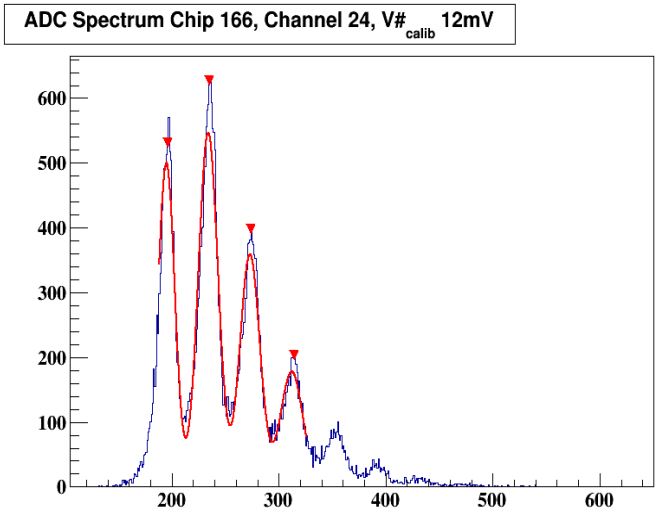
SiPM	V_{bd}	V_{op}
Hamamatsu (EBU)	~ 65 V	~ 70 V
Hamamatsu (NIU)	~ 65 V	~ 70 V
Old ITEP	~ 35 – 45 V	~ 37 - 50 V
New ITEP	~ 28 V	~ 32 V
UHH Ketek	~ 27 V	~ 30 V
SenSL	~ 26 V	~ 30 V

@ Konrad
CALICE Madrid 2014

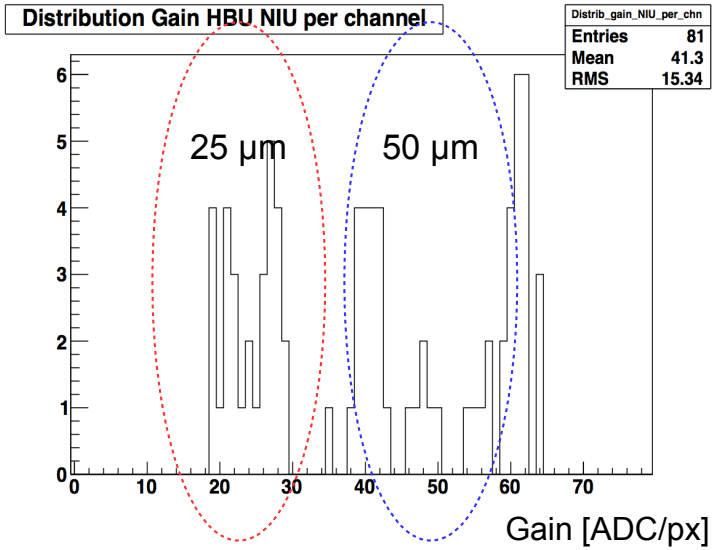
First Characterization

- For new boards, a first characterization of the SiPMs is needed. → Use of the integrated LED Calibration system.
- To do so, a LED scan over a certain voltage range is done by steps of 100 mV.
- Default chip parameters : Pre-Amplifier feedback capacity at 100 fF, External trigger, 16 triggers (one for each memory cells of the chip)
- Give us a first estimation of the gain (in ADC/px)

MPPC SiPM – SMD NIU



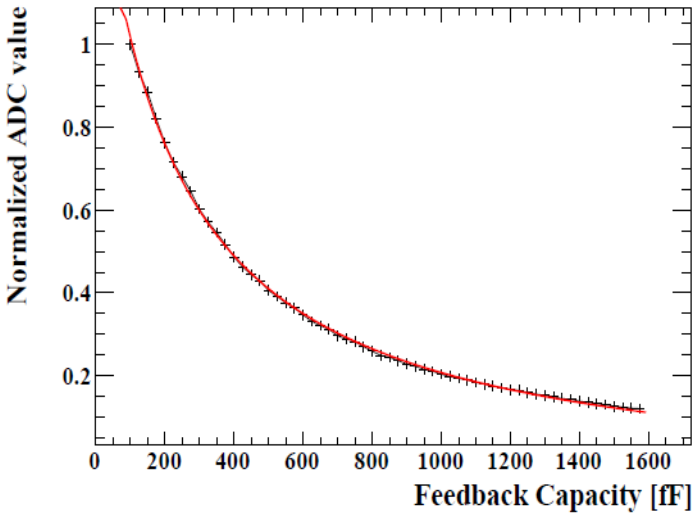
Amplitude [ADC]



Gain [ADC/px]

Gain equalization

- Goal : Matching the SiPM response to the ADC range of the chip and equalize the signal response between channels on the same chip/board.
- The gain can be modified by changing the PA of the chip. For each type of SiPM, a targeted gain is calculated.
- Then a second characterization is done in order to check if the targeted gain is achieved. Generally not more than 2 runs are needed.
- After the gain equalization, a final LED run is done with finer steps in order to get a gain value for each channels (to be put into the database for reconstruction) and threshold calculation.



Layer	4	5	6	7	8	9	10	11	12	13	14	15
Gain	~ 20	~ 22	~ 22	~ 22	~ 22	~ 22	~ 6	~ 6	~ 16	~ 16	~ 24	~ 24

Conclusion & Outlook

- Going towards a full prototype (1m3)
  - EUDET steel stack
  - First active cooling prototype
  - 27 boards equipped (including 4 big layers of 2x2 HBUs)
  - More boards to expect this year
- DAQ with 2 mini-xLDAs stably working
  - Stepping into a common DAQ (EUDAQ)
  - Next step : Wing LDA (up to 96 layers!!)
- Software
  - Fully implemented (supported by FLC desy)
  - Event display and Online Monitoring to check physics performance during data taking
- Commissioning
  - Lots of experience acquired during last summer
  - Trying to improve further the procedure and reduce time for commissioning
- Outlook
  - TB periods planned for June at DESY (dress rehearsal)
  - TB period this summer at CERN SPS
  - Maybe more...

Thank you for your attention