# CHESS-2 Readout Electronics

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Office of Science

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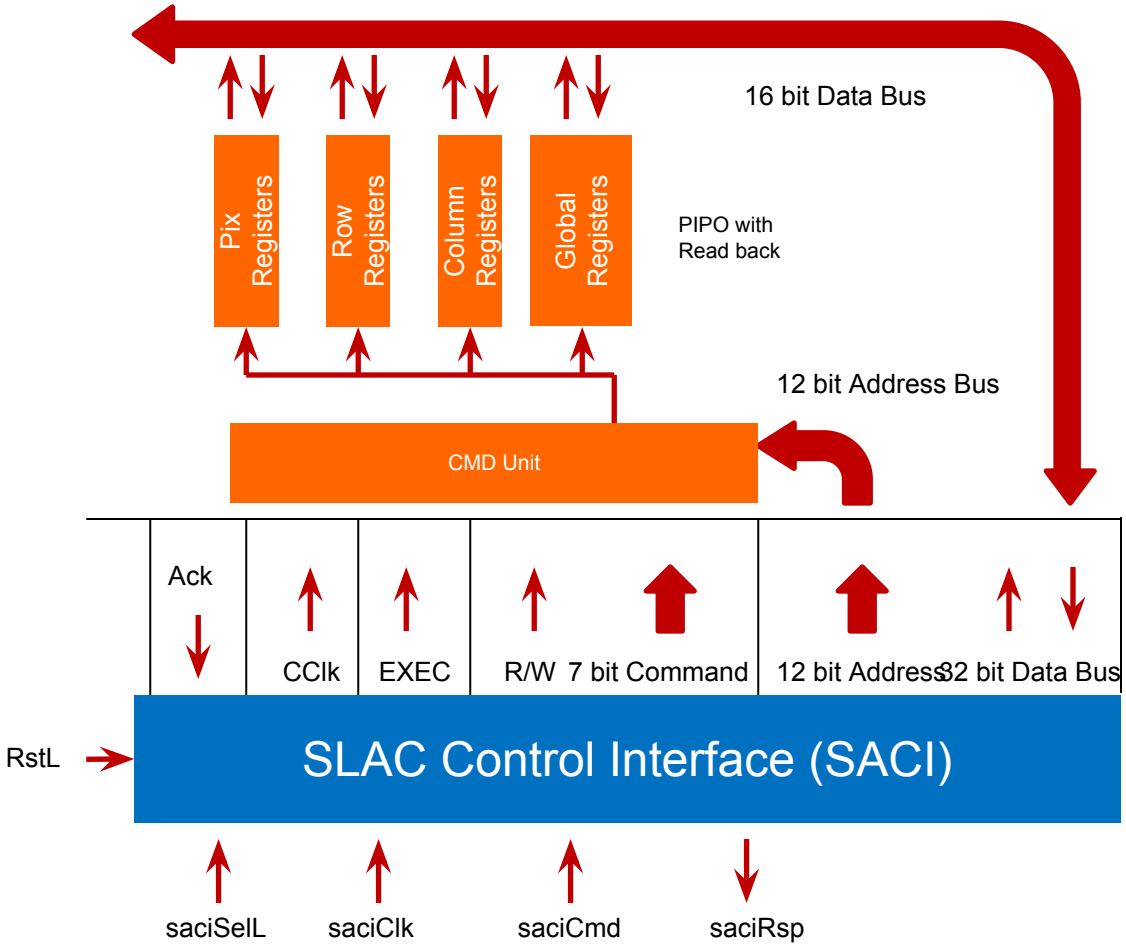
# SLAC ASIC Control Interface (SACI)




**Serial Interface with handshake protocol**

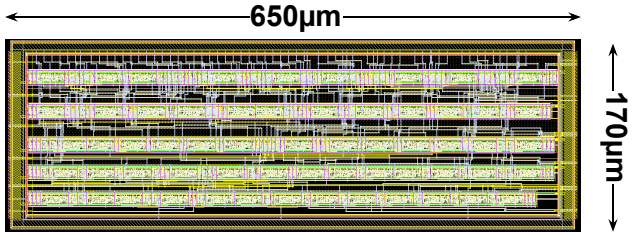
5 Signals

- 3 shared: *saciClk*, *saciCmd*, *saciRsp*.
- 1 dedicated select line per slave: *saciSelL*.
- 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.

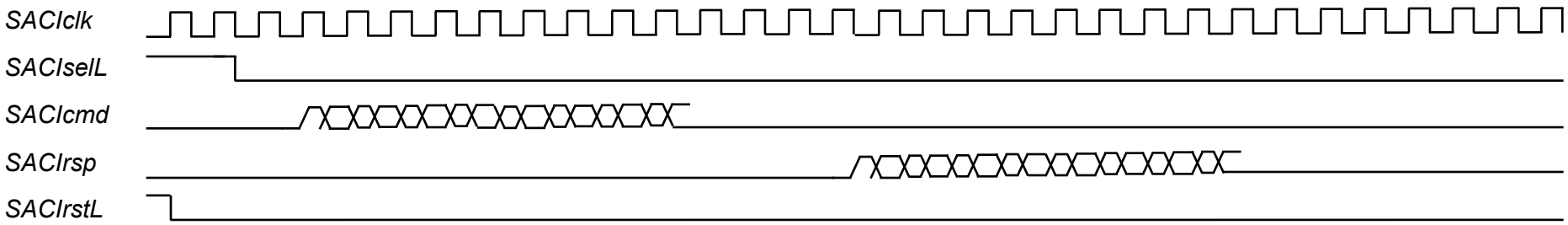
•Operated between 0V and 3.3V

• Allows multiple SACI on same bus (parallel mode).

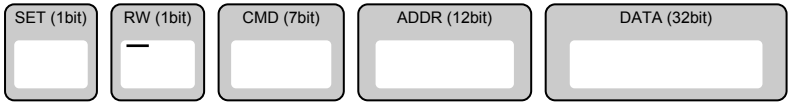
**Layout**



# SACI signals




SACIcmd (serial signal):

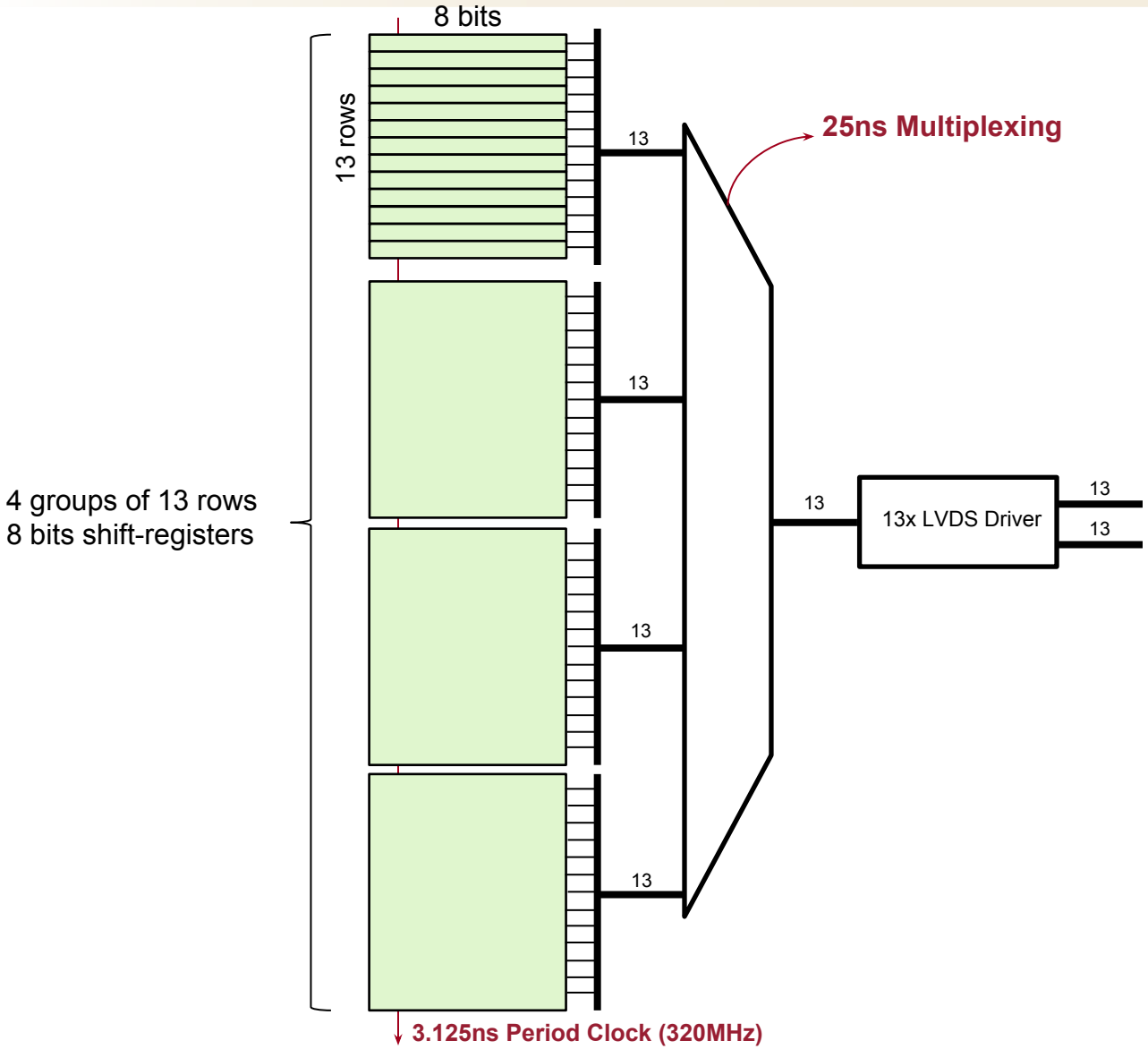



SACIrsp (serial signal):

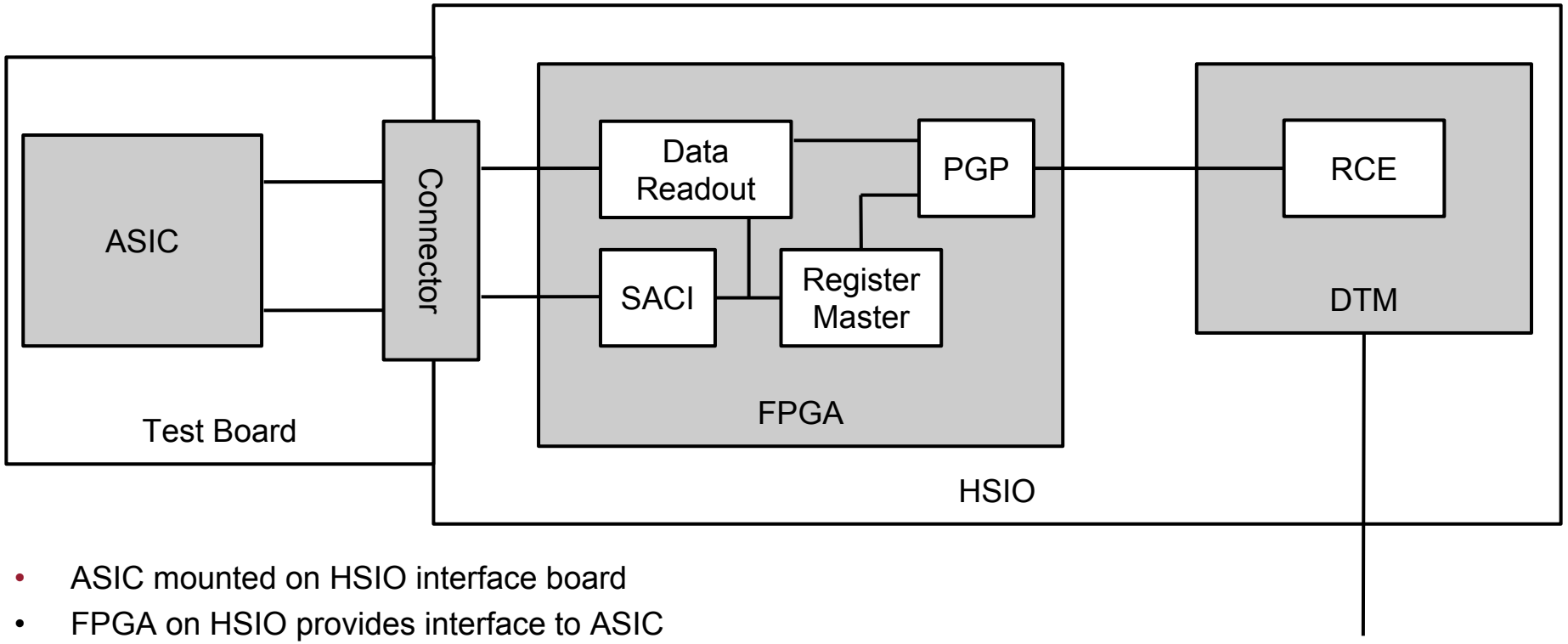

Write Mode

Read Mode

# Read-Out scheme

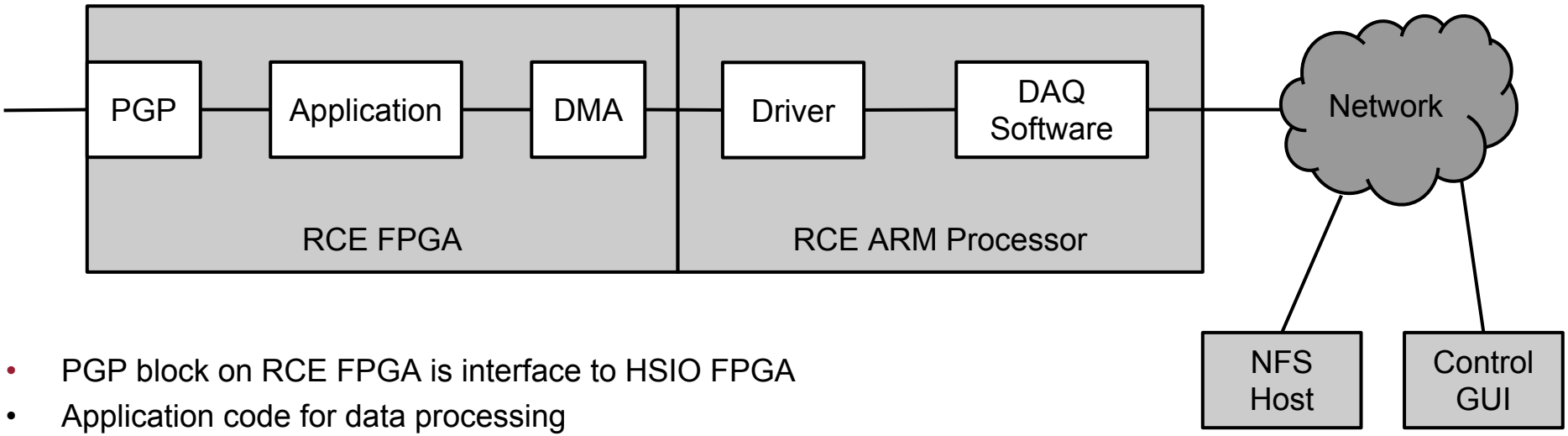


# Readout Hardware




- ASIC mounted on HSIO interface board
- FPGA on HSIO provides interface to ASIC
  - SACI for register access
  - Data readout block (13 LVDS pairs)
- PGP link to DTM mounted on HSIO
  - RCE contains stock PGP core and DMA engine
  - Inline data processing can be added later
- External 1Gbps Ethernet

# DTM Hardware / Software




- PGP block on RCE FPGA is interface to HSIO FPGA
- Application code for data processing
- DMA engine interfaces PGP core to software driver
- DAQ software resides on RCE
  - Register control and monitoring
  - ASIC configuration and control
  - Data processing
  - Generic software provided by SLAC
- Data stored on NFS disk space
- Control GUI for configuration and run control

# HSIO