

BCM1F

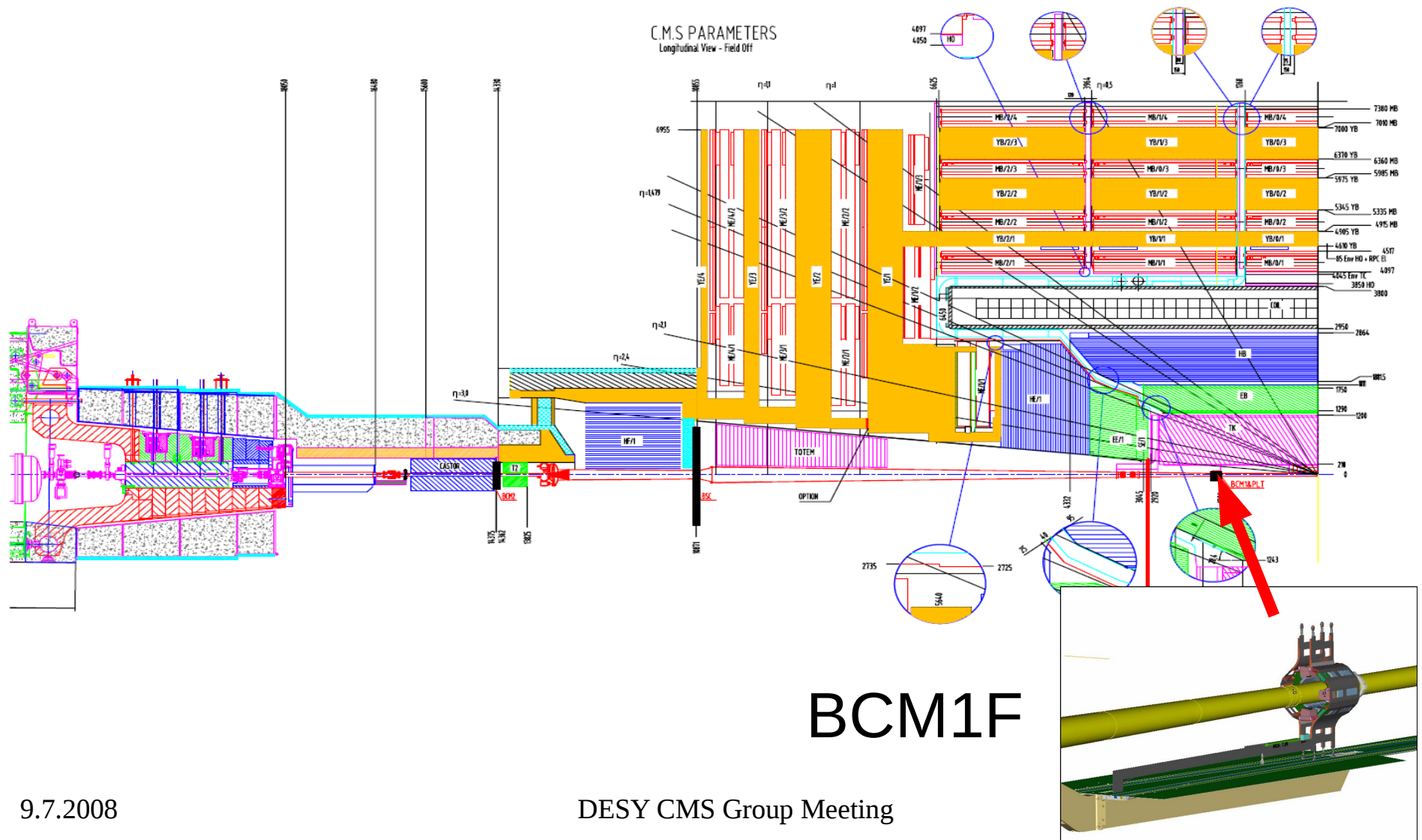
Status of DAQ Software

M. Ohlerich

Content

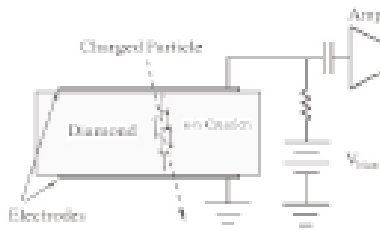
- Introduction
- Boundary conditions – Hardware Properties
- BCM1F DAQ Software – Design Principles

Introduction ...

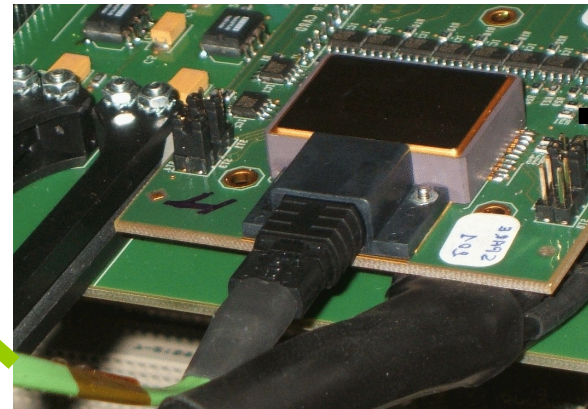
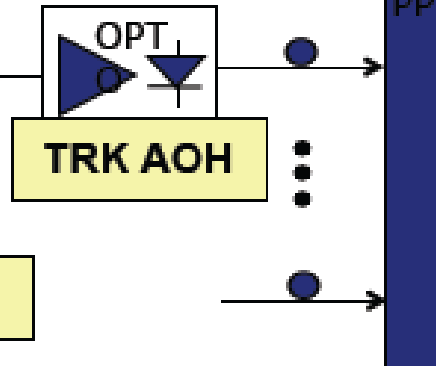


Readout-Chain

Single Crystal Diamond



Amplifier JK16 rad hard

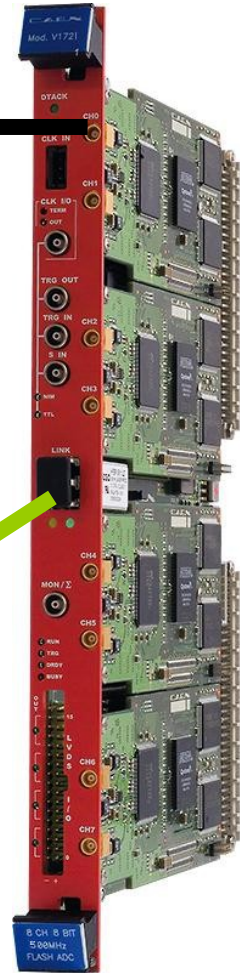


**Central Data
POOL
DIP Data Base**

DIP



opt.



ADC V1721

Digitizer's Main Properties

40MHz clock
(machine clock sync)

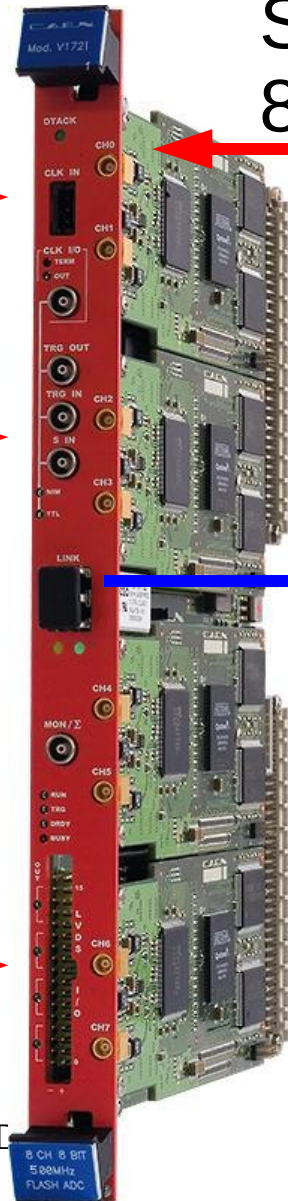
Signal from
8 BCM1F sc CVD diamonds

External Trigger
(Orbit clock $\sim 12\text{kHz}$)

Optical Link to
Readout PC

LVDS
Orbit number

LVDS pattern will be
in Event Header



Further properties ...

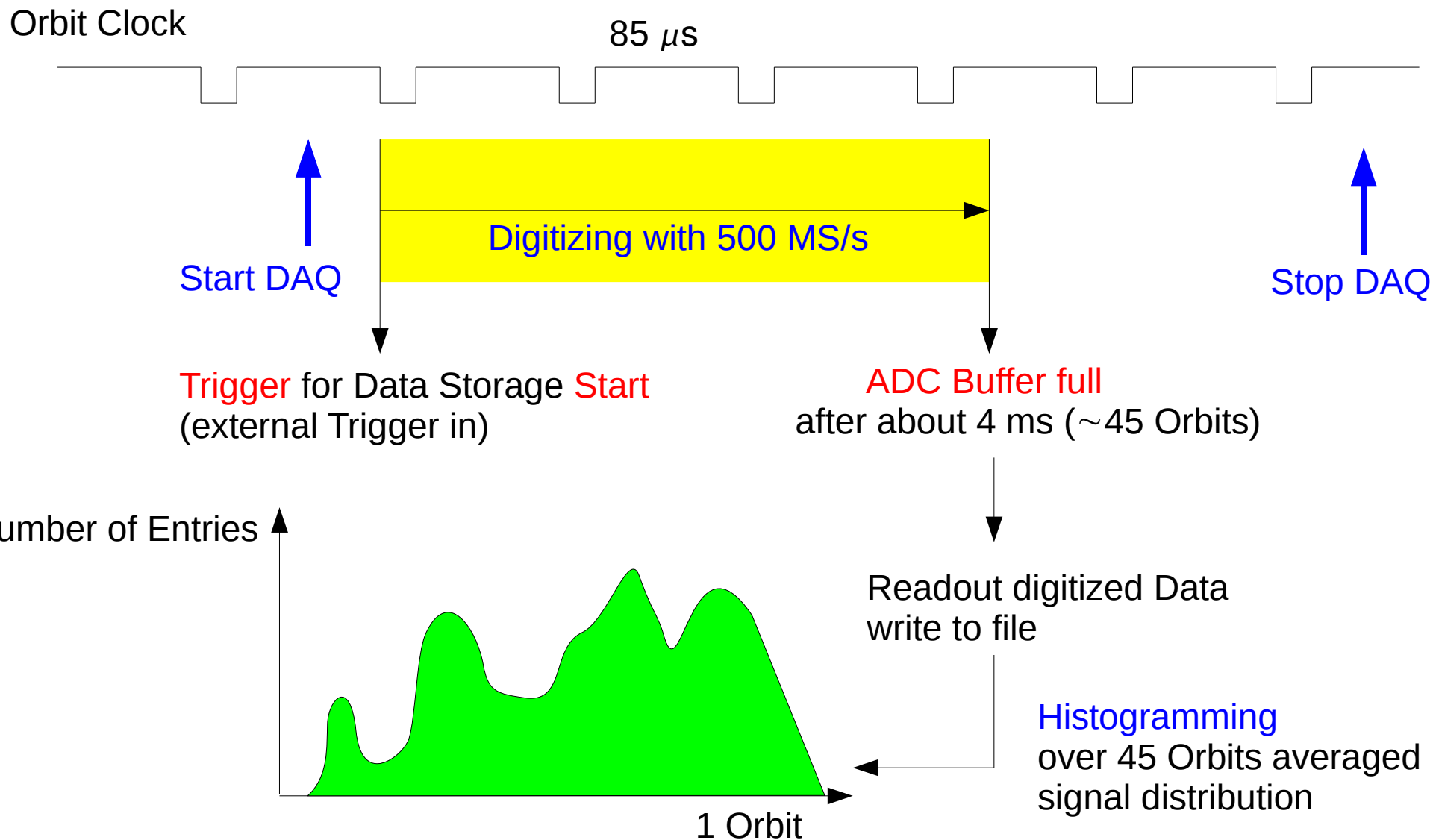
Data (signal voltage levels) are digitized

Sampling : 500 MB/s , i.e. one 8-Bit sample each 2ns

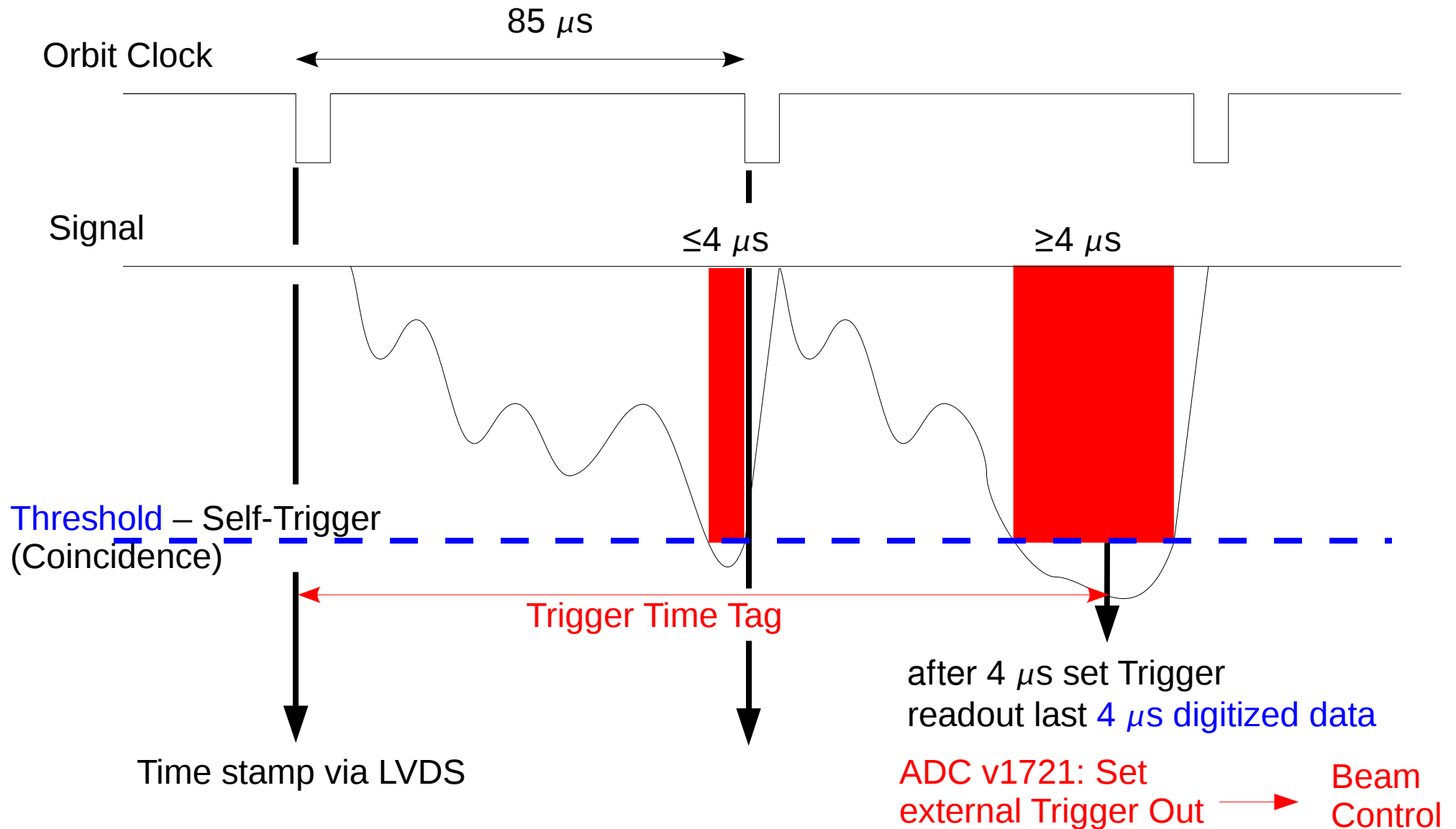
Readout : max 60-80 MB/s (VME)

Self-Triggering,
coincidence logic,
Zero-Suppression, ... similar to a oscilloscope

First Proposal – Learn Mode



Second Proposal – Warning Mode



Current Status - patchy Monitoring

Comparable to [Learn Mode](#), but with DAQ accessories

More complex / complicated due to User controls, Interfaces, ...

Necessary [Hardware](#):

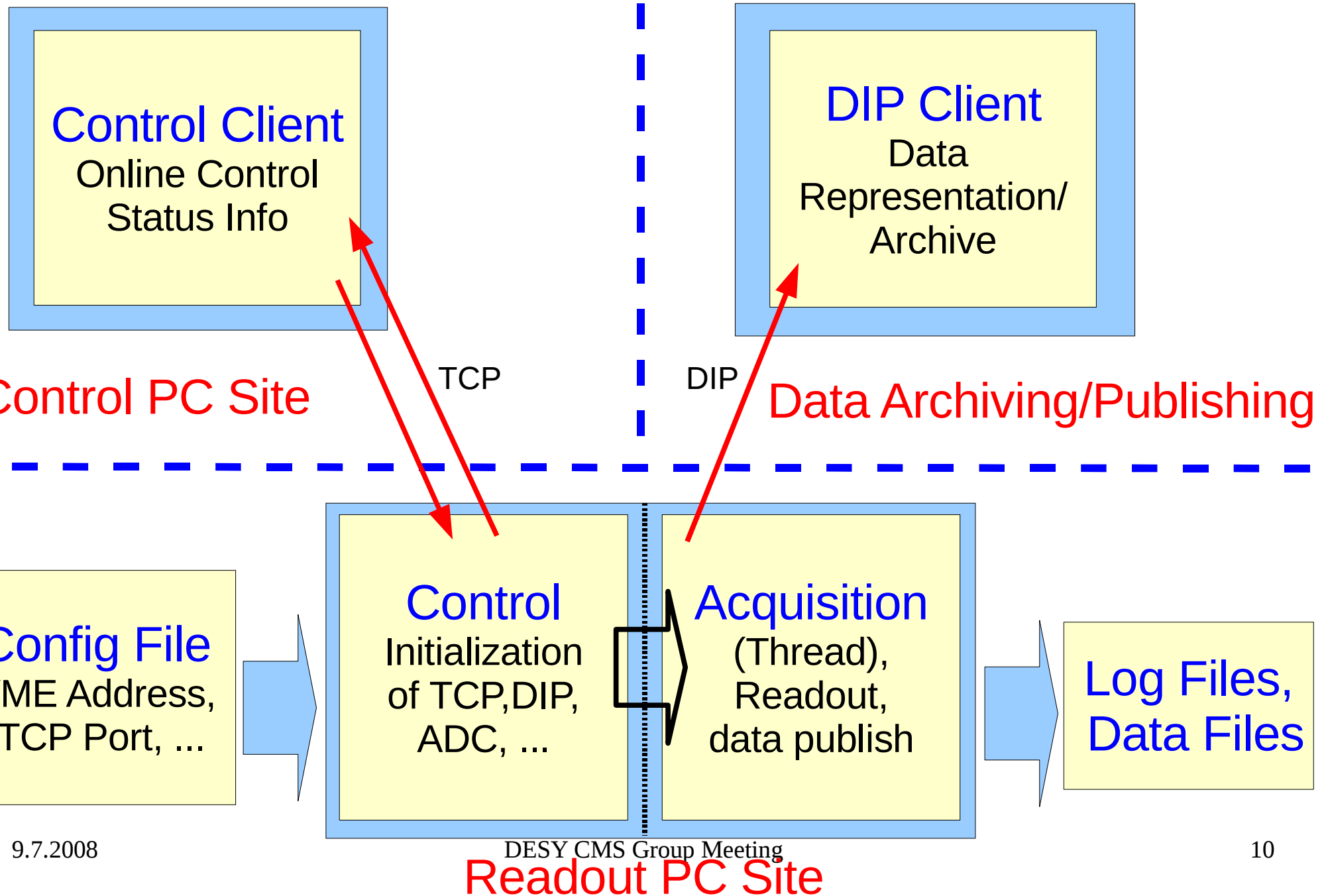
- 1 CAEN PCI card a2818

Necessary [Software](#):

- Linux (SL)
- CAEN Library
- a2818 Kernel Module (PCI card)
- DIP Library
- and
- BCM1F daemon

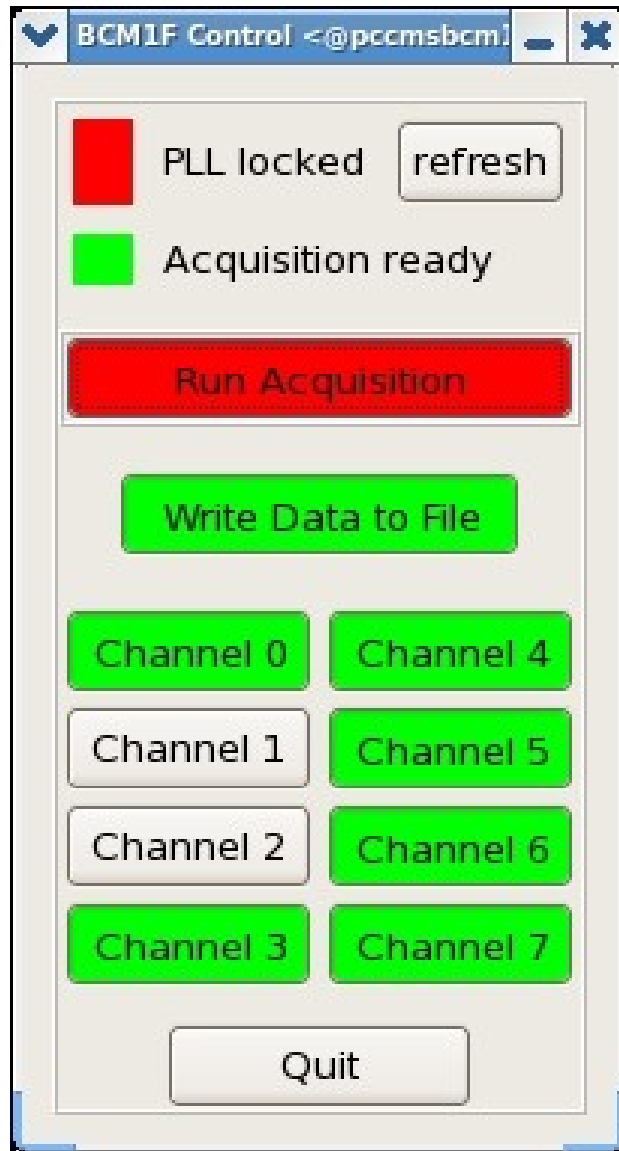


BCM1F Software Structure

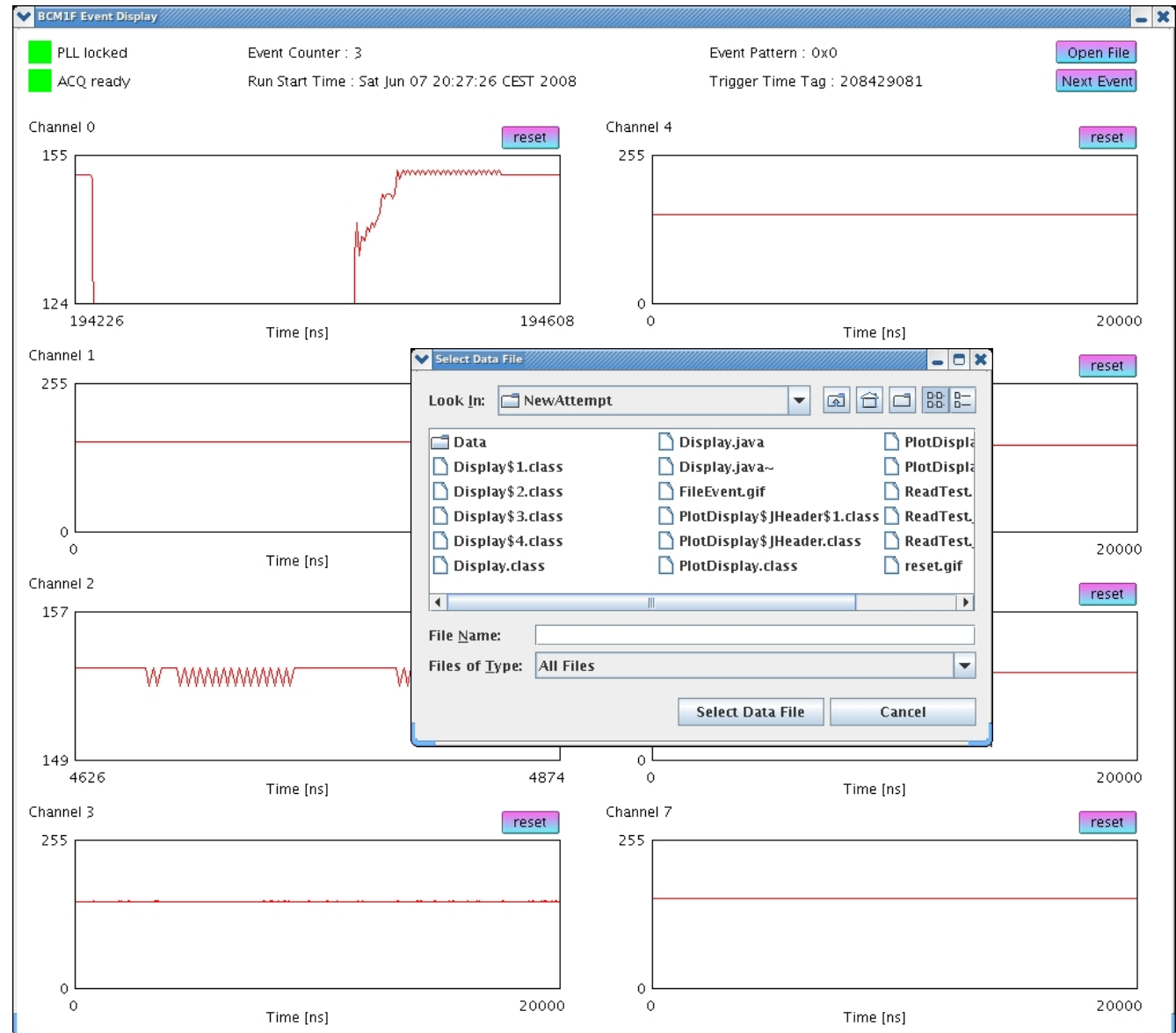


Surfaces – Python, Java, ...

Control Panel



On-/Offline Displays



Status ...

Must be further tested ...
(Test setup at DESY in Zeuthen)

Ringo Schmidt continues DSP ...

Must be integrated (Data → DQM, ...)