Minutes of Strip CMOS sensor progress report meeting, V.1

*2015-03-17*

*Present:* B.Hommels, J. Dopke, C. Buttar, D. Bortoletto ,,I.Mandic, , RNickerson, T.Huffman, V.Fadeyev, Z.Liang, J. Zhang, A. Grillo, C.Klein, D.Maneuski, F.Wilson, Forest, H.Grabas, J. JohnJohn, M.Kodan, Matt, P.Keener,R.Plackett, R.Wang, SLAC, S. Dong,
 [taken from Vidyo listing of attendees]

INDICO address: <https://indico.desy.de/conferenceDisplay.py?confId=12119>

*Next Meeting*

The next meeting will be 31st March 2015

*General*

An email list and a layout document were attached to the INDICO page, these were for reference. Comments were solicited on the layout document. The specific strip CMOS egroups email list will be used in future.

*Surface Charge and N-well simulations*

To attempt to understand the high isolation resistance observed after irradiation without guard rings, Julie has simulated surface charges. The results show a reduced resistivity contrary to the observation, there was speculation that the Oxide layer may be thinner than simulated, or rather that the trapped surface charge may be less. This is not yet understood.

Julie also reported on her simulations of the effects of rounding the corners on pads. The idea being to reduce the field strength. For 1000ohm substrate there is no point, and for 22ohm there is a reduction in peak fields, so there is no harm in doing it. Whilst the figures are relative, there is a suggestion that the peak field is close to breakdown in 22ohm.

SACI

The SLAC SACI was described and suggested as an interface to the CHESS-II chip. This offers advantages, including a well developed suite of software. It was stated that this was an open standard and that a block would be available to drop into designs. This would CHESS-ii to read-out ASIC. The system would also be applicable to final read-out, but the utility of this was less obvious due to the existing infrastructure at groups, and was left to further discussion offline. SLAC will work on providing interface blocks.

*CMOS Modules*

Alex presented his thoughts on module design, which is needed for the document on layouts. He listed a number of possible configurations and outlined the limitations. One will be selected for the layout document. Some further investigation of possible duplication of pads on the ABCn’ will be done.

*Testing HVStrip1*

Argonne reported on their progress in setting up a test bed for HVStrip1 chips. Some leakage current measurements were presented and a DAQ error reported. There were some suggestions on how to progress from the group.

*Testing CHESS 1*

Igor presented latest results on edge TCT on irradiated devices. Fluences up to 2x10^15neq are now in hand and three devices have been measured. The signal size measured with Sr90 continues to rise. This is consistent with the measured increase in the charge collection region caused by acceptor depletion.

The charge collection region measured with edgeTCT shows a, not understood, dramatic increase between 2 and 5 10^15 on PPA11. This does not seem to be reflected in signal size, so there is currently not a clear picture of what is happening here (slide 7 in presentation). The change in collection region can be seen in the size of charge collected at pixel boundaries, which improves a lot after irradiation.

*Test Kit Status*

JayaJohn reported on the AMS-CHESS1 board footprint and attached daughterboard schematics to the indico page for comment.