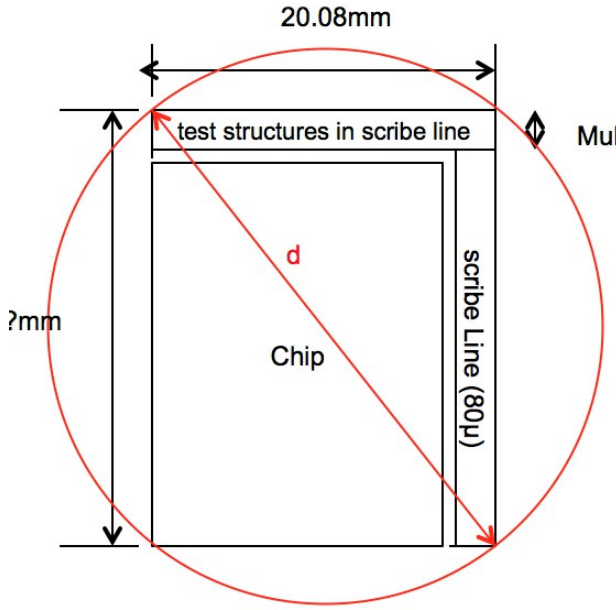
Module considerations

- Was travelling last time, could not properly connect – sorry.
- Please not that some work was already done during the “Strip-CMOS-TF” in early 2014, in particular by Tony Affolder
  - find some slides later, see https://indico.cern.ch/category/5333/
- Main message: The reticule size is limited by
  - $x < 22mm$, $y < 26mm$, $d < 31.112mm$ (diameter, i.e. $d < \sqrt{x^2+y^2}$)
  - Keep in mind dicing streets (80 µm) and possibly necessary test structures which are usually kept inside dicing streets (can be negotiated with AMS and probably limited to one side of the chip)

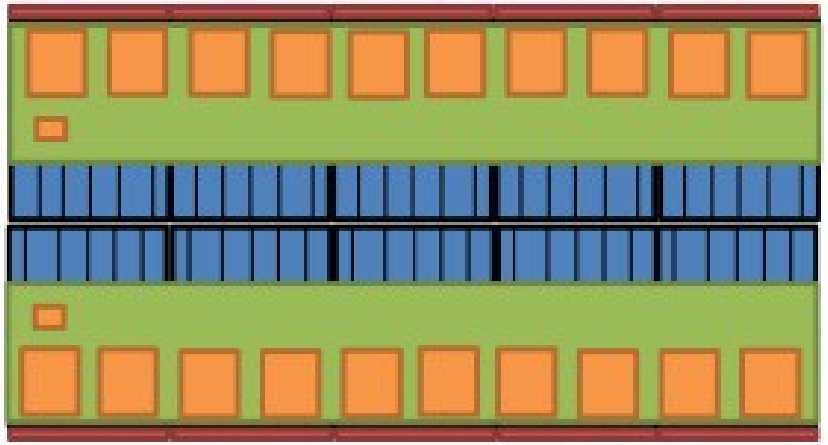


Max. ⌀ = 31112 µm
Max. x= 22 mm
Max. y = 26 mm

Calculation:
$d^2 = x^2 + y^2$
$31112^2 = 20080^2 + y^2)$
y= 23.764mm (part of this is end-of-column logic)

Module Architectures

- Not pursuing 2d stitching
  - Not possible at most foundries
  - Could have huge cost implications (cost per wafer and yield)
  - With 2d info in CMOS sensor, benefit of handling minimized
- We assuming base module element will be a 4-5 reticle wide x 1 reticle long object
  - Might make sense to build modules out of two of these with peripheries pointing out
- Width of base module element depends on how we assembly the reticle element and best use of the 8" wafers (current 97 mm width optimizes a 6" wafer)

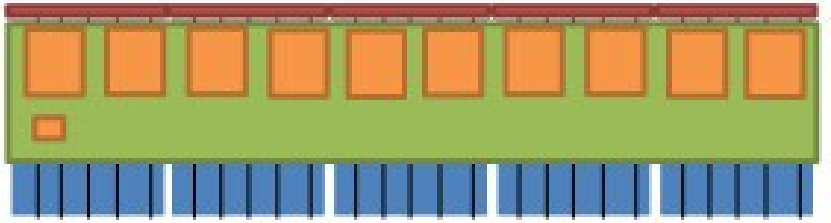


- Alternate modules on opposite sides of support material with overlapping active areas

Stave with alternating 48 mm modules

"Low" Yield Option (I)

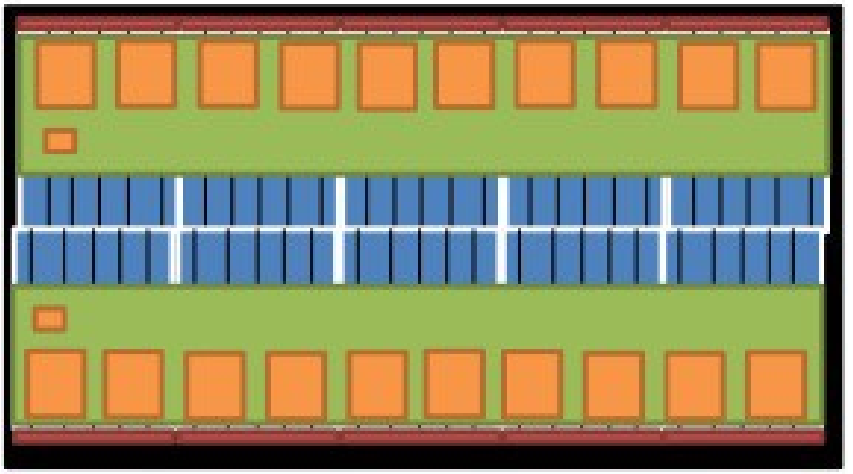
- If yield is low (<90-95%), cost benefits will hard to achieve unless modules assembled out of single good reticles
  - Width of module independent of CMOS wafer size
- Lowest mass method to do this is to use hybrid to tie reticles together
  - Required spacing between die and its precision isn't obvious

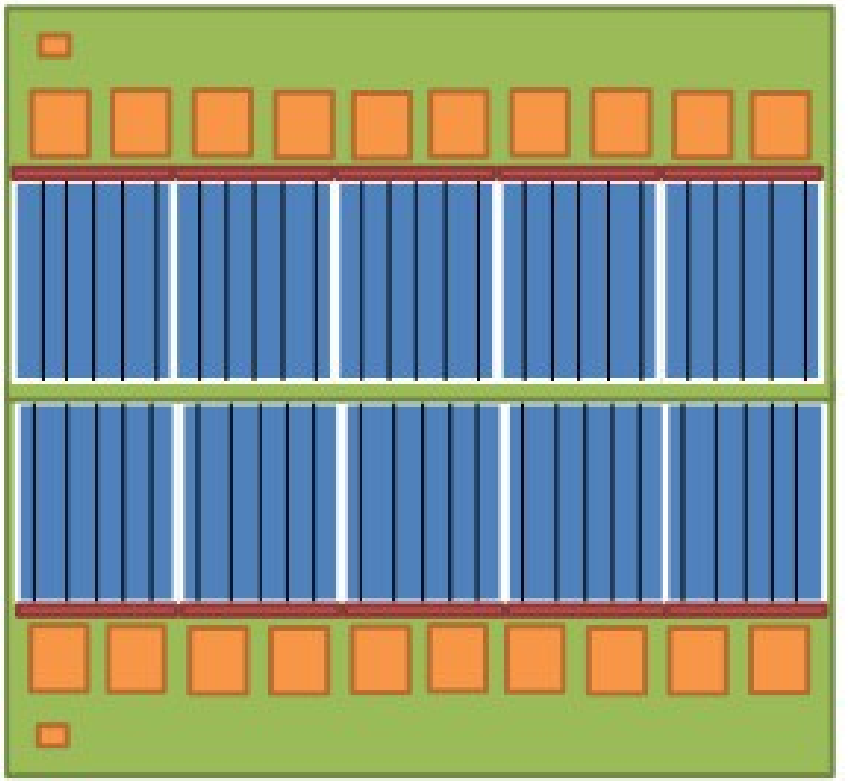


- In discussions with Tim, it may be more difficult to cool middle dies
  - No lateral cooling between dies (in silicon)
  - Cooling would have to be through face sheets to pipes

“Low” Yield Option (II)

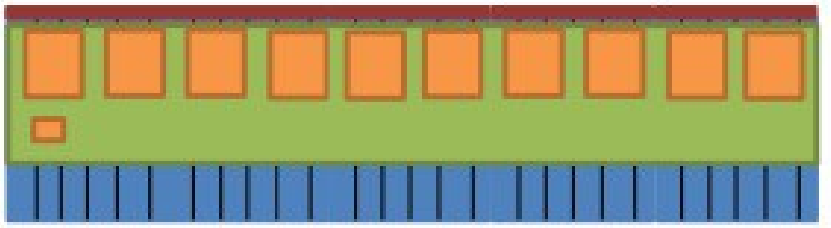
- A higher mass method would be to have a carrier with good thermal properties (CF, ceramics, TPG,..) which reticles are attached
- Or you could extend hybrid flex to provide in-between option





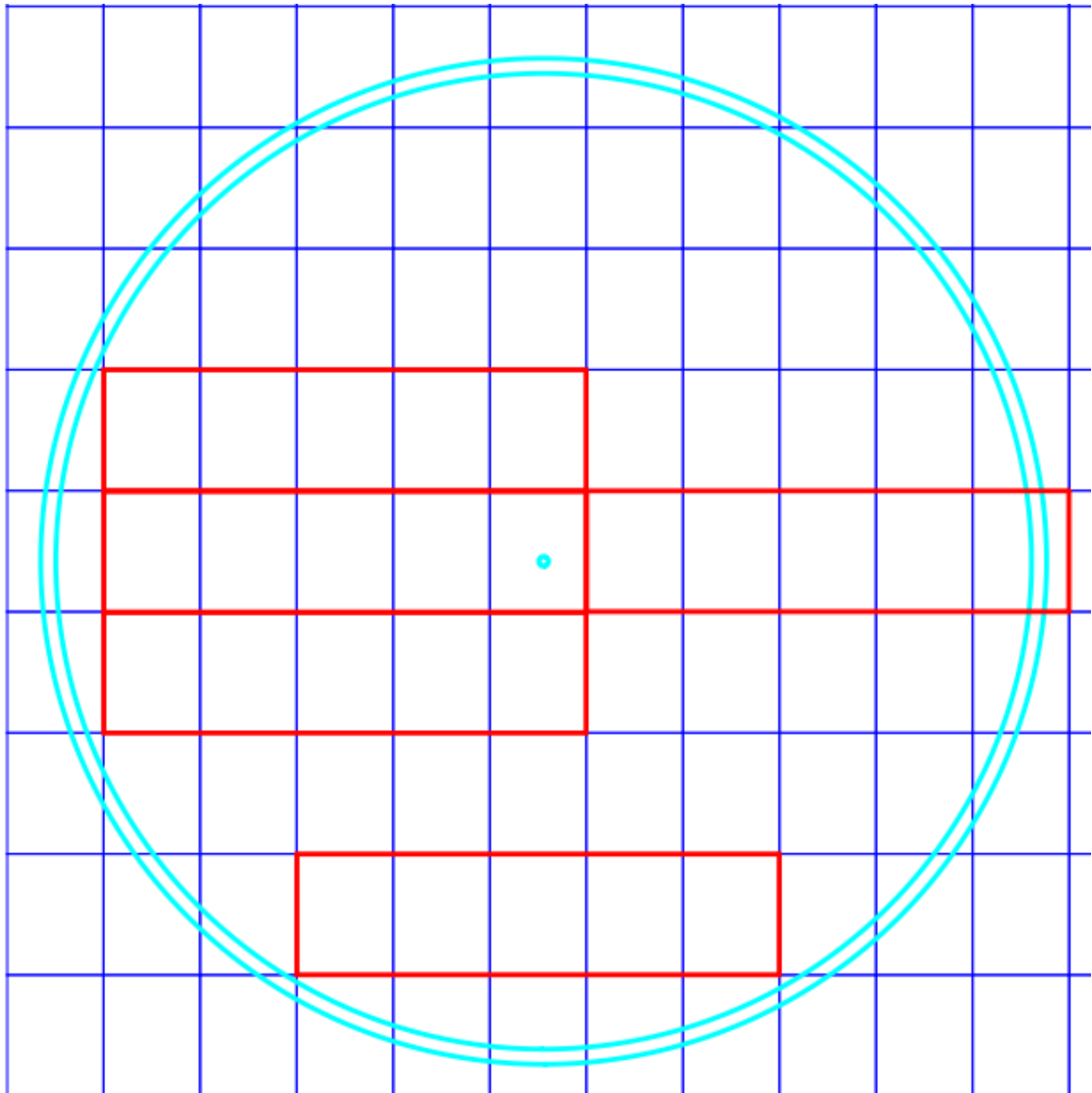
1D stitching option Option

- If available, 1d stitching could be considered
  - Benefits aren't huge relative to dicing 1xn section of wafer
    - Periphery could be tied together which will make servicing CMOS sensor easier
  - For stereo option, stereo strips ending at each of reticle could be tied to neighboring reticle in a "continuous" line
  - Dead area between reticles could possibly be reduced



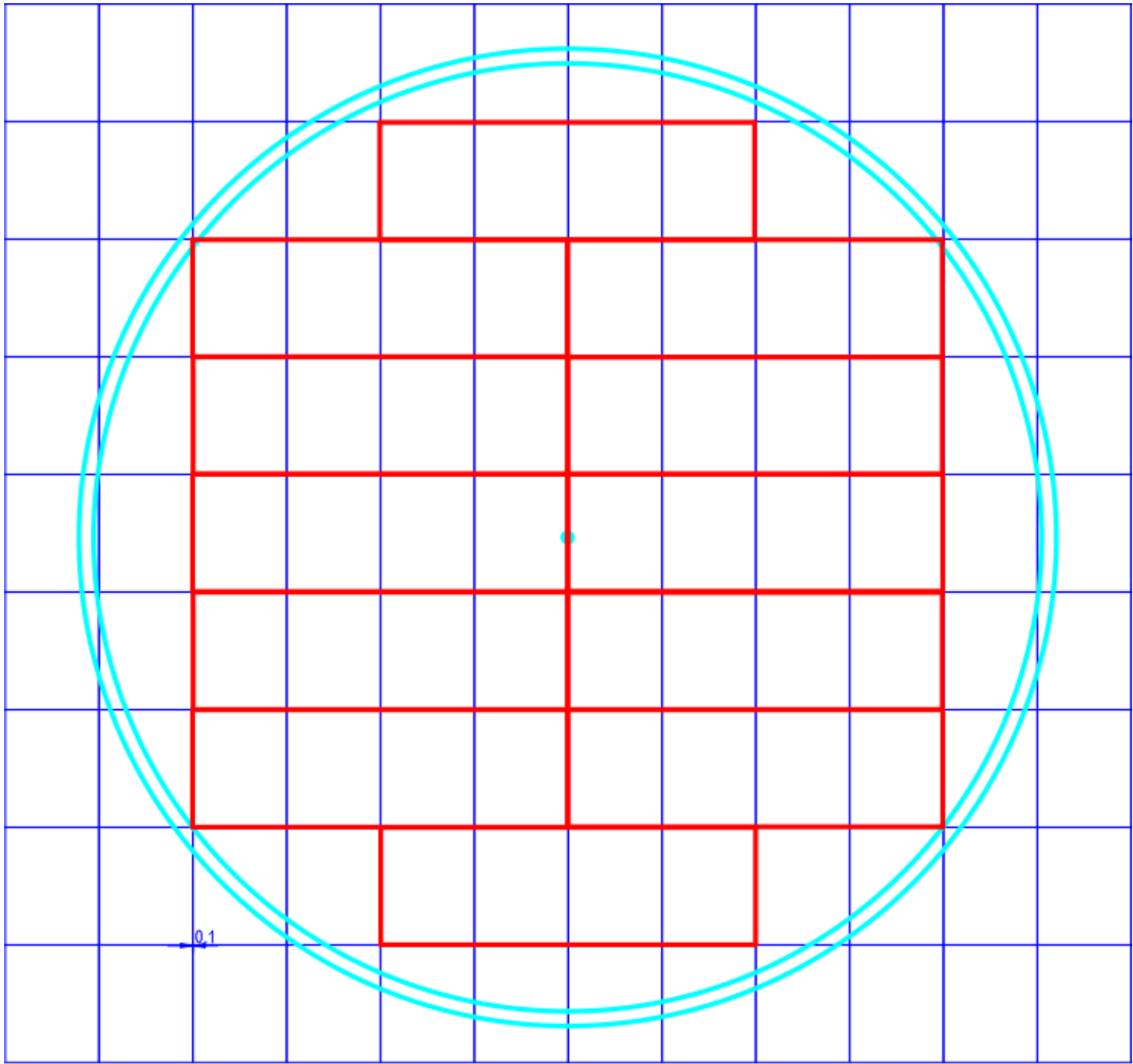
Area Considerations

- Apart from the reticule size which should be either as large as possible or at least “fit” the area read-out by one/two ABCN13, for ease of handling/assembly it was proposed to cut “strips/bars” from the wafer.
- basic idea: try to stay with ~10cm wide objects
  - issue: 8” wafers are ~20cm wide, and we likely have to allow for some edge
    - assume 3 mm of edge here
  - tried with 1.9cm wide reticules and 100um dicing distance between them
    - impossible to place 2 “bars” next to each other even for the middle part → inefficient area usage



Area Considerations

- alternative: reduce to 4 reticules → ~8cm
  - seems that we could nicely fit 12 “bars” on a 8” wafer
  - fairly good area usage
  - but need to get “safe” numbers on edge width and on scribe line width/test structures to be sure
- area usage:
  - ~220 cm^2 used out of (theoretically) ~295 cm^2 (~74%)
    - → ~5-7 kWafers

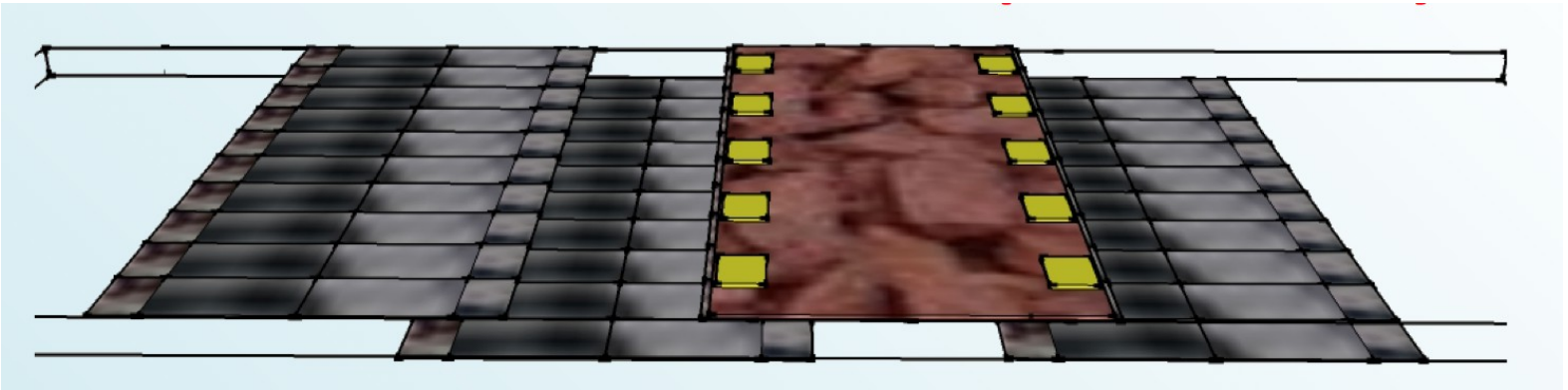


Periphery

- Exact periphery size to be determined by Hervé, but Ivan often suggested ~1% for the comparators and another 1.5% for the encoding.
- Ivan conservatively estimated 1mm on 24mm length (~4%)
- This is in any case **much** less than Alex assumed in his slides (6mm out of 24.5mm or 24%) from a fortnight ago

Conclusions/Wrap-up

- Insisting on 10cm wide objects is leading to bad area usage on an 8” wafer if we are to cut multiple reticules out of it (groups of 2 would not be a problem, of course)
  - is it necessary to keep 10cm stave width? In the TF, I had the impression that we could reduce to 8cm – there will anyhow be several changes for CMOS, it is not a pure “drop-in” replacement
- We should try to minimize the number of ACDCs/connections
  - Don't go to 1cm narrow reticules and increase the number of chips by a factor 2
  - I am (by the way) a big fan of BGA-like industrial bump-bonding to fabricate CMOS-reticules with a 130nm readout chip on top → much more robust and cheaper than wirebonding
- Inefficient gaps between reticules are (IMHO) not bad enough to require overlaps – should follow Alex' “Double Sensor Row” modules



Conclusions/Wrap-up

- For the forward region, we essentially assumed we would ignore the petals and adopt a chessboard-design. Do Petals make any sense for our case? Can we just have half-disks that we populate?
- Have we decided whether to stick with the “lossy fixed-latency encoding” or to go for a time-stamp-based encoding?