Strucutre	Schematic	Group resp.	Time	Layout	Group resp.	Time
Diode	Done	SLAC	0	Done	SLAC	0 day
Amplifier	Done	UCSC	0	To do	UCSC	2 days
Comparator	Done	UCSC	0	To do	UCSC	1 day
Charge injection	Done	UCSC	0	To do	UCSC	½ day
Tune DAC	Done	UCSC	0	Done		0
Analog pixel simulation	To do	UCSC	2 day			
Pixel digital latch	Done	Ivan	5 day	Done	Ivan	5 day
Strip Hit encoding	Done	UCSC	0 day	To Do	UCSC	3 day
Strip Hit encoding simulation	To do	UCSC	1 day			
Pixel analog and digital integration				To do	UCSC	3 day
Full pixel simulation	To do	UCSC	2 day			
Strip encoding	To do	Ivan	15 days	To do	UCSC	5 days
Strip encoding simulation	To do	Ivan	5 days			
Pixels and encoding integration				To do	UCSC	1 day
Pixels and encoding simulation	To do	UCSC	1 day			
Register (Col, Row, Dac)	To do	SLAC	2 days	To do	SLAC	5 days
Pixels and registers integration (decoder, pointers, data bus architecture , memory cell)	To do	SLAC/ UCSC	5 days	To do	SLAC/ UCSC	10 days
Pixels and registers simulation (for 25Kb)	To do	SLAC/ UCSC	3 days			
Global DACs	To do	Ivan		To do	Ivan	
Global DACs simulation	To do	Ivan				
SACi	Done	SLAC	0 day	Done	SLAC	0 day
Control unit + interface	To do	SLAC	2 days	To do	SLAC	5 days
Register/Output multiplexer	To do	SLAC/ UCSC	4 days	To do	SLAC/ UCSC	4 days
LVDS transmitter	Done	SLAC		Done	SLAC	
LVDS receiver	Done	SLAC		Done	SLAC	
LVDS TX/RX simulation	Done	SLAC				
Pad ring	To do	UCSC	1 day	To do	UCSC	2 days
Chip top level integration				To do	UCSC/ SLAC	5 days
Chip level simulation	To do	UCSC/ SLAC	10 days			