

Chess2 Review

May 4th 2015

Configuration and Readout blocks

Pietro Caragiulo on behalf of the SLAC Team



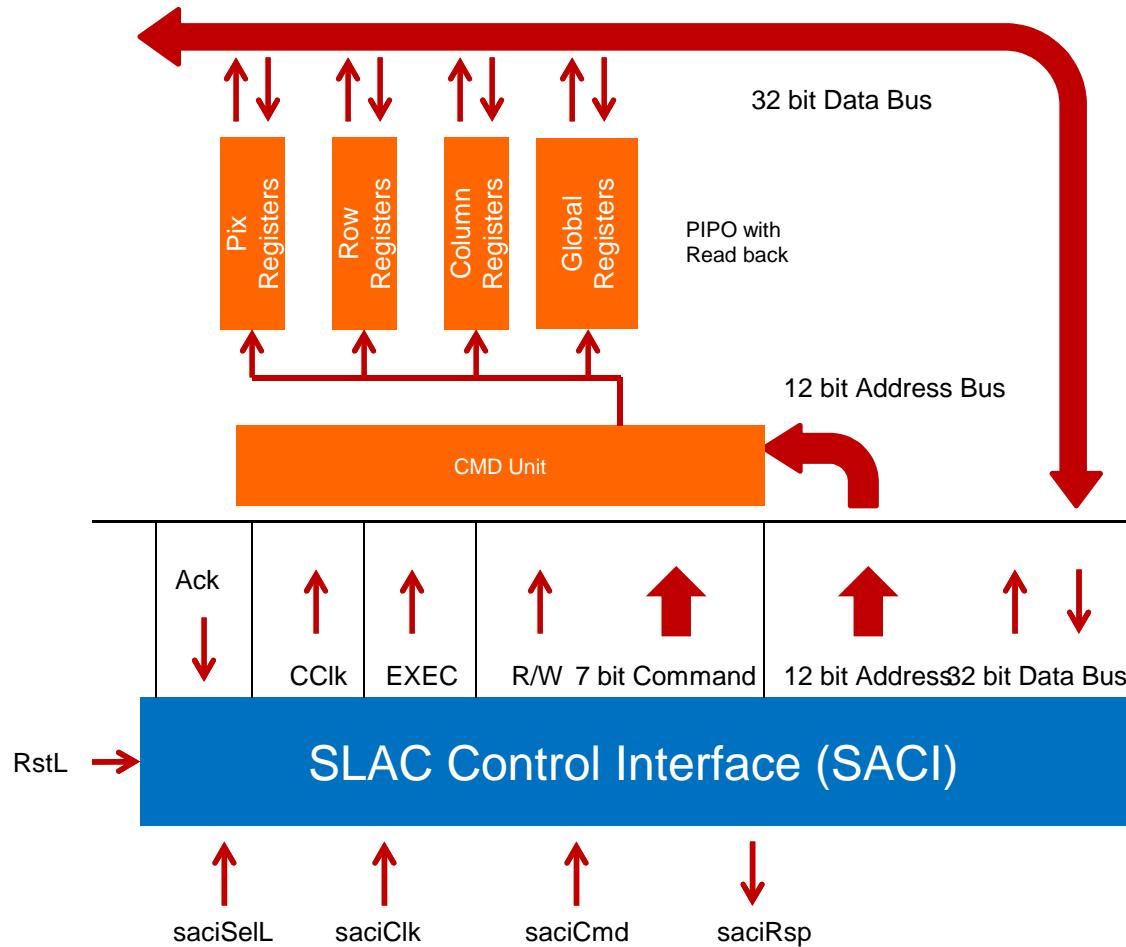
Outline



- Configuration
 - SACI
 - Description
 - Layout
 - Signals
 - Simulations
 - Configuration
 - Commands
 - Pixel Register Configuration
 - Global Register Configuration
 - Pixel Selection for Calibration
 - Read-out
 - Overview
 - LVDS Driver
 - LVDS Receiver

SACI – SLAC ASIC Control Interface

SLAC

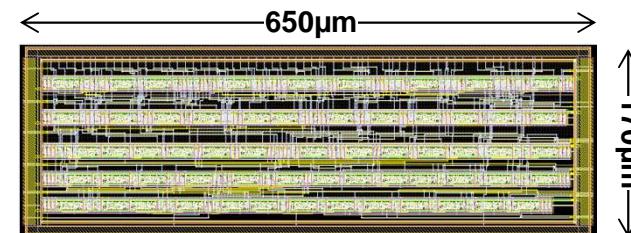


Serial Interface with handshake protocol

5 Signals

- 3 shared: *saciClk*, *saciCmd*, *saciRsp*.
- 1 dedicated select line per slave: *saciSelL*.
- 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.
- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).

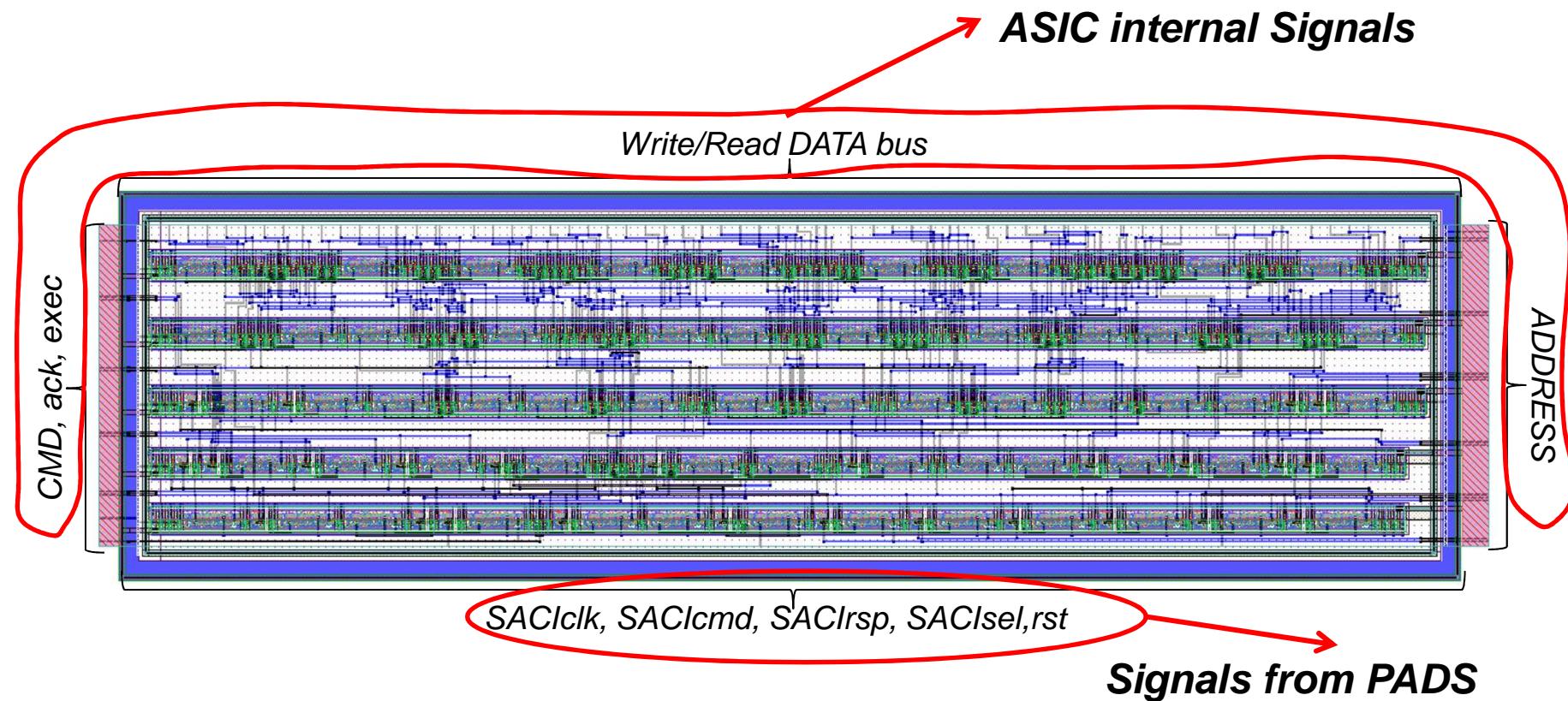
Layout



SLAC ASIC Control Interface (SACI)

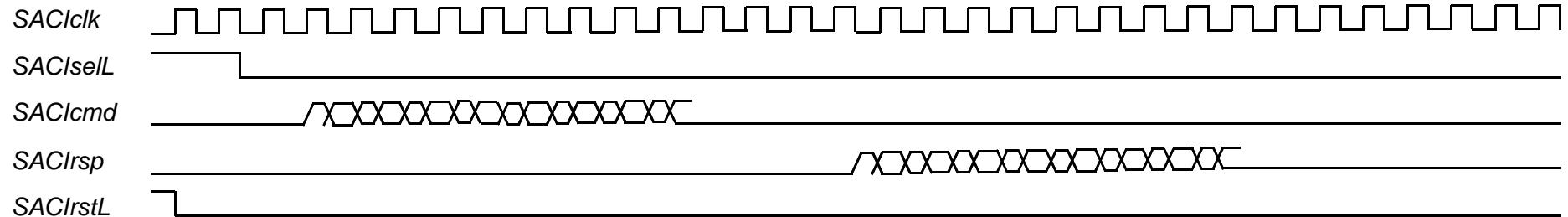
SLAC

SACIcmd (serial signal):



SACI - Signals

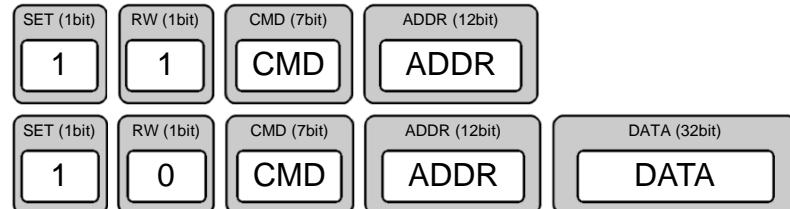
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SACIcmd (serial signal):



SACIrsp (serial signal):



Write Mode

Read Mode

SACI - Simulations

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Inputs to SACI



SACIcmd (serial signal):

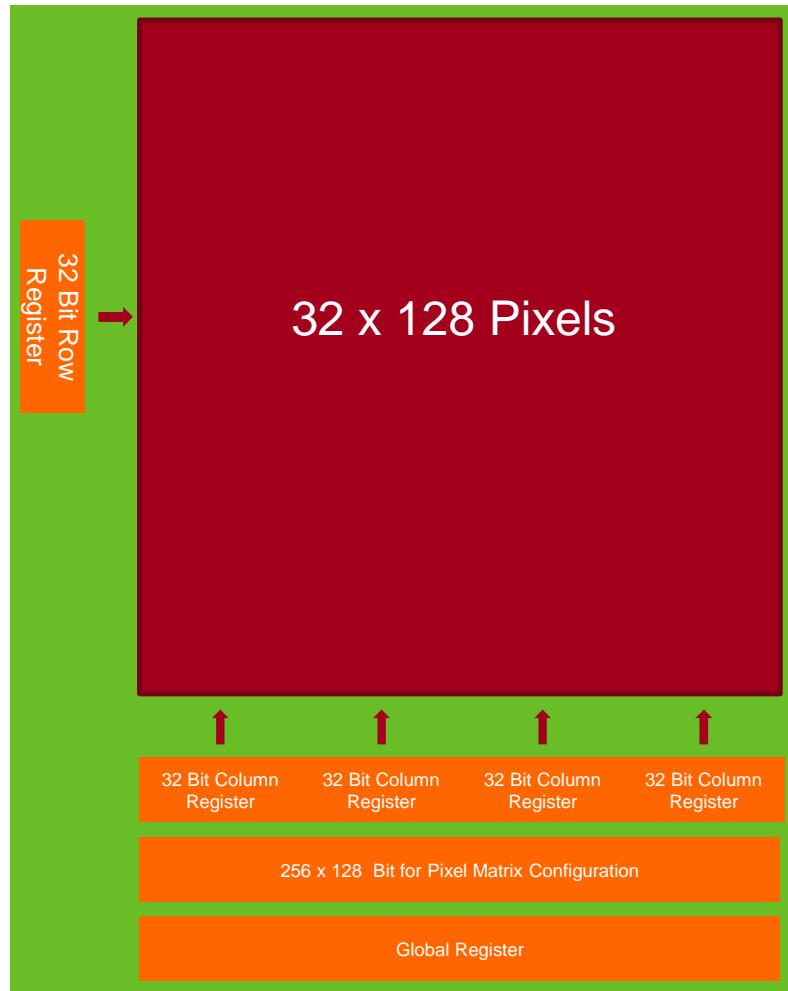


SACI Outputs to the ASIC



SACI – Configuration

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- Pixel Register Configuration
 - Threshold trimming
 - Pixel Masking
- Global Register Configuration
 - DACs Configuration
- Matrix Pixel Selection
 - Calibration

SACI - Commands

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RW	CMD	Function	Clock Cycle
0/1	tbd	Read/Write Global Register	
1	tbd	Write Matrix	
0/1	tbd	Read/Write Pixel	

- The ASIC decoded the command last 4 bits. Any given command longer than 4 bits will be interpreted as a 4 bit command.

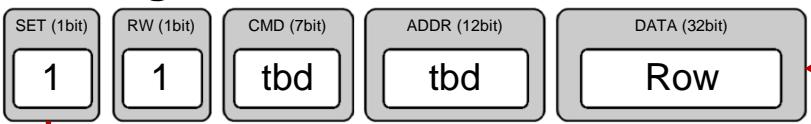
SACI – Pixel Register Configuration

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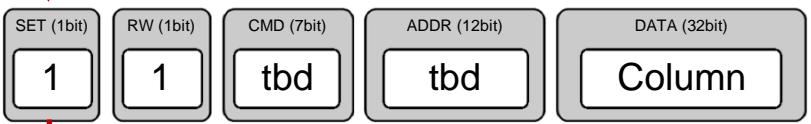


CMD = Prepare for Pixels configuration

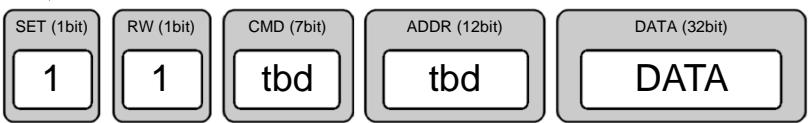
Configure Pixel



Select Row Register and writes address Row

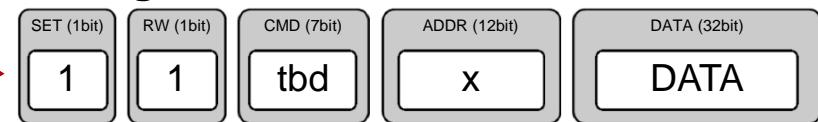


Select Column Register and writes address Column



CMD = Shift data in addressed pixel

Configure entire Matrix



CMD = Select Matrix and shifts data in all pixels

SACI – Configuration – Global Registers

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- WRITE Configuration Registers:



- READ Configuration Registers:



SACI – Configuration – Matrix Pixel Selection for Calibration

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- WRITE Row Registers:

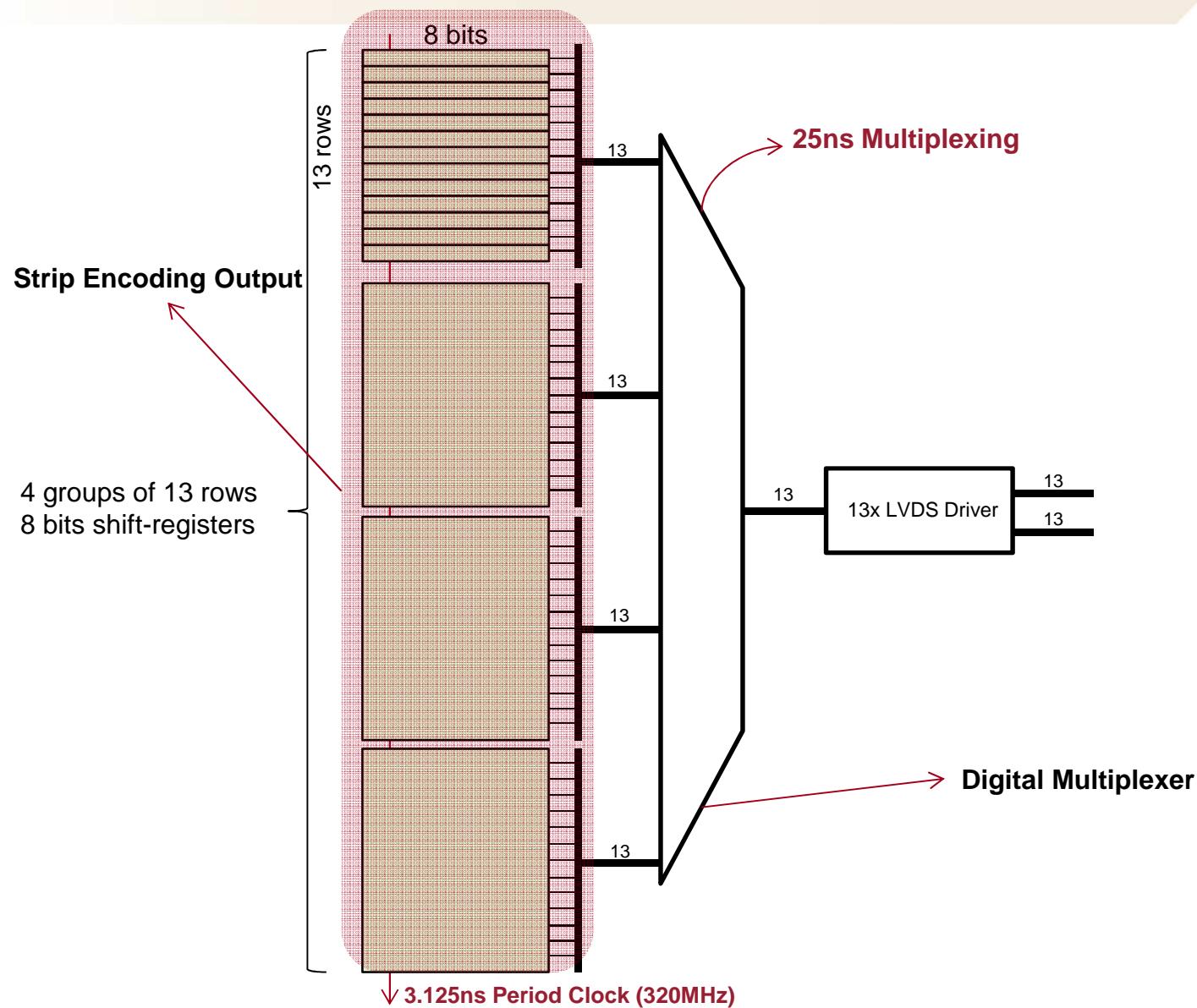


- WRITE Column Registers (x4)



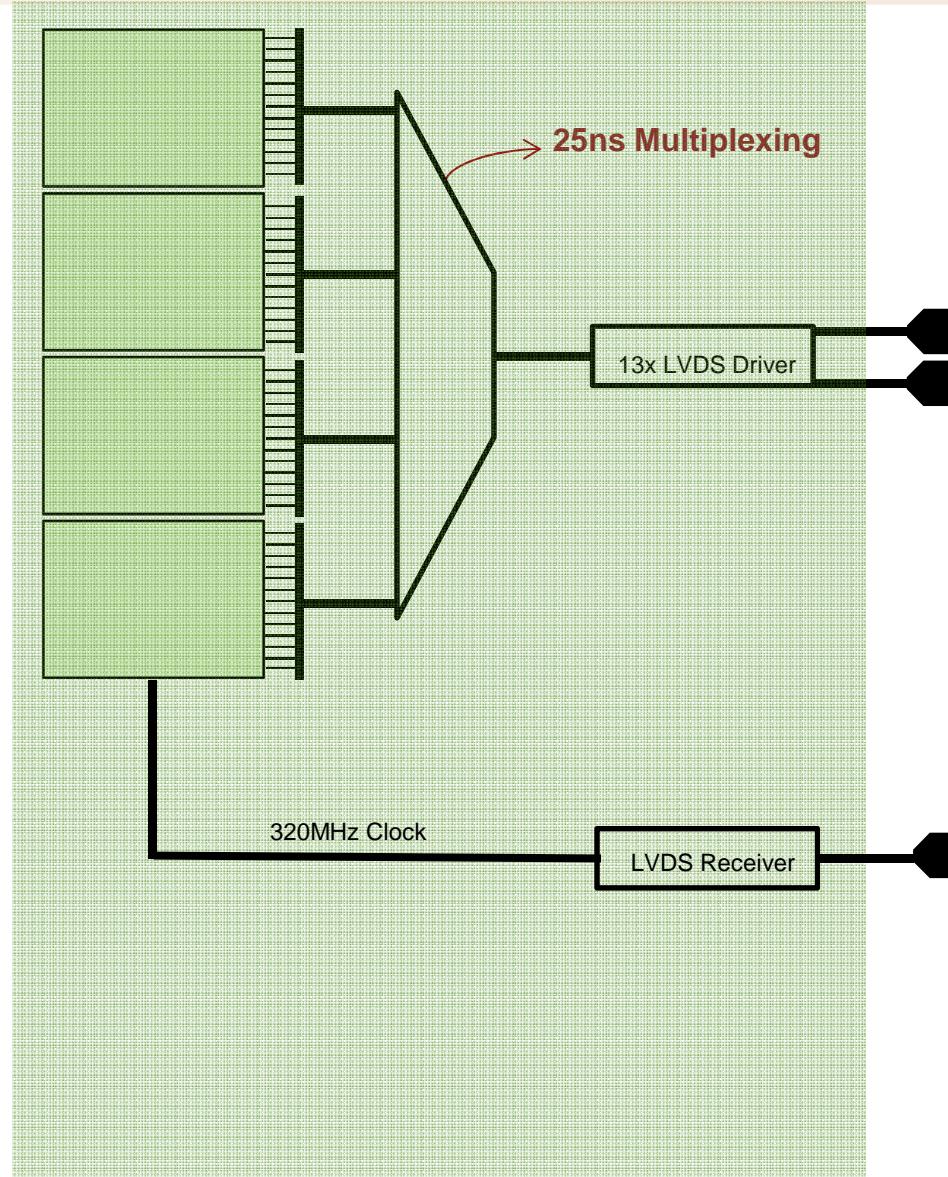
Encoding Read-Out scheme – Overview

SLAC



Encoding Read-Out scheme – Overview

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LVDS Driver – Simulated Performance

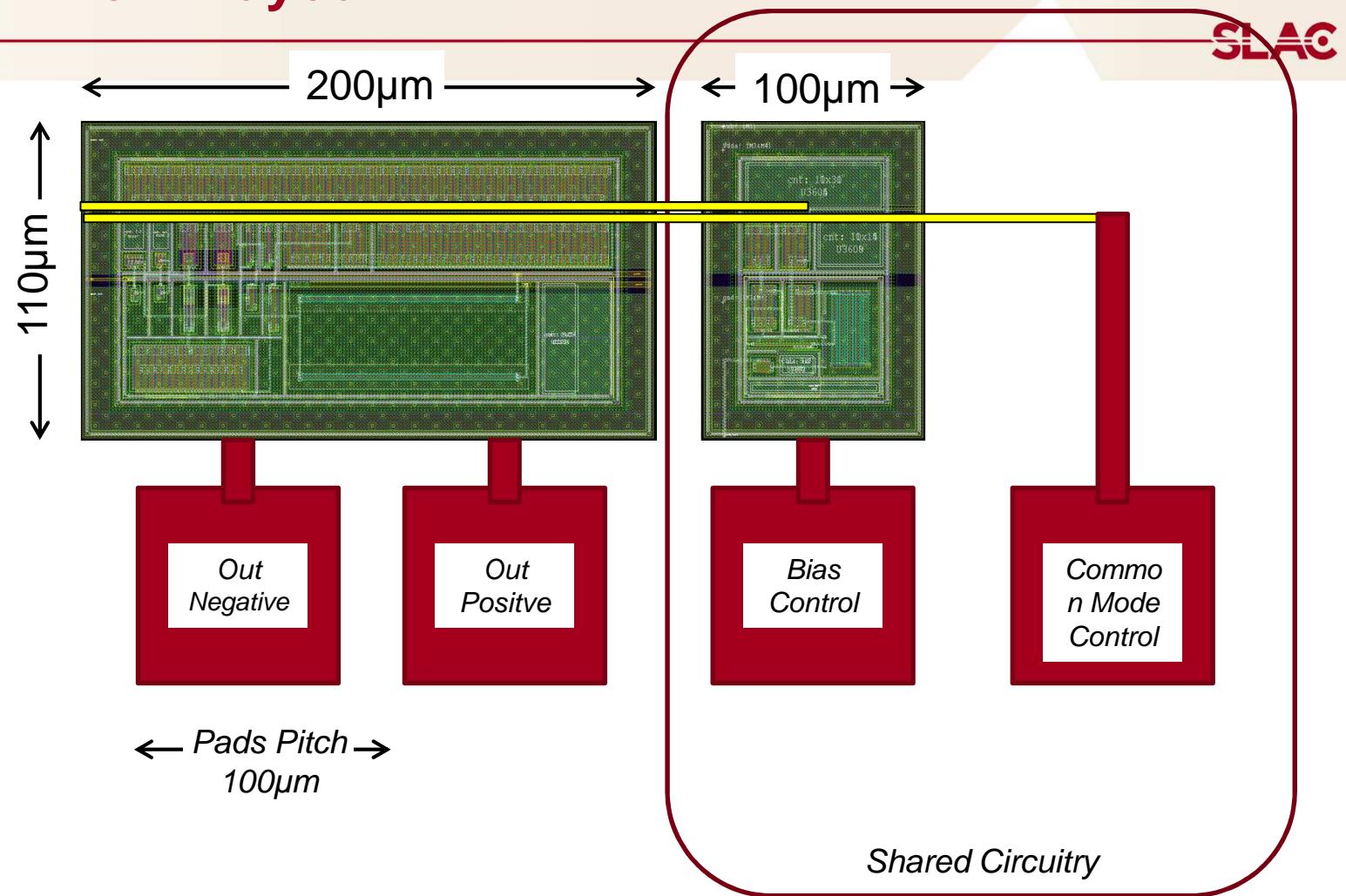


Schematic simulated at all condition (w_o, w_z, w_s, w_p) at room temperature.

Specs	Typical	Min	Max
Differential Output Voltage (@ $R_{LOAD} = 100\Omega$)	600mV		
Output Common Mode	1.2V	0.5	2.8
Current	3mA	0.2mA	3.5mA*
Speed	320MHz		500MHz
Supply	3.3V		

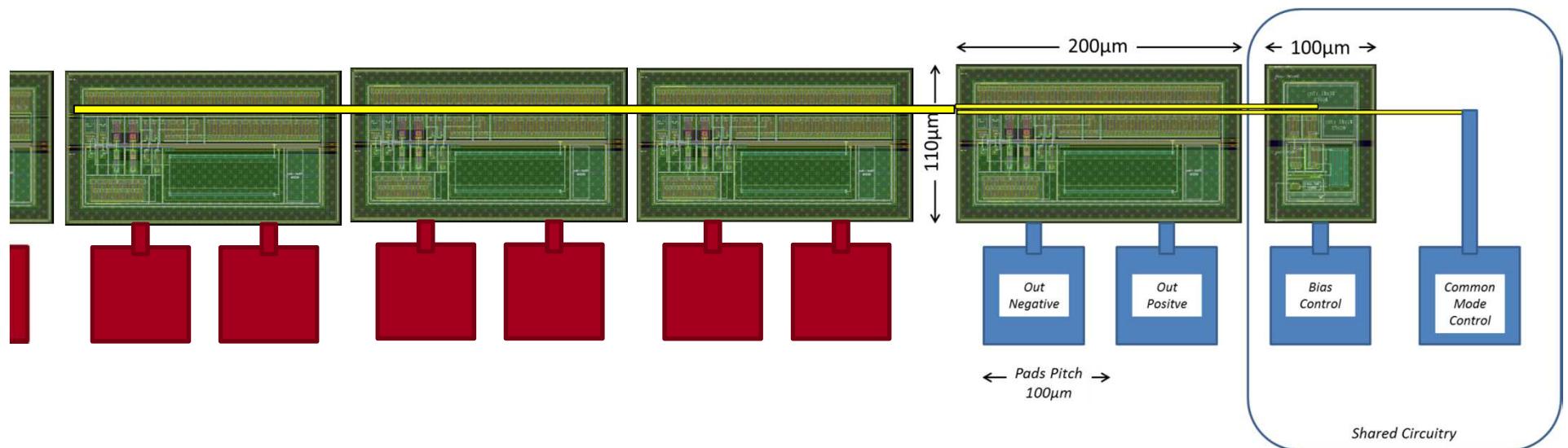
* *Can meet standard LVDS requirements.*

LVDS Driver - Layout



LVDS Driver - Layout

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LVDS Receiver – Simulated Performance



Schematic simulated at all condition (wo,wz,ws,wp) at room temperature.

Specs	Typical	Min	Max
Differential Input Voltage (@ $R_{LOAD}=100\Omega$)	600mV		
Output Common Mode	1.2V		
Input Current	3mA*		
Speed	320MHz		500MHz
Supply	3.3V		

* *Can meet standard LVDS requirements.*

