

HZDE LLRF status report

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Outline

① ELBE

② Status

③ Recent developments

260 MHz Buncher

Real-time BLC

④ Plans for future

Hardware

Software / Firmware

Installation

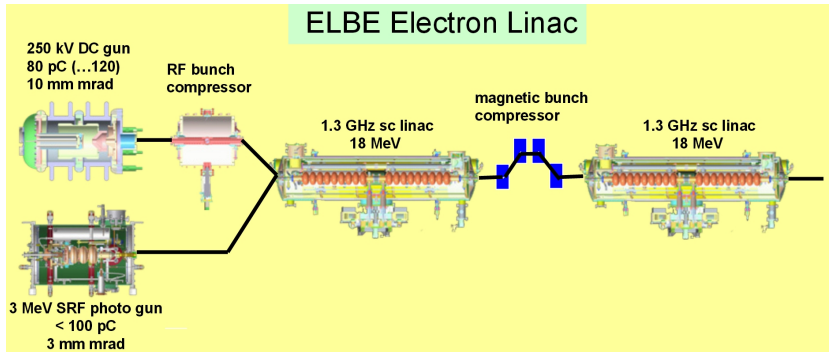
① ELBE

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Layout of ELBE



Source: Peter Michel "ELBE Upgrade ", ARD Workshop February 2013

① ELBE

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(Almost) Done

System

- Closed loop operation verified

Hardware

- Power supply
- MCH / CPU
- SIS8300L2 (digitizer+controller)
- DRTM-DWC8VM1

Firmware

- DRTM-DWC8VM1 BSP
- SIS8300L2 BSP (minor changes expected)
- Controller application (minor changes expected)

① ELBE

② Status

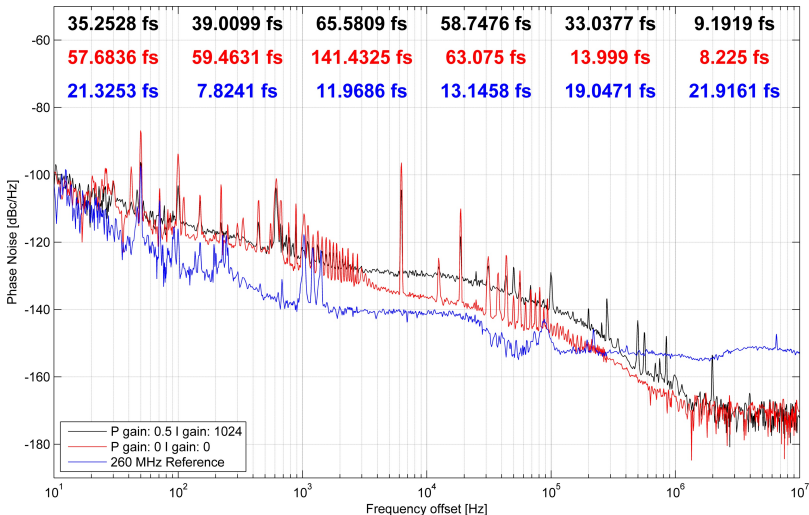
③ Recent developments

260 MHz Buncher

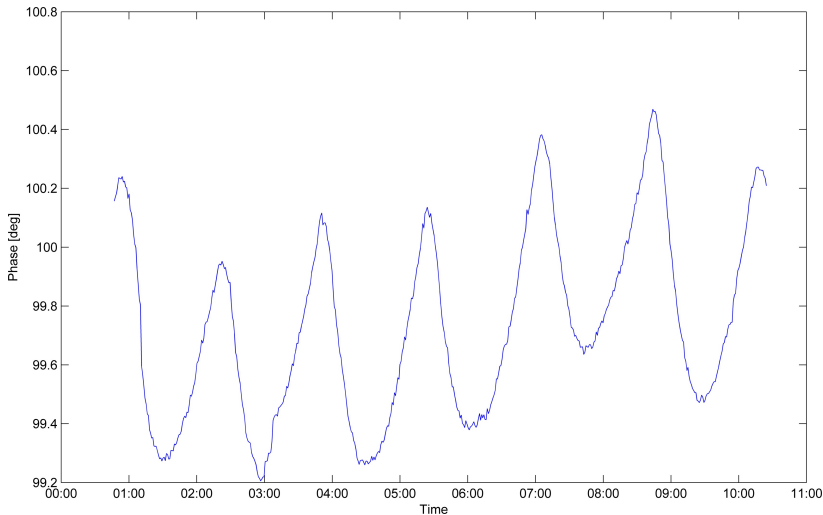
Real-time BLC

④ Plans for future

Results: phase noise

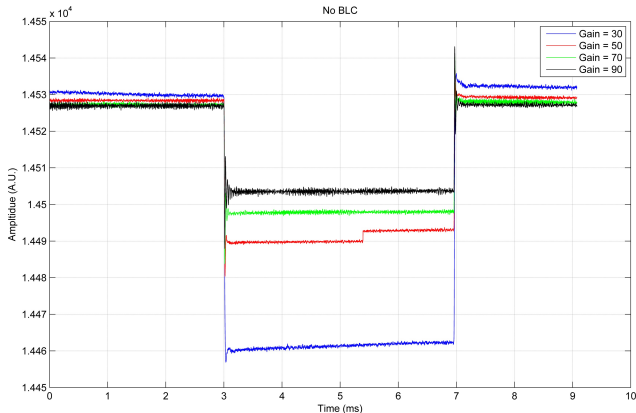


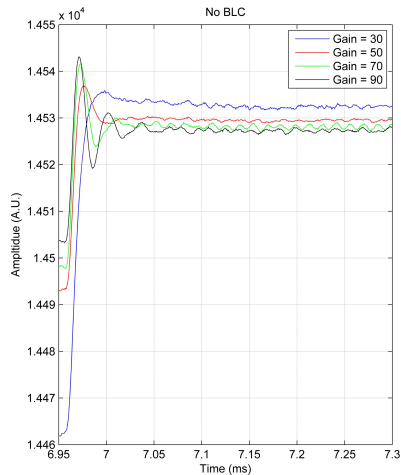
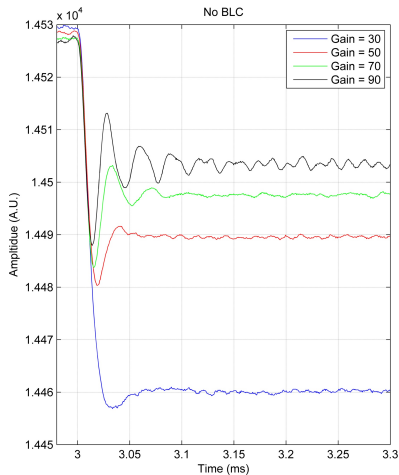
Results: drifts



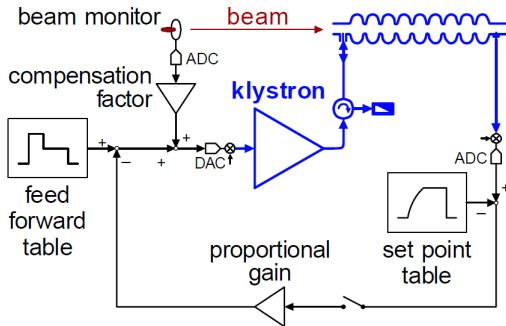
Problem

Control loop react (with a delay) to sudden drop in the gradient.
Proportional controller suppresses the error, but not perfectly. Integral controller can not have doubling time short enough.



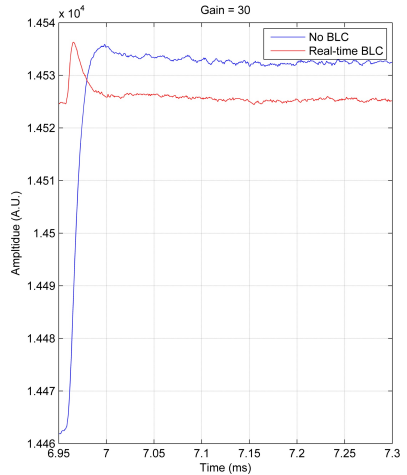
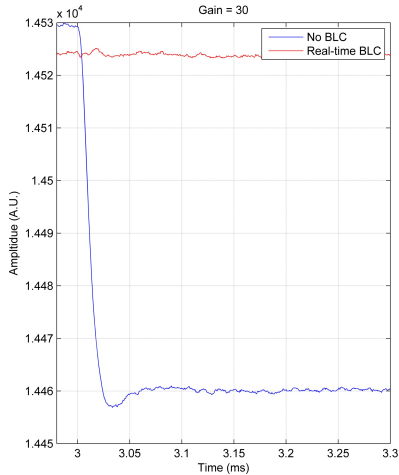


Idea

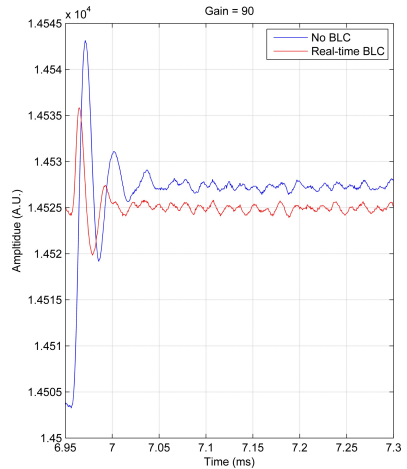
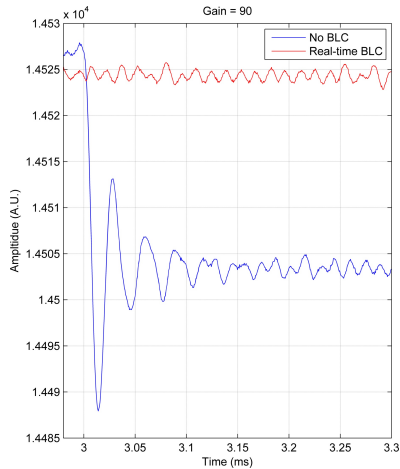


E. Vogel, et al. "Beam loading compensation using real time bunch charge information from toroid monitor at FLASH" (PAC 07)

Results: BLC (Gain = 30)



Results: BLC (Gain = 90)



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Awaiting new revision

- DRTM-DS8VM1

Must be build

- LO Generation Module (UNILOGM)
- Reference distribution box

Needs implementation

- Timing / Interlock module

Firmware

- A BSP for the DRTM-DS8VM1 must be implemented.
- Access to the source code must granted by Holger Schlarb.

Software

- API specification from Martin Killenberg.
- Adaptor to be developed for HZDR.

Rack occupation

A drawing should be prepared.

Cabling

To be done after the LO Generation and Reference distribution modules are build. Low drift cables preferred.

Training

HZDR's stuff must be trained.

Questions

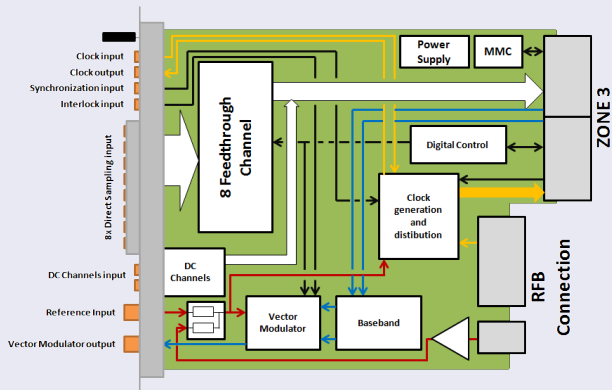


Thank You for attention!

DRTM-DS8VM1

Designed for direct sampling of low frequency signals
2nd revision (major changes)

Block diagram



Analog front-end

