HR-CHESS2 update

D. Das, R. Turchetta, STFC-RAL, UK
26/05/15

Science & Technology Facilities Council
Technology

Specifications

Close to HR-CHESS spec (Physics requirements!)
Specifications below for one block

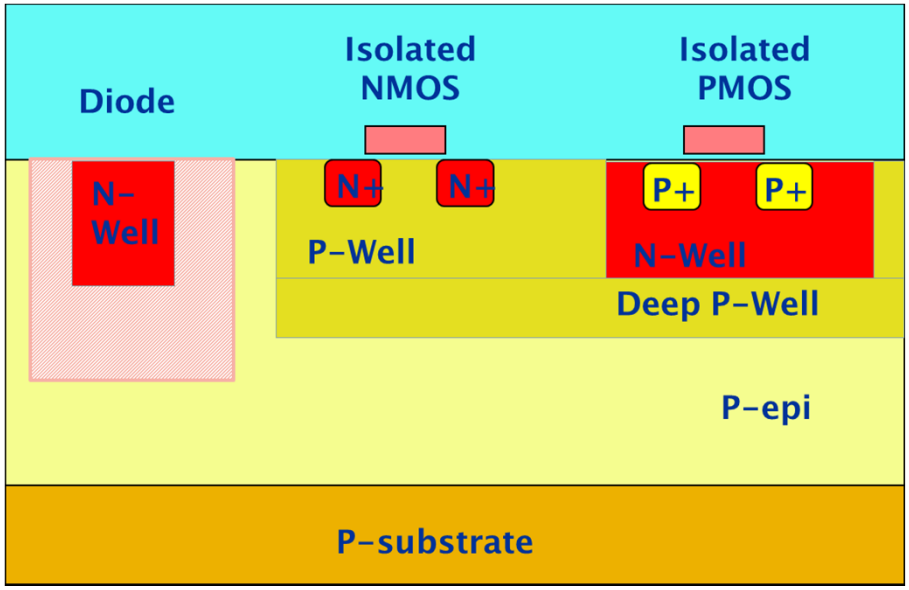
Technology: TowerJazz 180 nm
Voltage supply 1.8/3.3V
Wafers: epitaxial
Epi resistivity/thickness: up to 25um/up to >1kOhm cm *
Segment size: 40umx800um (Segments could contain smaller pixels *)
Number of strips: 128
Number of segments per strip: 32
Readout speed ≥ 320 Mbit/sec
Output buffers: LVDS with adjustable bias current and CM level
Maximum number of hits per strip: 1 + overflow flag
Maxcimum number of hits in block: 8
Size of data output per strip: 13 bits
Format of data output: 5 (segment) + 1 (segment overflow flag) + 7 (strip address) bits

* pending results from HR-CHESS1

Science & Technology Facilities Council
Technology

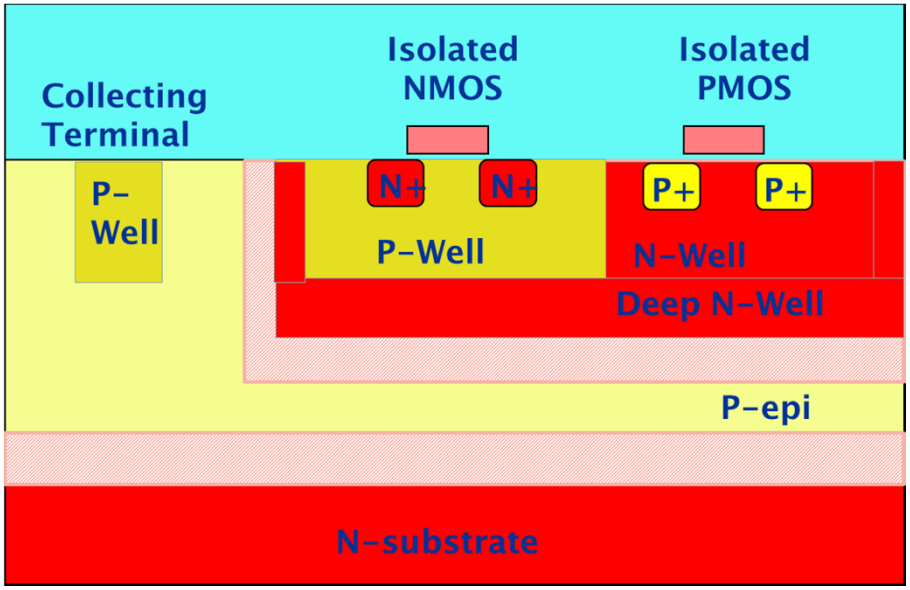
Wafer types

P on P
aka P epi on P substrate



Conventional
Depletion starting from collecting N-well

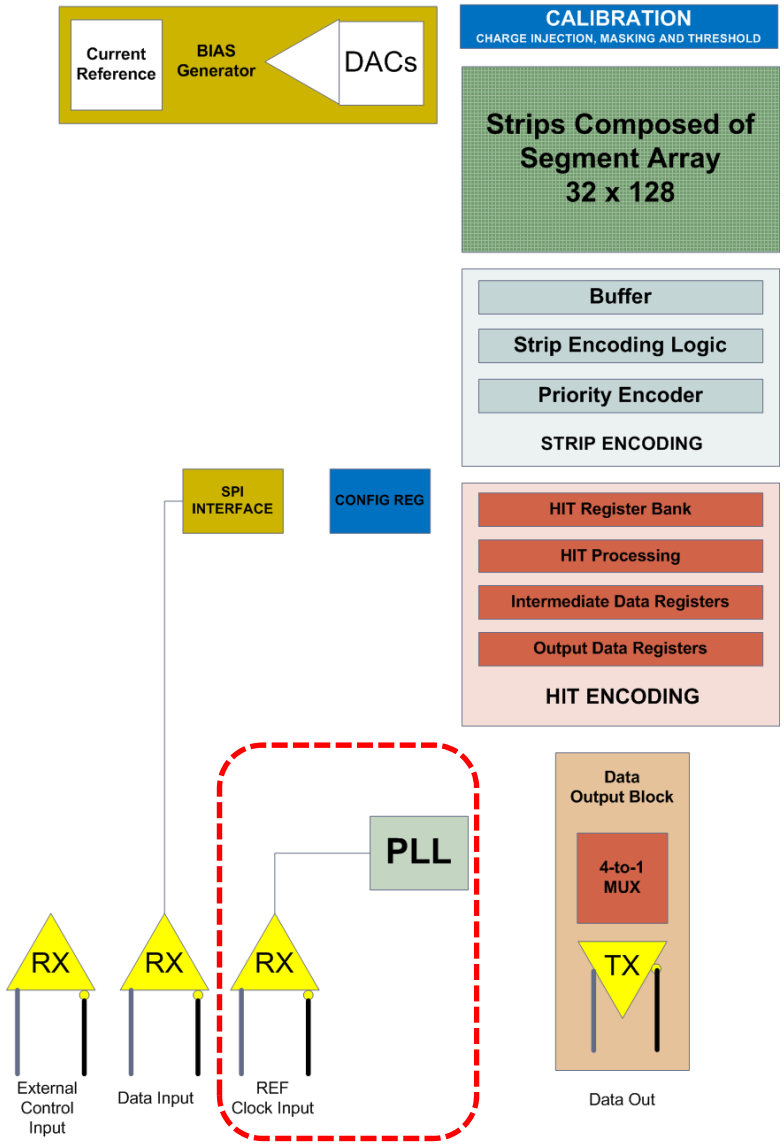
P on N
aka P epi on N substrate



New
Depletion starting from deep N-well and N substrate

Science & Technology Facilities Council
Technology

Architecture Demo Chip Block Diagram



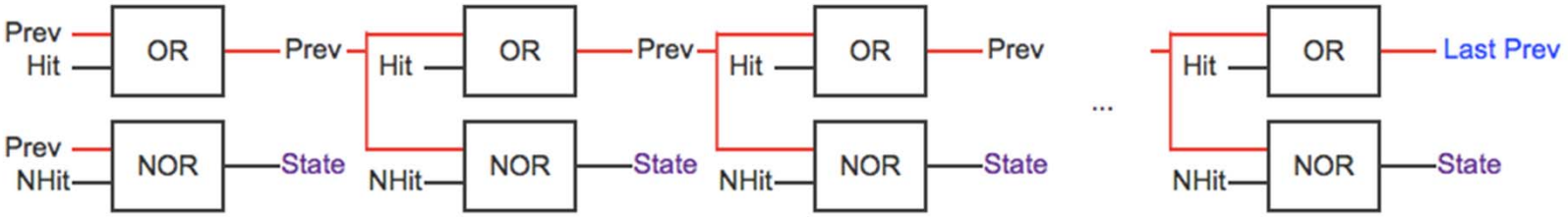
Science & Technology Facilities Council
Technology

Strip Encoding

We plan to follow the HR-CHESS scheme. See below drawings from their design review. Not yet implemented. Using 180 nm so speed should be fine.

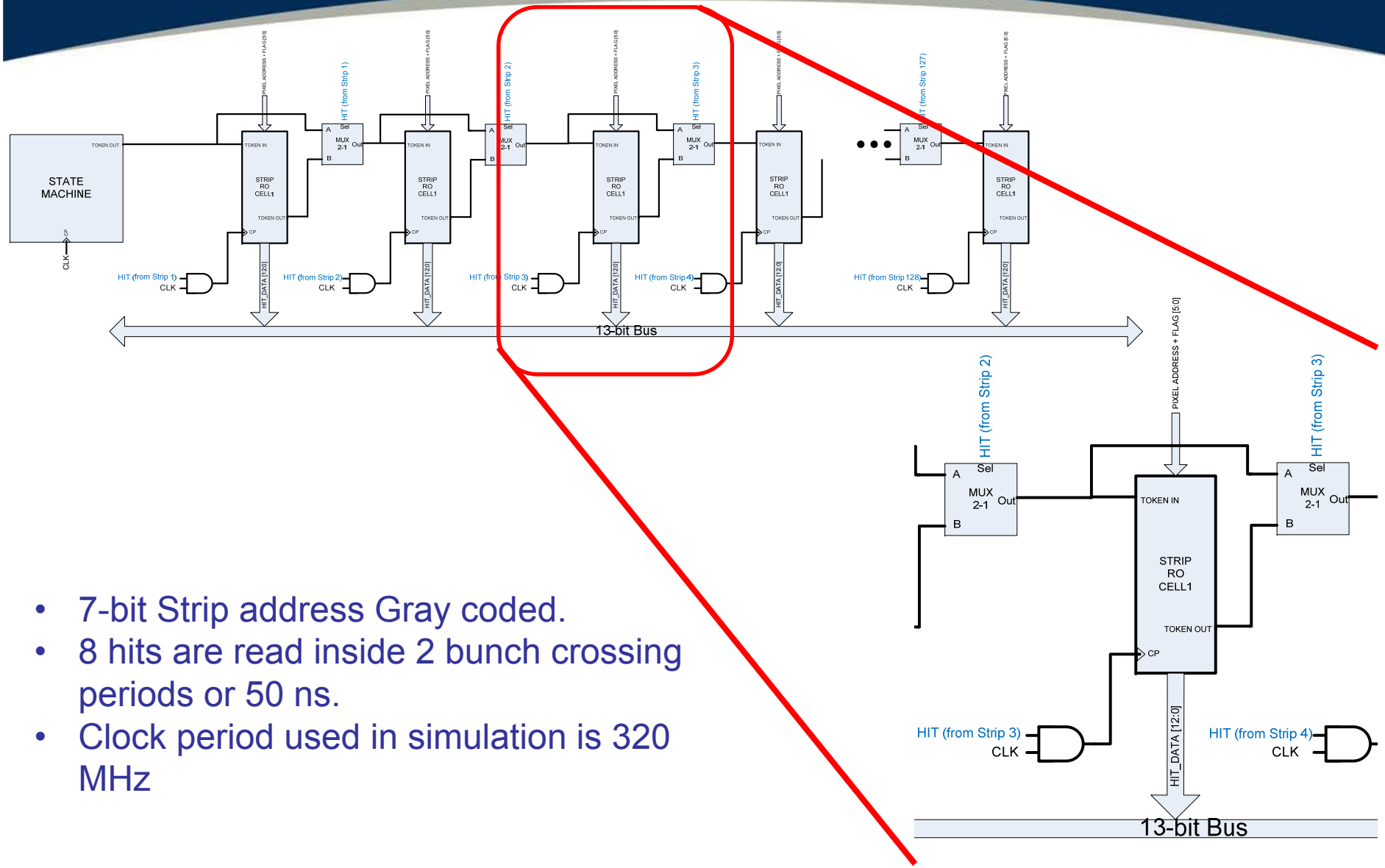
- Single hit in the strip
  - Encoded position of the first hit
- Double or multiple hits in the strip
  - Encoded position of the first hit + Flag

- The first hit in the strip is encoded on **5bits**
- Additional hit **Flag** is raised in case of multiple hits.
- **Flag** provides loose information on the position of the additional hits.
- During strip encoding an internal bit is also raised when the strip is hit.



Science & Technology Facilities Council
Technology

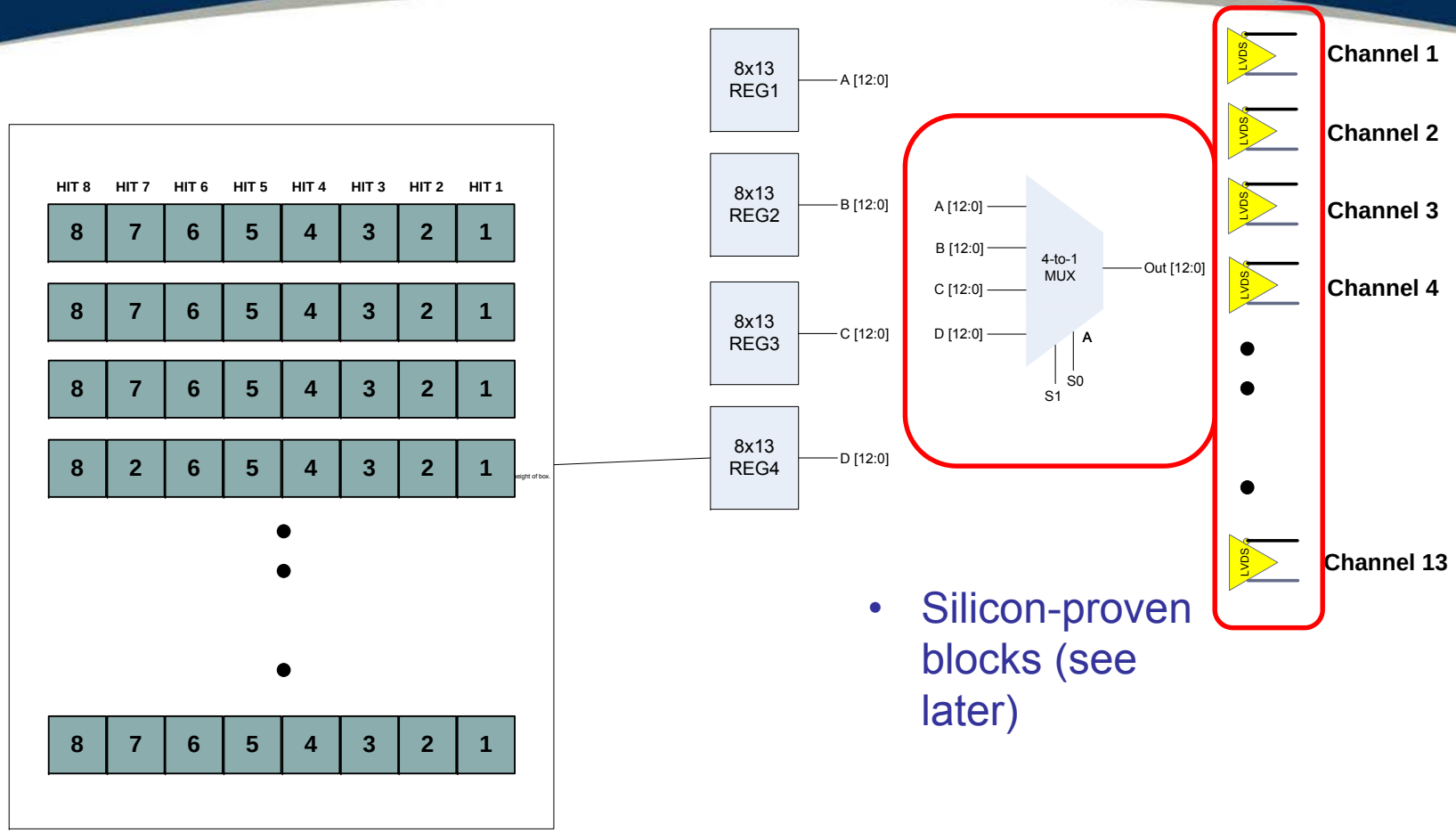
Hit Encoding Functional Block Diagram



- 7-bit Strip address Gray coded.
- 8 hits are read inside 2 bunch crossing periods or 50 ns.
- Clock period used in simulation is 320 MHz

Science & Technology Facilities Council
Technology

Data Output Block



- Silicon-proven blocks (see later)

- 4.16 Gbits/sec total data-rate
- Each LVDS channel operates at 320 Mbits/sec (single data-rate)
- Read-out 104-bits in 25 ns
- Reference clock for sync to be added (not shown here)

Science & Technology Facilities Council
Technology

HIT READOUT ILLUSTRATION

HIT READOUT ILLUSTRATION FOR 6 BUNCH CROSSINGS (BC)

		25ns	50ns	75ns	100ns	125ns	150ns	175ns	200ns	225ns
	BUNCH CROSSINGS (BC)	BC1	BC2	BC3	BC4	BC5	BC6			
ODD BUNCH GROUP	128-bit REG	REG1	RESET	REG1	RESET	REG1	RESET	REG1	RESET	REG1
EVEN BUNCH GROUP	128-bit REG	RESET	REG2	RESET	REG2	RESET	REG2	RESET	REG2	RESET
ODD BC	HIT PROCESSING BLOCK 1		PROCESS BC1		PROCESS BC3		PROCESS BC5		PROCESS BC7	
EVEN BC	HIT PROCESSING BLOCK 2			PROCESS BC2		PROCESS BC4		PROCESS BC6		PROCESS BC8
ODD BC	8x13-bit INTERMEDIATE REG1		STORE BC1		STORE BC3		STORE BC5		STORE BC7	
EVEN BC	8x13-bit INTERMEDIATE REG2			STORE BC2		STORE BC4		STORE BC6		STORE BC8
	8x13-bit OUTPUT REG1				READ BC1				READ BC5	
ODD BUNCH GROUP	8x13-bit OUTPUT REG2					READ BC2				READ BC6
	8x13-bit OUTPUT REG3						READ BC3			
EVEN BUNCH GROUP	8x13-bit OUTPUT REG4							READ BC4		
	OUTPUT				BC1	BC2	BC3	BC4	BC5	BC6
		LATENCY = 75ns			**OUTPUT 8 HITS PER BC PERIOD**					

IF LESS THAN 8 HITS IN ANY BC PERIOD THEN FILL WITH '1' TO DENOTE BLANK HITS

- Schematic completed for 128 strip hit encoding block
- Layout partly done and simulated

Science & Technology Facilities Council
Technology

High-speed output

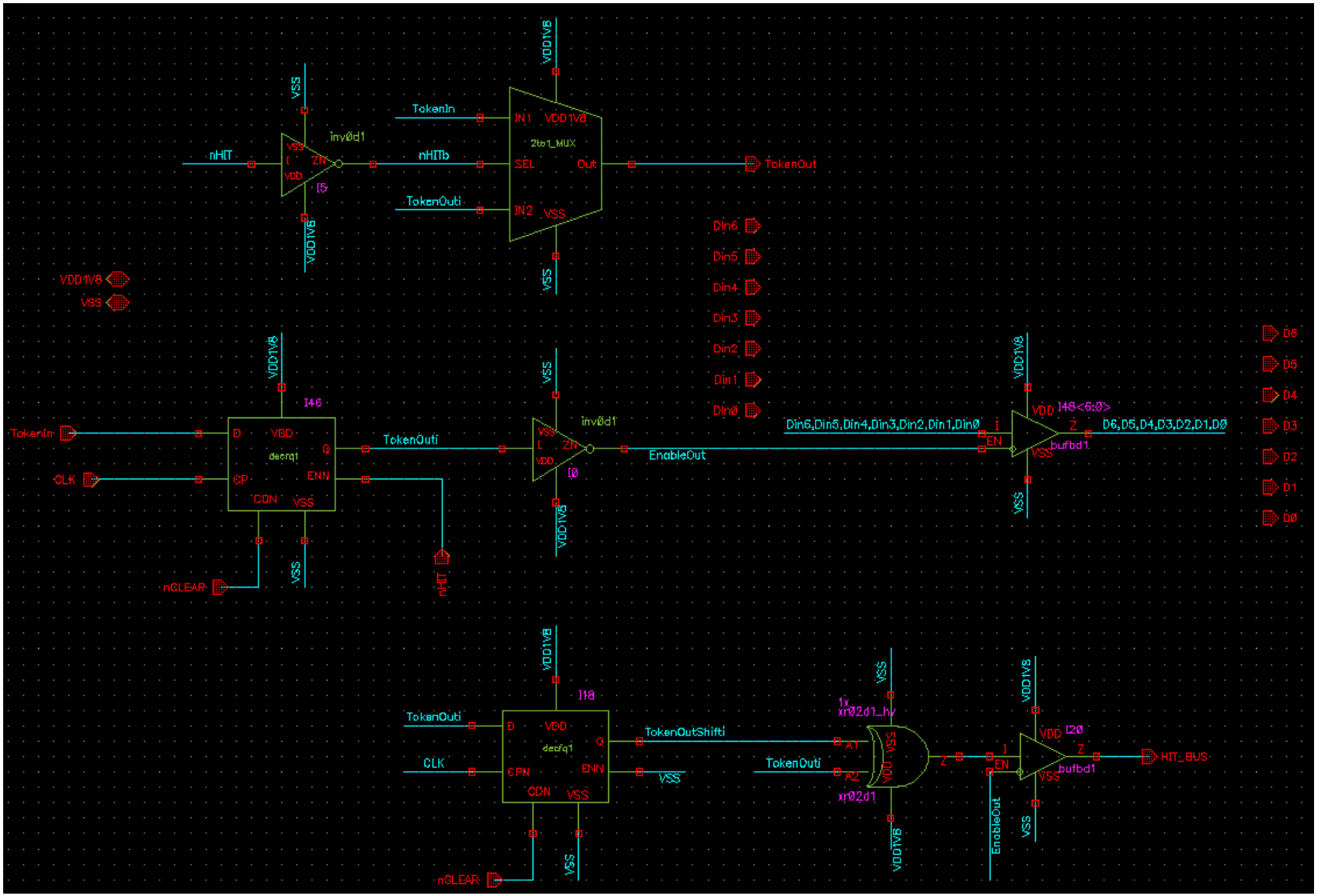
- High-speed 4:1 mux already characterised. 1.8V transistor only → rad-hard
- LVDS RX-TX already characterised. Some 3.3 V transistors. To be be tested for rad-hard. Might need to re-design 3.3V in enclosed geometry
- LVDS-TX specs:
  - Differential input voltage (@Rload = 100 Ω) = 600 mV
  - Output CM = 1.25 V, adjustable
  - Output current = 3 mA
  - Input current ~ 300 μA, adjustable
  - Supply = 2.5 V
  - Speed up to 800 Mbit/sec (double data rate)

Science & Technology Facilities Council
Technology

Backup

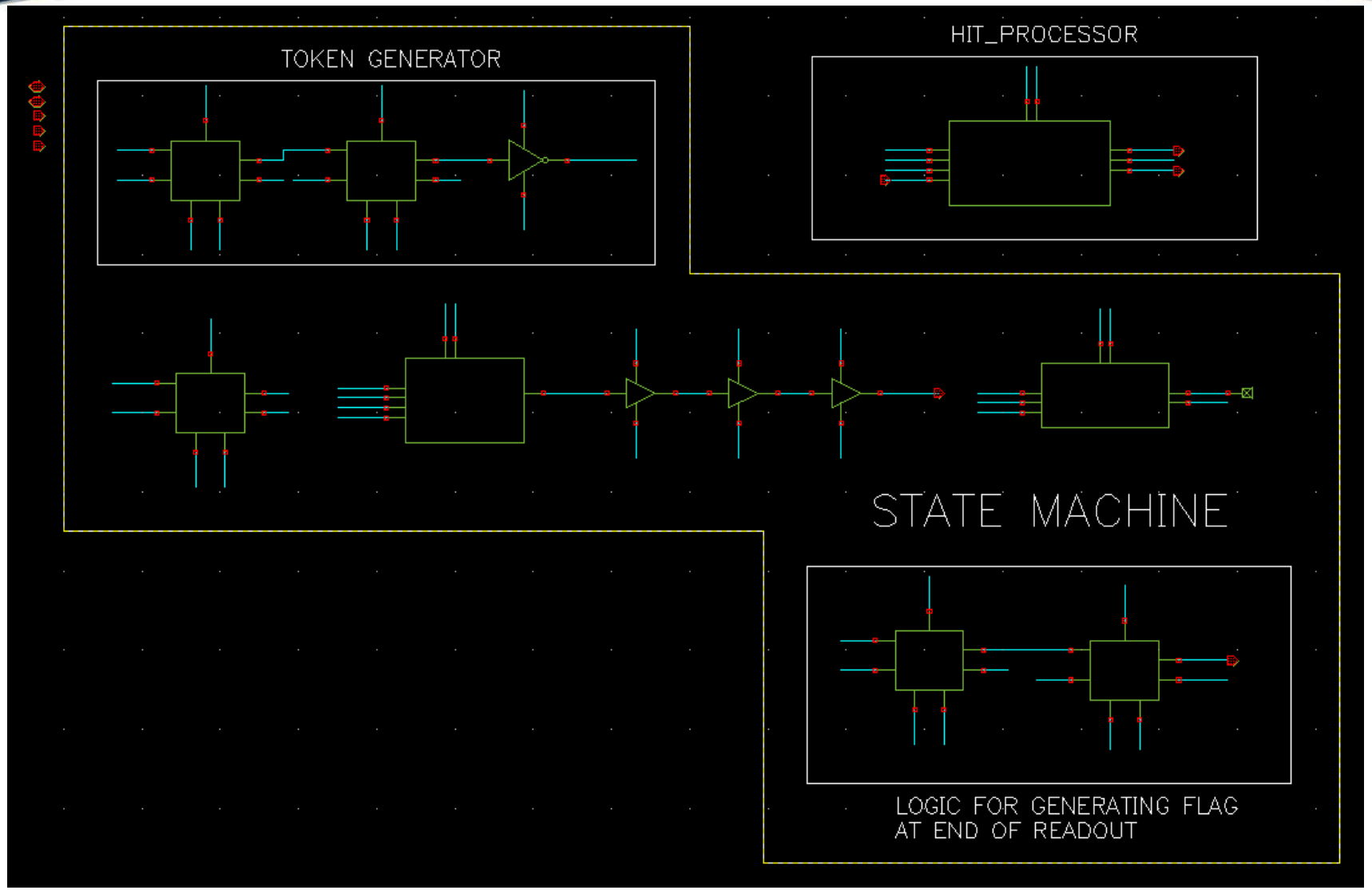
Science & Technology Facilities Council
Technology

STRIP Readout Cell With Fast Skip Logic



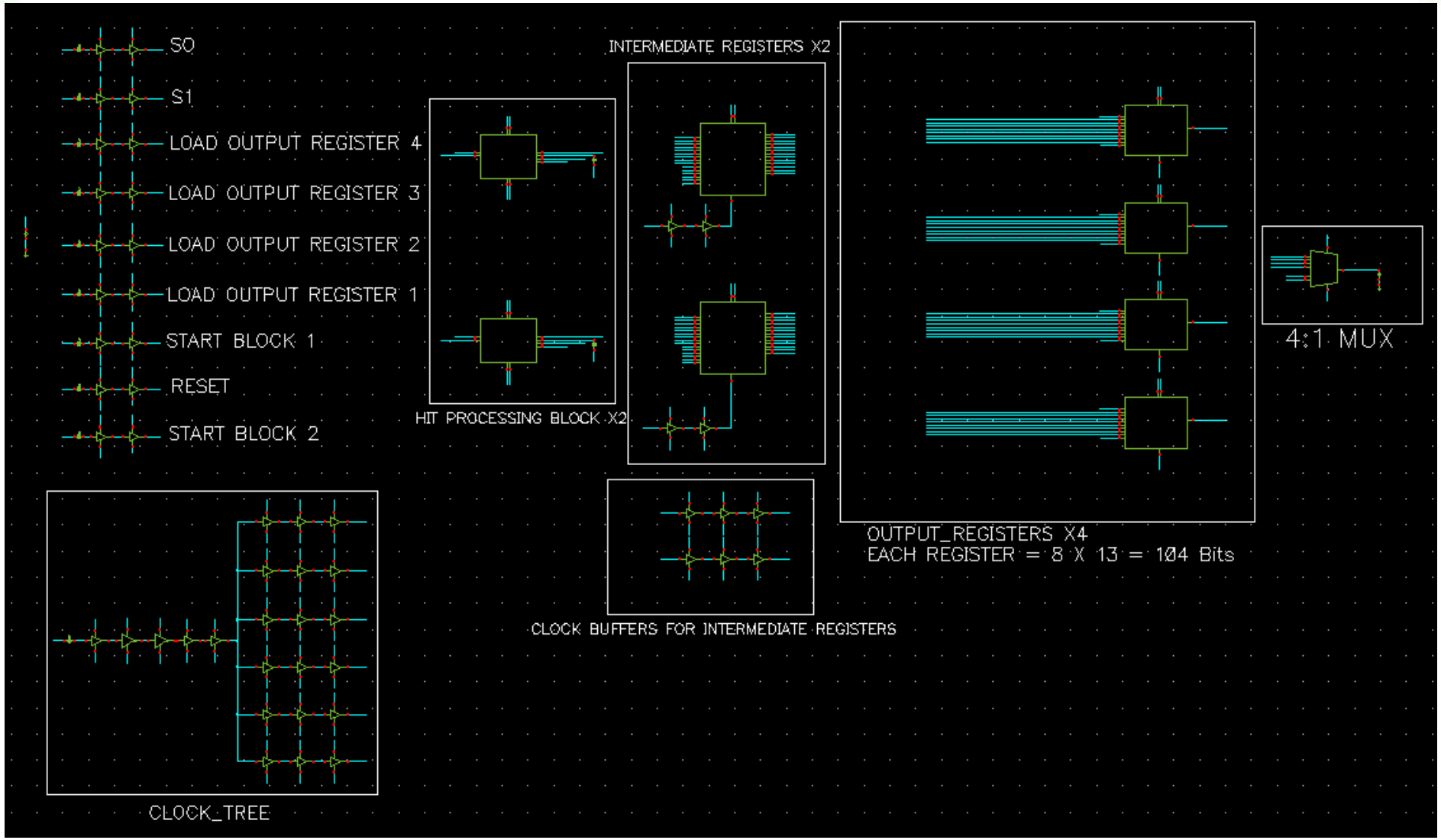
Science & Technology Facilities Council
Technology

HIT Processing Block



Science & Technology Facilities Council
Technology

Digital HIT Readout Block



Science & Technology Facilities Council
Technology

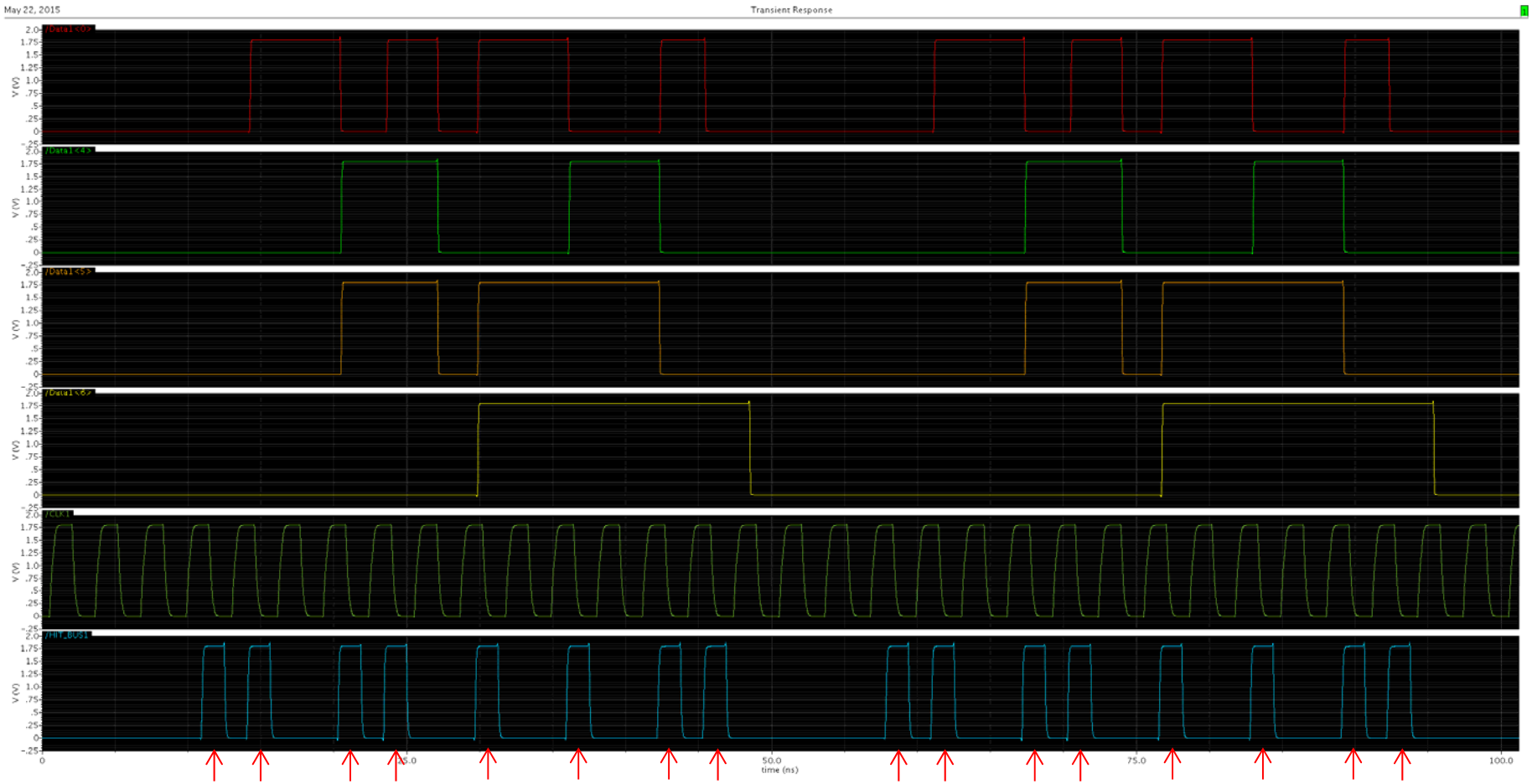
Strip HIT Detect & Address Simulation

- We simulated the schematic of the whole HIT Readout Block.
- Hard coded 8 Hits in the 127 strip array.
- 7-bit Strip address Gray coded.
- Goal is to read out these 8 hits and output their address inside 2 bunch crossing periods or 50 ns.
- Clock period used in simulation is 320 MHz
- The Hit addresses corresponding to each bunch crossing are then stored and readout through LVDS stages every 25 ns.
- Table below shows the Hit locations and corresponding 7-bit Strip address (Gray coded).

Hits	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0	Strips
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	32
4	0	1	1	0	0	0	1	33
5	1	1	0	0	0	0	1	65
6	1	1	1	0	0	0	0	95
7	1	0	0	0	0	0	1	126
8	1	0	0	0	0	0	0	127

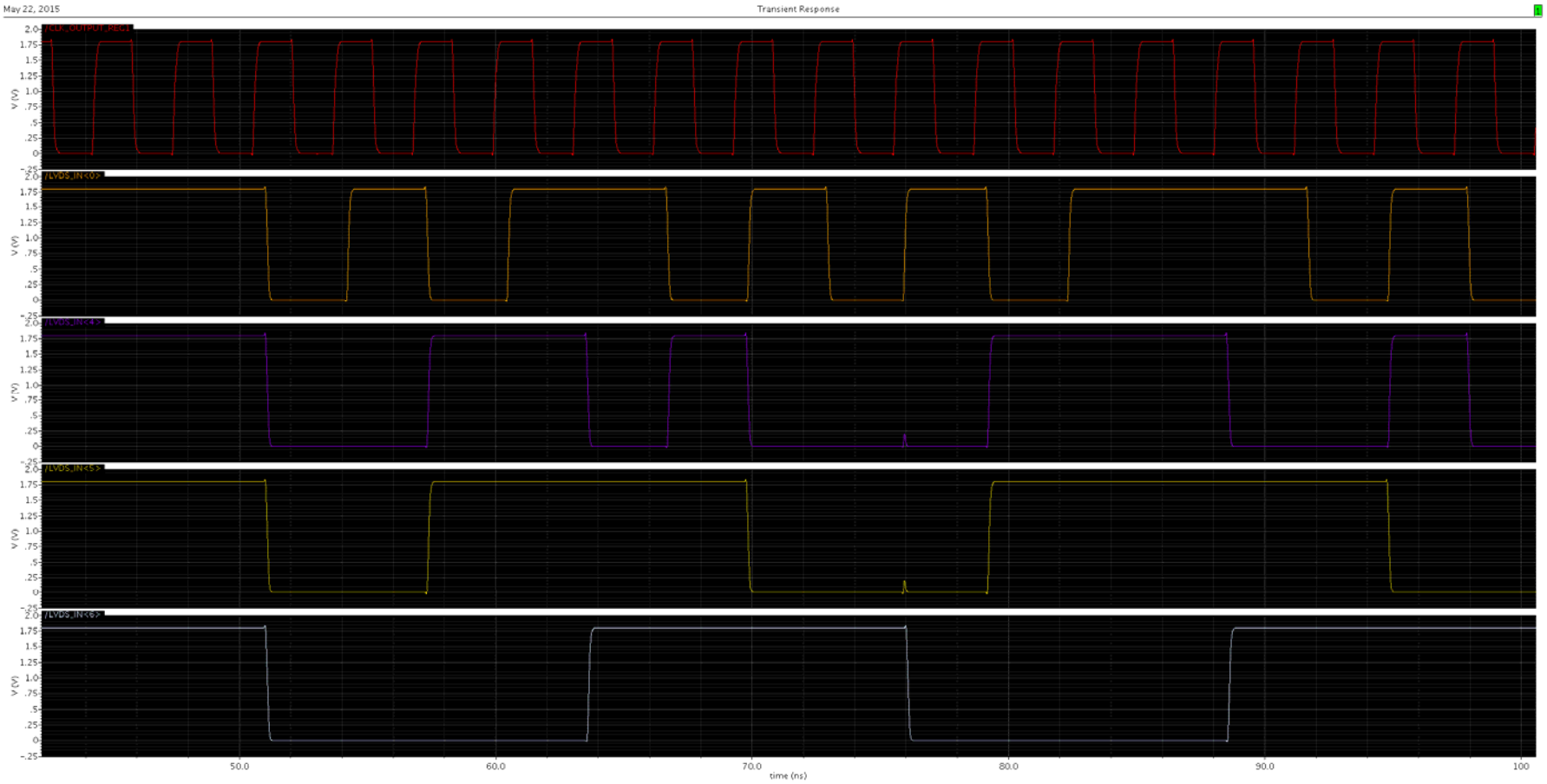
Science & Technology Facilities Council
Technology

Strip HIT Detect & Address Simulation



Science & Technology Facilities Council
Technology

Strip HIT Detect & Address Simulation – Input to LVDS



Strip: 0 1 32 33 65 95 126 127

Science & Technology Facilities Council
Technology

Technical Specification
Final Sensor

Additional Requirements

On top of the above, the sensor will also require the following features.

- Configuration Register
- Calibration (0.5fF capacitors per segment for charge injection)
- Comparator 4-bit threshold trimming
- PLL with mux to select external clock source
- SPI (serial command decoder for minimal pin count)
- Analogue pre-amp channel output for monitoring one channel
- Segment masking
- LVDS current control to save power
- Provisions to test CMOS data output transmission