Optimizing the built-in amplifier in HV-CMOS CHESS1

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Isolated amplifier in CHESS1 chip

- HV-CMOS CHESS1 chip has built-in isolated amplifiers
- designed to optimize amplifier performance
  - Six amplifier biasing control
  - Optimization can be done with pulser, without using laser injection or beta source.
  - Change its gain and output signal shape by changing biasing control
- Try to study the amplifier performance as input to CHESS2 design

Table 3.4-e: Fast Amplifier Biasing for optimum performances

Pad number	Pad name	Value
1	iN	65µA
2	Casc	2.4V
3	VPload	1.85V
4	iBias	7nA
5	iFB	2nA
6	iNSF	20nA

3.5. Isolated Fast Amplifier

An array of 7 isolated fast amplifiers circuits is included with an input and out pad. This is to separately test the characteristics of the amplifier in order to separate its characteristics and their evolution with radiation from that of the passive pixel sensors. The amplifier used is the same as the one included in the active pixel array. However instead of being capacitively coupled to the nwell they are capacitively coupled to the input pad. Multiple copies of the amplifier are included to allow testing of matching of amplifiers in close proximity to each other. It will also allow comparing the performance of amplifiers on several of the test chips available to test similar matching across a wafer.

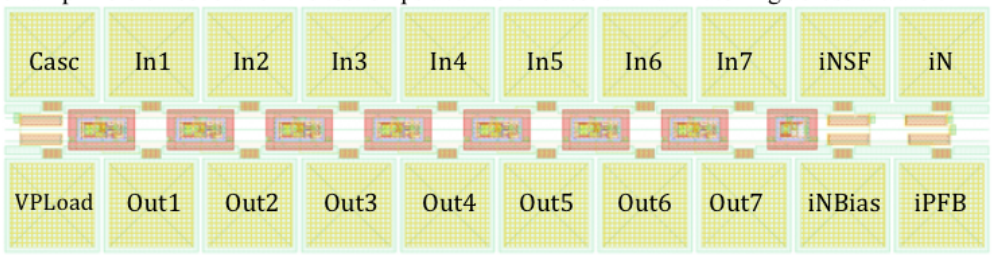
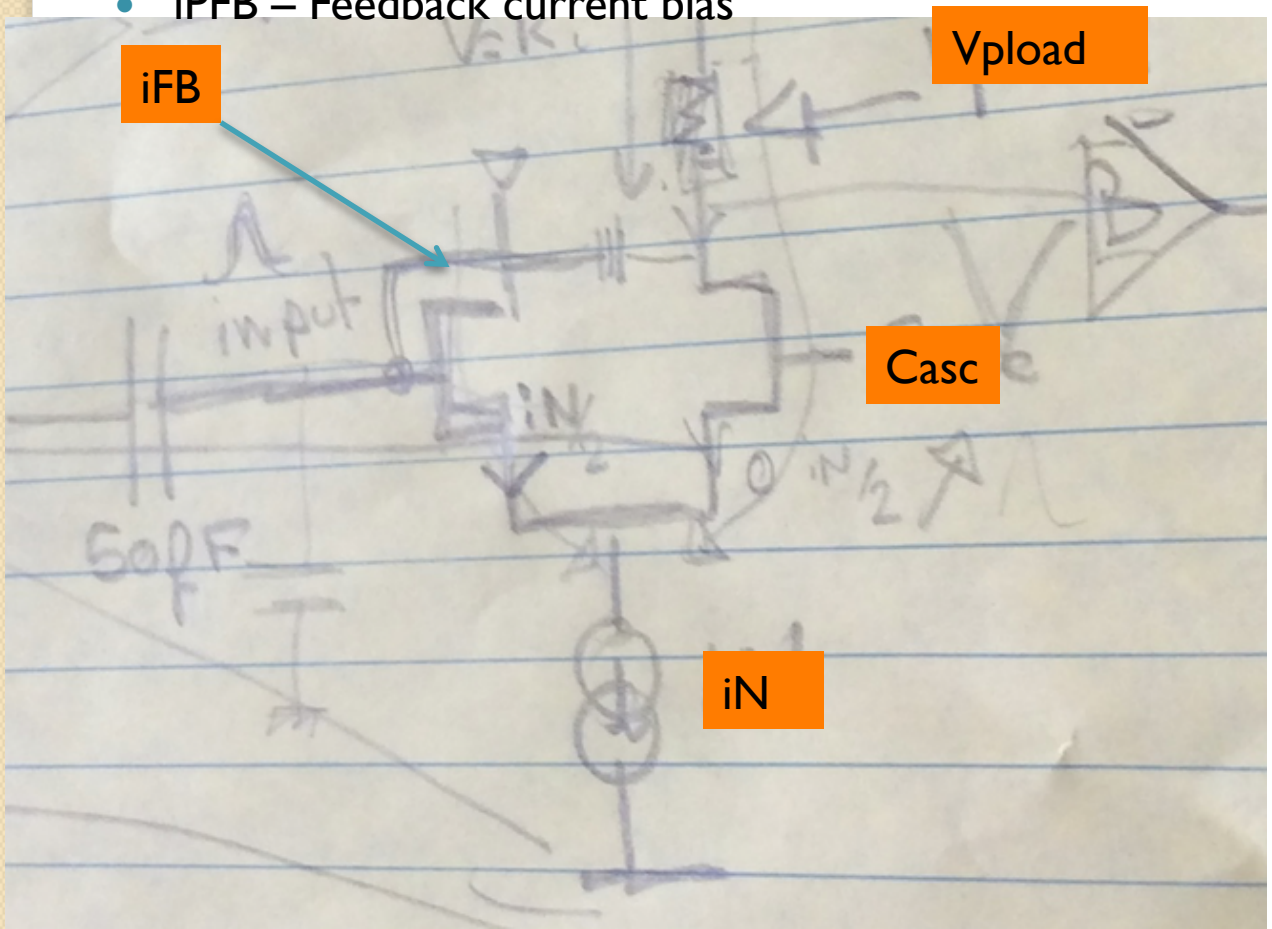


Figure 3–4: Layout of the isolated fast amplifiers.

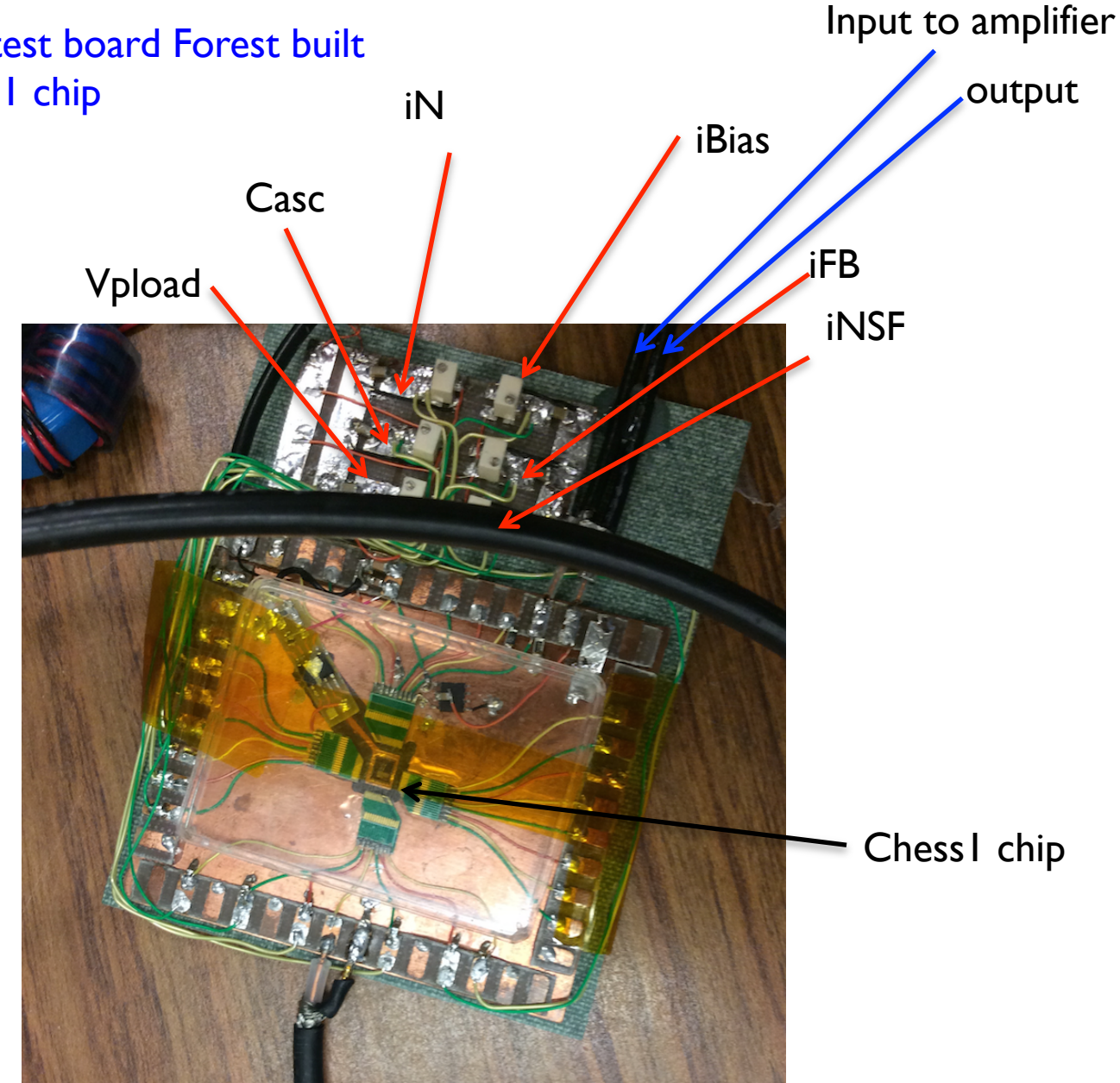
Amplifier Biasing

- Casc -Cascode bias
- iNSF – Source Follower Bias
- iN – Amplifier current source bias
- VPLoad – Amplifier Resistive Load bias
- iNBias – Nwell resistive path bias
- iPFB – Feedback current bias



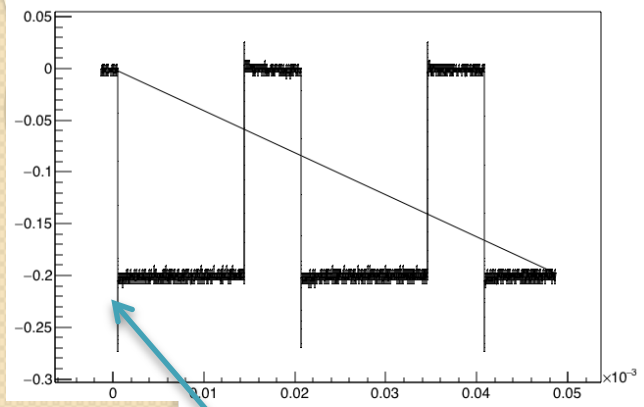
Setup to test amplifier performance

Home grown test board Forest built
To test CHESS1 chip



Setup to test amplifier performance

Voltage (V)



50fF coupling capacitance

Pulser

Input pulse

Voltage source

3.3V bias for amplifier

Isolated Amplifier on CHESS1 chip

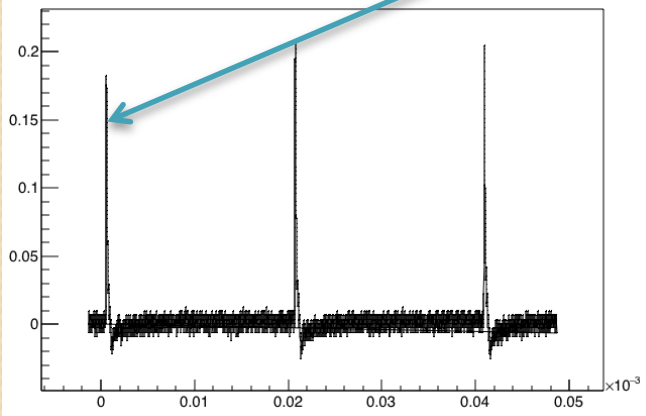
Amplifier output

Source follower

Scope

Falling edge

Voltage (V)



Time (s)

4 configuration of amplifier setting

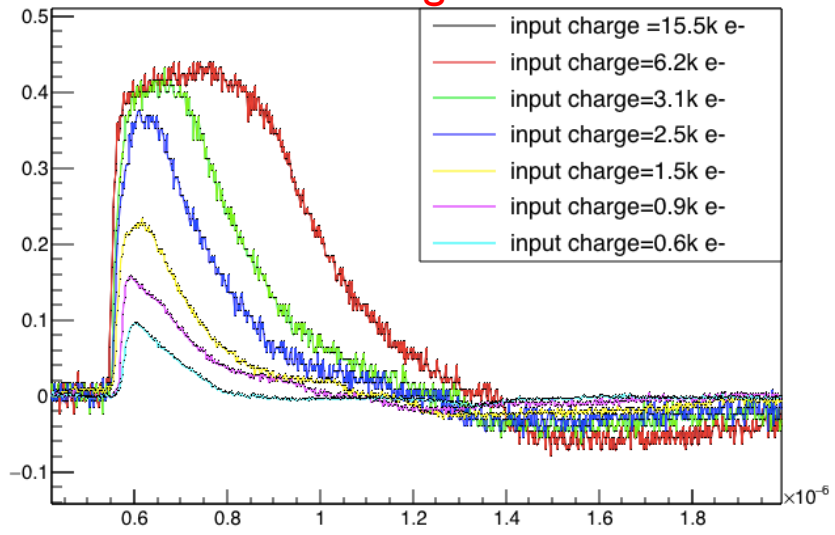
- Keep iBias,Cacs,Vpload, iN constant
  - iBias=0.34V. Cacs =2.6V,Vpload=2.1V, iN=1.4
- Varying iFB and iNSF to optimize the performance

- Config1:
  - iFB=2.664V, iNSF=0.569V
- Config 2
  - iFB=2.597V,iNSF=0.576V
- Config 3
  - iFB=2.71V,iNSF=0.766V
- Config 4
  - iFB=2.682V,iNSF=0.566V

Output pulse Vs input charge

Output (V)

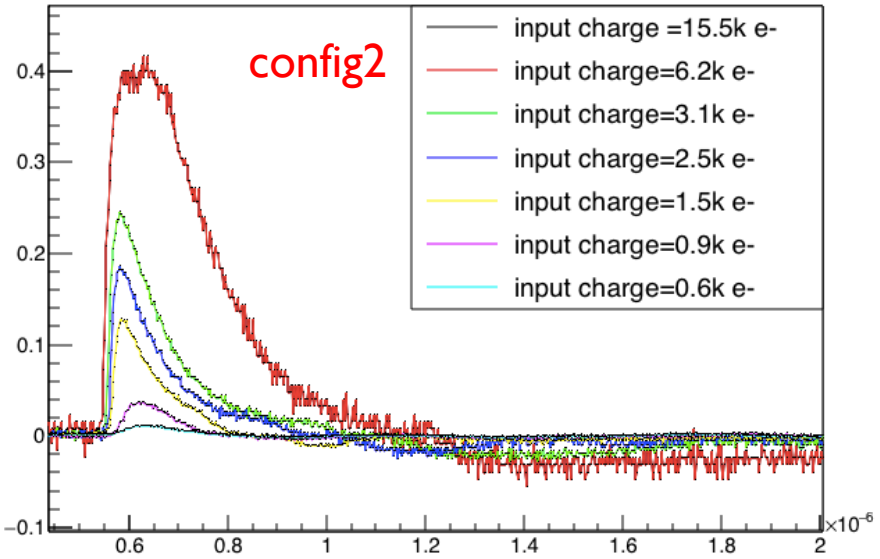
config1



Time (s)

Output (V)

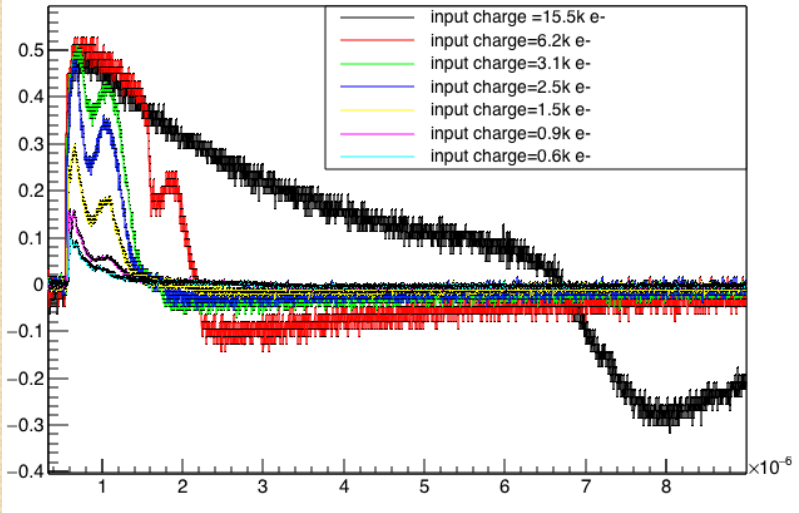
config2



Time (s)

Output (V)

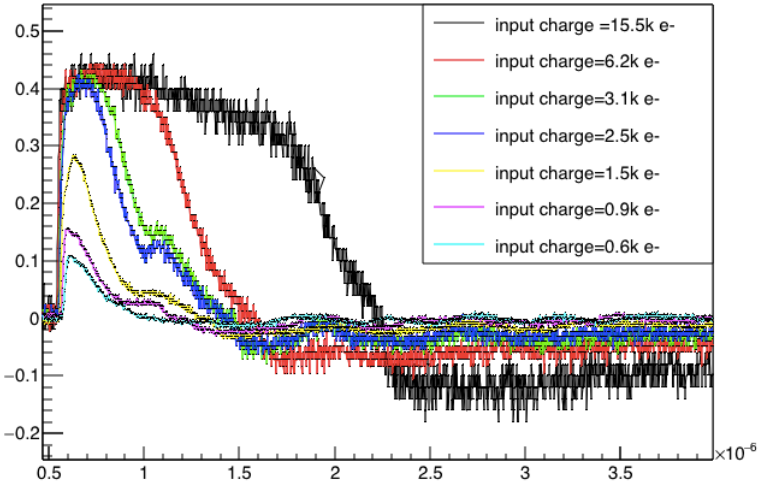
config3



Time (s)

Output (V)

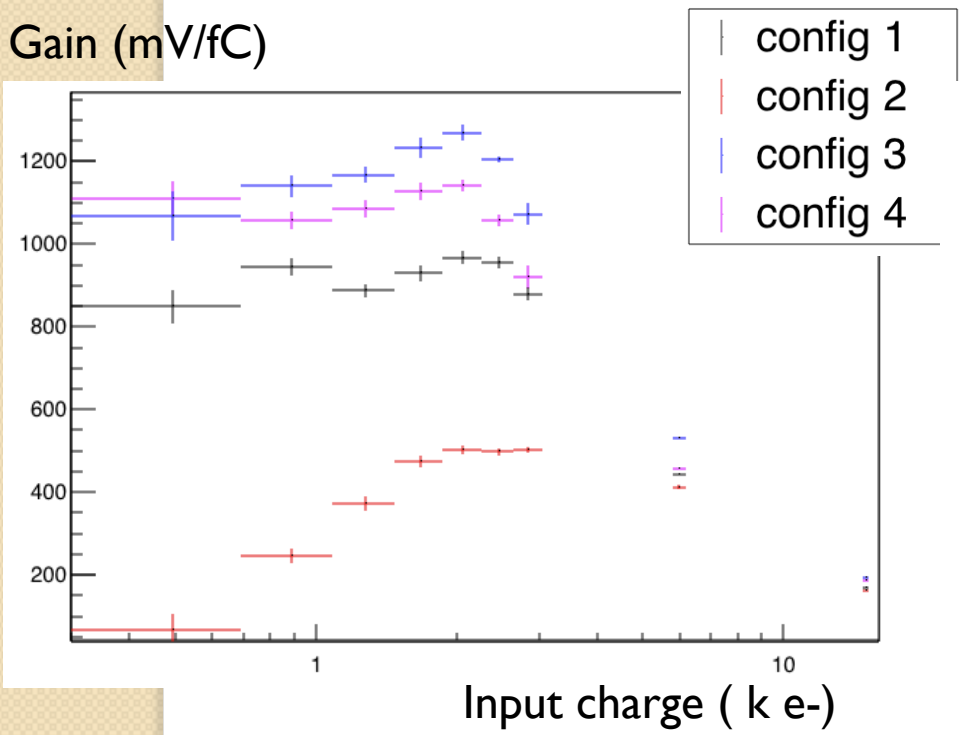
config4

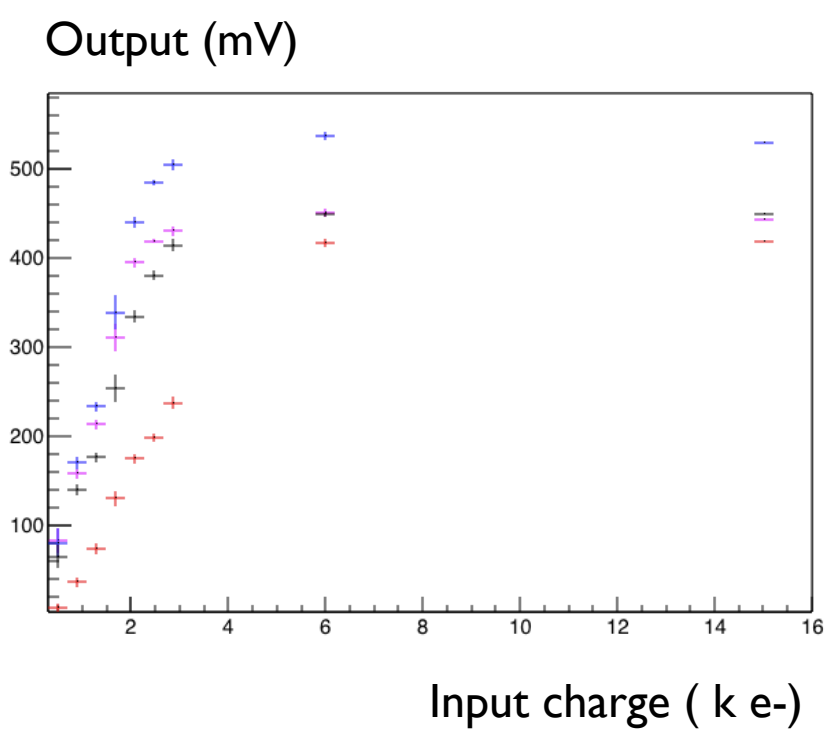


Time (s)

Gain Vs signal size

- Assuming Gain=V_out/Q_in
- gain is designed to be 500 mV/fC
  - Measured gain is higher
- Config 2 is bad for small signal





Amplifier Noise

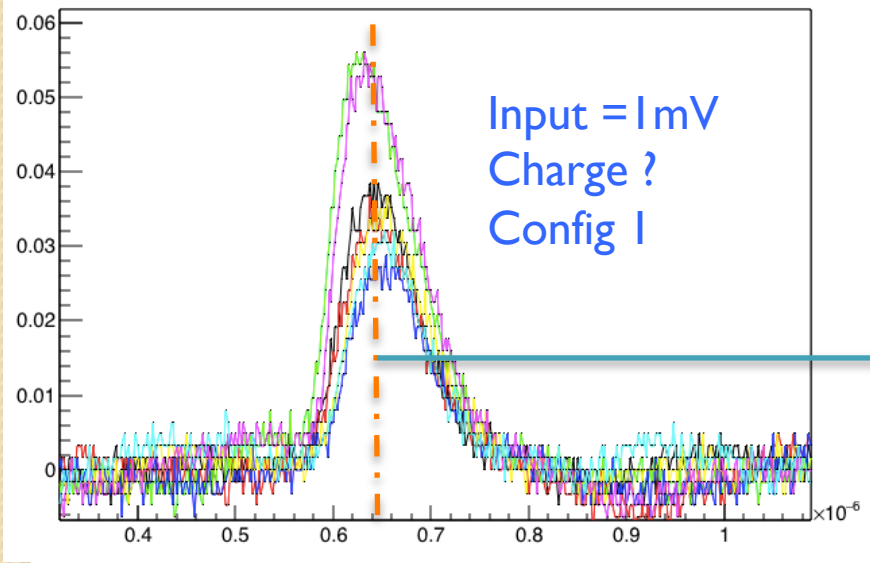
- Noise of the amplifier (upper limit) can be estimated by measuring the event-by-event variation in signal peak

8mV output noise
750 mV/fc measured gain for 1mV signal

→ 66.5 e- measured input noise
<100 e- input noise expected

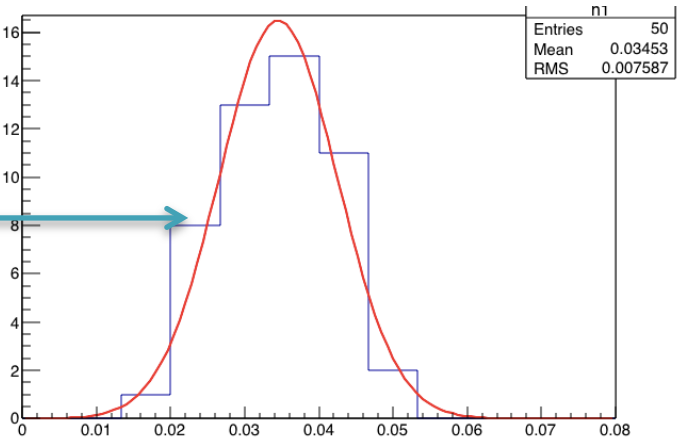
Output (V)

Different color is
From different events



Time (s)

count

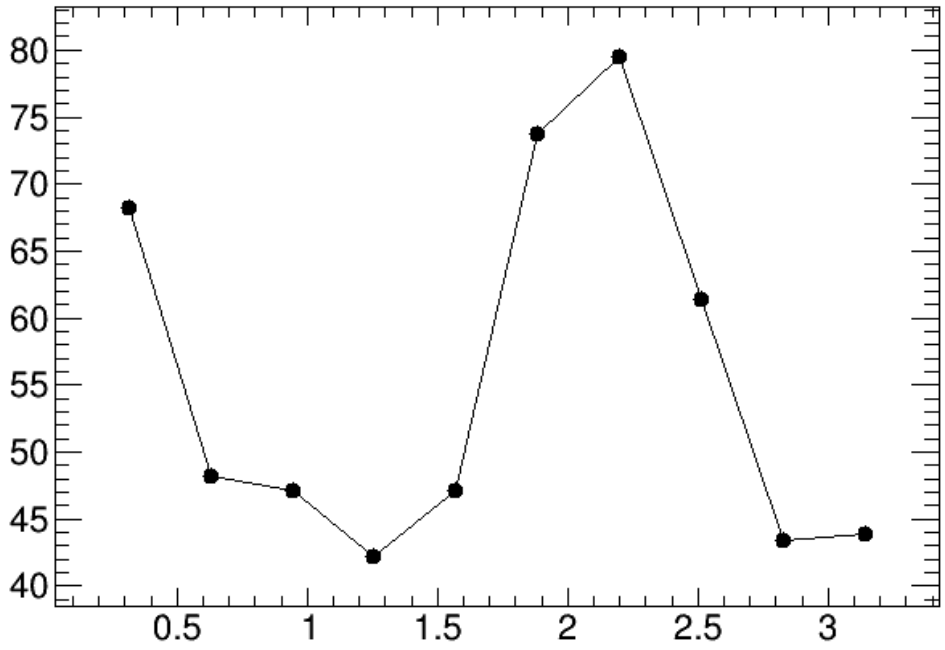


Output at peak (V)

Amplifier Noise

- Input Noise : 40~80 e- (<100 e- expected)

Input Noise (e-)

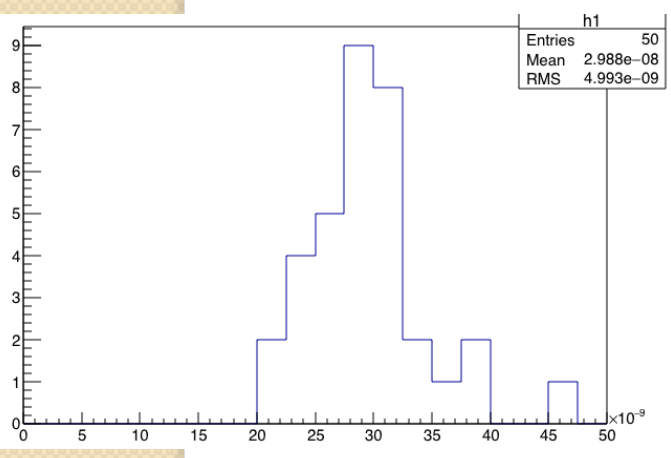


Input charge (k e-)

Amplifier output signal rise time

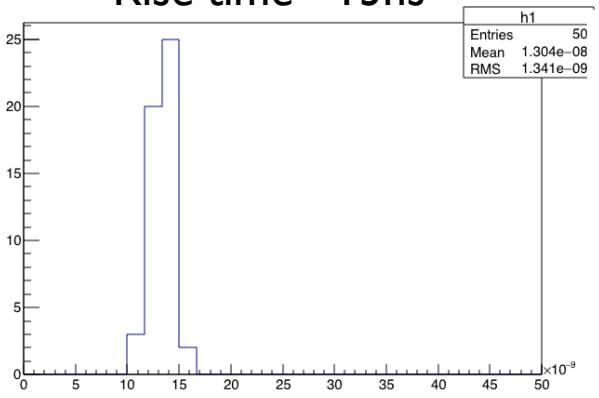
- Pulser input signal has 9ns rise time
- Amplifier output Rise time (10%-90%) vary between 13ns – 30ns
  - Depending on the input signal amplitude

Input =0.3k e-
Config 1
Rise time =30ns



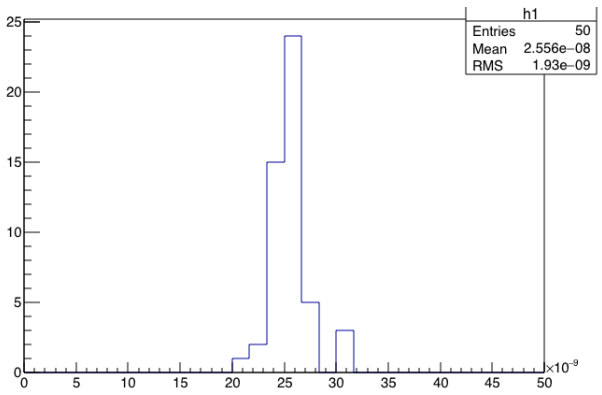
Output signal rise time(s)

Input =1.5k e-
Config 1
Rise time =13ns



Output signal rise time(s)

Input =3.1k e-
Config 1
Rise=25ns

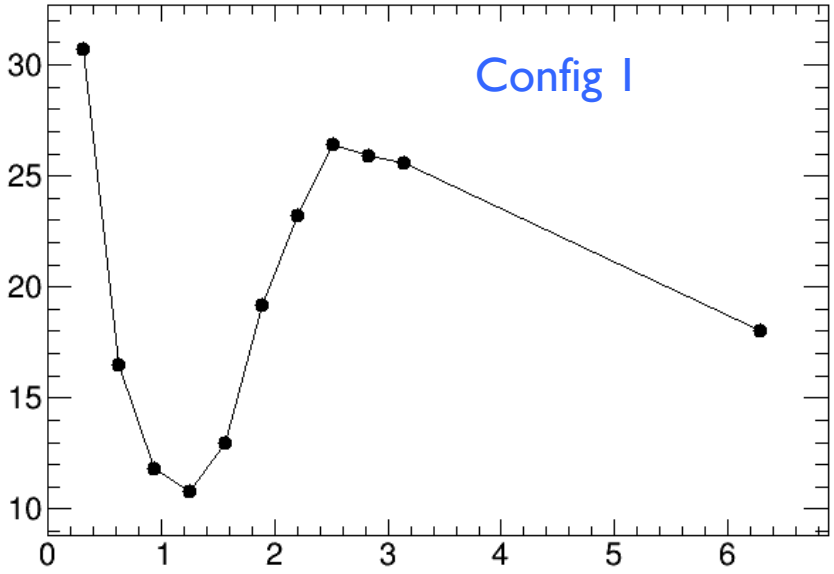


Output signal rise time(s)

Amplifier output signal rise time

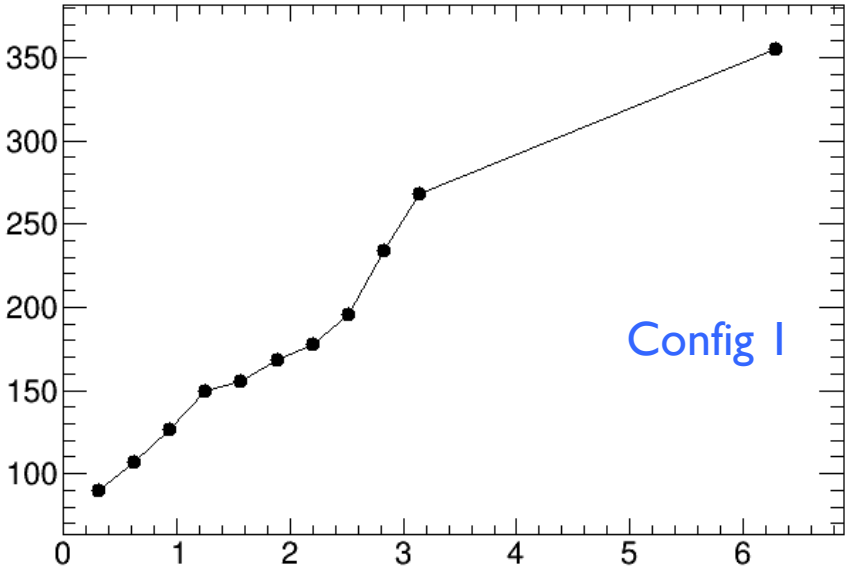
- Rise time : 10~30 ns depending on signal size
- **Full width at half maximum is from 80ns ~360ns depending on signal size.**

Rise time (ns)



Input charge (k e-)

FWHM(ns)



Input charge (k e-)

Summary

- first exercise on optimizing the built-in CMOS based amplifier in CHESS1 chip
  - As input to CHESS2 active array design
- Measured Amplifier performance
  - Gain : 500 ~ 1300mV/fC (500 mV/fc is expected)
  - Input Noise : 40~80 e- (<100 e- expected)
    - Input noise is good
    - But It is measured in isolated amplifier without sensor
    - It may be nosier in real detector
  - Rise time : 10~30 ns depending on signal size (15ns expected)
  - Full width at half maximum is from 80ns ~360ns depending on signal size.
- Configuration 1 gave the best performance
  - Best balance between gain and output signal shape.
  - iBias=0.34V. Cacs =2.6V, Vpload=2.1V, iN=1.4
  - iFB=2.664V, iNSF=0.569V
- Next steps:
  - Try to reduce power consumption by reducing Amplifier current source bias(iN)
  - Study signal to noise using laser injection in active pixel array