CMOS Strip Project   
1st year Status Report

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For the CMOS Strip Collaboration

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Abstract (Do we need one ?)

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# The CMOS Strip project within ATLAS

## Introduction

This document describes the progress made since June 2014 in establishing a CMOS-based strip sensor as a drop-in solution for the ATLAS Phase-II Strip Tracker Upgrade. It gives an overview of the project and its rationale and then addresses the impact of such a sensor on the overall detector mechanics and electronics. The current statuses of the tests are given together with the upcoming plans for the next year. It concludes with an outlook about the future of this technology within ATLAS.

### The Phase-II Upgrade strip tracker layout

For the Phase-II Upgrade of the ATLAS detector scheduled to be completed in 2022, it is planned to replace the current tracker with an all-silicon detector using both pixels and strip sensors. The current layout as described in the Letter-of-Intent (LoI) [1] consists of a barrel with four hybrid-pixel layers and five strip layers (including a stub) and two endcap consisting of six hybrid-pixel disk and seven strip disks each. Each layers uses small-angle stereo sensors with a pitch of 75 µm on each side. The total area of this tracker is estimated to be 201 m2, of which over 95% belongs to the strip tracker. The current layout is shown in Figure 1 and has been adopted as the baseline design for the upcoming studies.

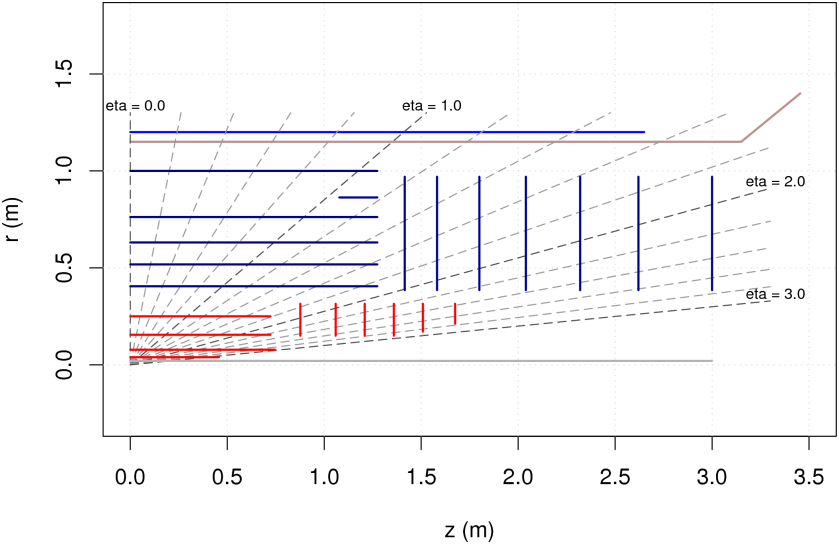


Figure 1: The current baseline Tracker layout for the ATLAS Phase-II Upgrade

The strip tracker uses staves and petals (see Figure 2) as central building blocks compared to the present module-based ATLAS SCT. A stave consists of a carbon-fibre core with thirteen identical modules mounted on each side. A module has a silicon sensor with 10x10 cm dimensions and a strip length of 2.5 cm with a strip pitch of 75 µm. Each module has two hybrids with ten ABC130 readout ASICS each. Altogether a module has 4096 channels. All the data, commands and the power are centrally routed through the end-of-substructure card. For the endcaps, a similar scheme has been proposed, however the wedge-shaped petals have nine differently shaped modules on each side. The data/commands are routed to the DAQ using High-Speed radiation-hard optical links – the so-called GBTs – which are envisaged to provide bandwidth up to 9.6 GBit/s. Low-Voltage is distributed using DC-DC converters for each module, while for the sensor high-voltage a HV-Multiplexing scheme is foreseen.

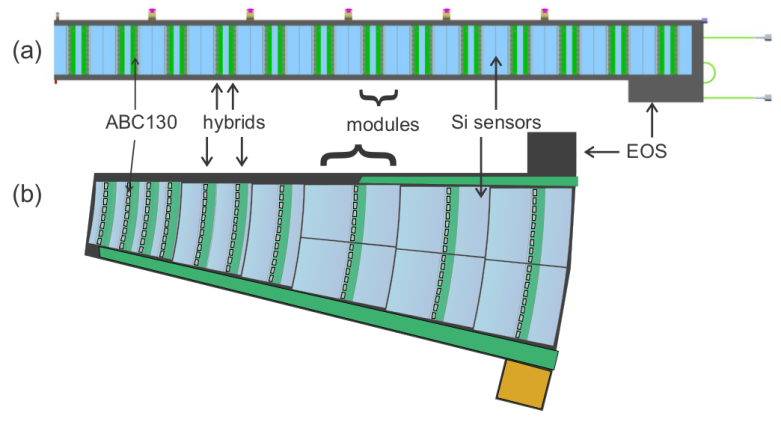


Figure 2: Staves (a) and Petals (b) as building blocks of the baseline design.

ATLAS is currently re-vising its baseline design for the upcoming Technical Design Report (TDR) which is scheduled to be finalized in September 2016.

### Monolithic active pixel sensors

Monolithic active pixel sensors (MAPS) have been developed since the early 90s as imaging sensors and have currently replaced the CCD sensors in most applications. Very early on, their potential as a particle detector has been realized and the first MAPS for particle physics appeared shortly thereafter. The last two decades have seen a tremendous progress in the development of MAPS both for particle physics as well as adjacent fields like heavy-ion physics and synchrotron-light applications. The basic MAPS cell was based on a 3-Transistor (3T) structure diode using NMOS transistors only. The charge is being collected with a readout diode using charge diffusion. There were two basic limitations of this approach. The n-well of the PMOS acted as a parasitic charge collection unit, which prevented the use full CMOS functionality and the devices were inherently slow due to the charge collection mechanism by diffusion. The introduction of deep implants allowed the use of full CMOS while the use of high-resistivity epitaxial layers (HR-CMOS) or the use of a special HV-CMOS process allowed collecting the charge much faster thanks to presence of a drift field. Both of these processes are potentially both very radiation-hard, to make them suitable to be used for the HL-LHC (1015-1016 neq).

## Advantages compared to the baseline solution

A CMOS-based sensor offers several attractive benefits compared to the baseline solution, which is based on a planar strip sensor. These benefits can be split in three categories, reduction of material, improved resolution and reduced cost. For the following discussion, we are using a StripCMOS sensor with a pitch of 40 µm and a length of 400 µm, which is chained a together as a digital z-encoded sensor of 2 cm length (see 1.3.1).

In the baseline solution, there is a need of having silicon sensors on both sides of the stave/petal, to provide the necessary z resolution using a small-angle-stereo configuration. The CMOS solution eliminates the need for the small-angle stereo configuration as the pixels already provide full 3D-Hits. This leads to a reduction of the material from 1.8% to 1%. The finer strip pitch and the use of pixels instead of a strip improve the resolution by a factor of two in r-φ and provide a precise point in z as well. Finally the reduction in cost and associated assembly time is significant. The total silicon area is reduced by a factor of two, which is estimated to safe in the order of 30 MCHF in core cost. There is a potential additional cost-saving benefit by switching from a very specialised process for the planar sensors to a mainstream high-volume CMOS process, which has not been fully quantified yet. Having a factor of nine less wire bonds has a significant impact on the assembly time and the associated non-costs. A summary of the potential benefits is given in Table 1.

|  |  |  |
| --- | --- | --- |
| Parameter | Planar Sensor | StripCMOS Sensor |
| r-φ resolution | 20 µm – 23 µm | 11 µm |
| z-resolution | 8500 µm | 162 µm |
| Two hit resolution in r-φ | 160 µm-240 µm | 80 µm |
| z-element length | 2.5 cm | 1.8 cm |
| Fraction of two hit clusters | 15% - 20% | 2%-3% |
| Geometry inefficiency on stave | ~0.7% | ~1% |
| Radiation Lengths per stave | 1.8% | 1% |
| Insensitive crossings after a hit | 1 BC | 0.1 (1/32 of strip is dead 3 bunch crossings |
| Number of ASICS | 2 x 10 | 2 x 10 |
| Number of Wire bonds | O(4500) | O(500) |

Table 1 Comparison between the baseline and StripCMOS solution for the ITk Phase-II Strip Tracker Upgrade

## The StripCMOS programme

At the ATLAS Upgrade Week in 2014, it was decided that ATLAS will investigate the use of CMOS sensors for the Phase-II Strip Tracker Upgrade and a three-year programme with well-defined break points after each year will start in June 2014 to lead this investigation. It is an aggressive time-driven development programme, which given the time-constraints is not optimised to fully exploit the possibilities of CMOS, but attempt to secure the benefits mentioned above for the Phase-II Tracker Upgrade. A part of the charge was that this programme will not distract resources from the baseline solution so that the TDR can be delivered on time. Part of the mandate was to have an annual review to review the progress of the programme and to decide on its continuation.

### Basic StripCMOS architecture

Given the time-constraints given by the completion date of the TDR and the available resources, it was very early on decided to investigate a so-called drop-in solution, which would replace the sensor itself and would require some modifications of the readout ASIC, but would keep everything else beyond exactly the same as in the baseline solution, therefore minimising the impact on the overall effort. It is obvious, that this solution if not taking advantage of all the benefits, that a CMOS solution would offer, but it is the only viable solution given the time-scales and the available resources. Therefore solutions, which eliminate the need for a readout ASIC by embedding all the digital logic in the sensor as well, were not pursued.

For the drop-In architecture, we have adopted a digital z-encoded design with a basic pixel size of 40 µm in r-φ and a length of 400 µm in z. The choice for the digital variant was made, it was considered to it would be easier to implement and less of a risk than an analogue z-encoded solution. The pixels then are chained connected together as a “virtual strip” or “strixel”, which is connected to the Encoder block at the end of the sensor. Each pixel has its own comparator and the z information – effectively the pixel ID – is encoded into the digital data stream in the Encoder block (See Figure 3).

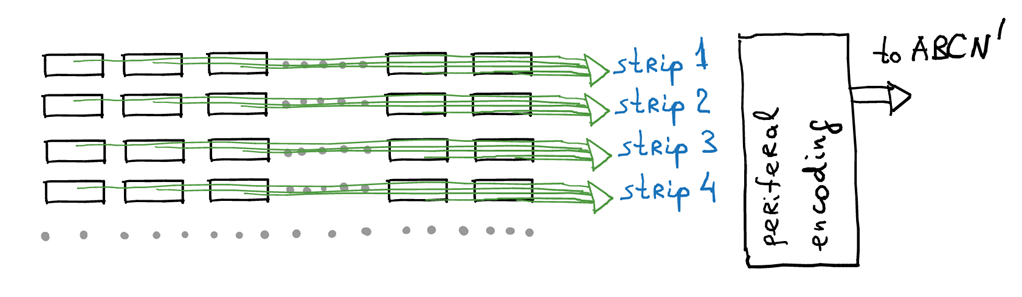


Figure 3 Sketch of the digital z-encoded design

The Encoder block at the periphery of the chip is then connected to a modified version of the ABC130 readout ASIC, which is called ABCN’. This chip has effectively the analogue front-end removed and just consists of a slightly modified digital back-end (to handle the z-encoded data coming from the Encoder block) and the interface to the HCC (Hybrid Control Chip) chip. The total size of the chip is planned to take advantage of the maximum available reticule size, which is in the order of 2 cm x 2.5 cm. For reasons of effort and potential yield, there is no stitching solution being pursued at the moment, which would allow overcoming the size limitations of any CMOS process.

### Selection of the investigated CMOS processes

The CMOS Strip programme has very early on decided to minimise the number of processes to be studied to a maximum of two. The following candidate processes have been initially investigated:

* AMS HV-350
* GlobalFoundries 130 HV
* LFoundry 180 HR
* TowerJazz 180 HR-CMOS
* Espros Photonics AG (EPC) 150 HR.

It was then decided to select both one HV and one HR CMOS process in order to have two orthogonal approaches and the most promising ones were selected. This will allow exploring the largest possible amount of phase space given the time-scales and the effort available.

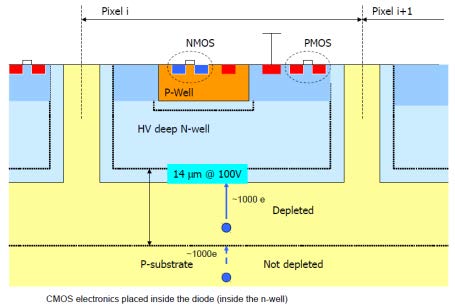


Figure 4 AMS 350 HV CMOS

For the HV-CMOS, the AMS HV-350 process was selected given the large amount of experience with this process already within the community and ease of access. The AMS HV350 technology is a variation of a standard CMOS process that is frequently used for power devices. It allows for higher-resistivity substrates and 60-100 V bias voltages to be applied. A pixel in AMS HV-350 technology is shown in Figure 4.

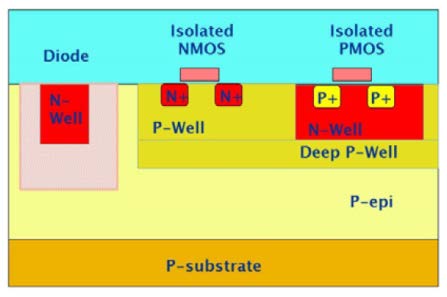


Figure 5 TowerJazz 180 HR-CMOS pixelMAPS

For the HR-CMOS the TowerJazz 180HR process was selected, given good connections past experiences and ALICE is using this process for the MAPS. This process offers thin epitaxial layers (< 20 µm) consisting of high resistivity material. It also allows to use of full CMOS capabilities due the availability of deep p-implants. A pixel in TowerJazz 180 HR-CMOS is shown in Figure 5.

### The three year programme

As already mentioned above, the StripCMOS programme has been given three years to investigate the use of CMOS. It officially started in June of 2014, co-lead by V. Fadeyev (UCSC), R. Nickerson (Oxford) and M. Stanitzki (DESY). Below the goals and milestones for each year are summarised.

#### Year 1: Characterization of basic sensor/electronics properties and Architecture

The goal of the first year is to establish the feasibility of using CMOS for the the Phase-II Strip Tracker Upgrade. Two decisions have already been made beforehand, the selection of AMS and TowerJazz as the target foundries and the decision to pursue a digital z-encoded design. In terms of the Pixel development, the primary goal was to establish characterize the pixel itself, especially its radiation hardness. The boundary electronics need to be specified and a common readout system for testing needs to be selected.

Furthermore, the impact on the physics is to be evaluated and the integration in the baseline design needs to be studied. Together with the foundries, the viability of stitching, cut lines, stitching and multi-reticule possibilities need to be evaluated.

#### Year 2: Fabricating and evaluating a large-scale device.

The main goal of tear two is to manufacture a large scale sensor with close to full functionality, evaluate its radiation hardness and to characterize the pixels in terms of Hit efficiency, charge collection speed and to measure to signal-to-noise ratio. The boundary electronics architecture needs to be tested and its performance must meet the goals.

For the mechanics, all potential substantive changes required need to be evaluated and test parts will be fabricated for any essential new elements. Potential changes to the services need to be studied and bus tapes to be redesigned to accommodate new module configurations. The last item is the ABCN’, which needs to be designed, fabricated and tested and a first hybrid design needs to be available at the end of year two.

#### Year 3: Full prototypes of sensors and ABCN’ .

The ABCN’ needs to be available in significant quantities and tested with sensor prototypes from year two. A full scale sensors needs to be designed, fabricated and characterised and both sensor and ABCN’ need to operated in a module-like configuration. As a second step, have more than one of these module operating on a bus tape. Changes to accommodate new layout and stave/petal need to be designed and assembly protocols and series production planning have been considered.

### The StripCMOS “collaboration”

While the programme started from within ATLAS, there is a significant fraction of key people, which are not members of the ATLAS collaboration, but have still a strong interest in the success of this project and are contributing a lot of effort. Therefore we’ve formed the StripCMOS “collaboration” to give credit to all participants whether they are part of ATLAS or not.

# Resources

For the three-year programme we’ve made use of existing infrastructure and effort in the participating groups as well as having some additional resources, which is coming partially from existing grants or additional funding from labs. The major fraction of the money up to now went into the submission of the chips (Details see Sections 4.2 & 4.3) and a significantly smaller fraction in production of the associated testing PCB’s.

## Submission Costs

We have submitted two chips in the first year (CHESS1-AMS and CHESS1-TJ) and are in the process of submitting a third chip. The individual contributions to the submission costs are listed in Table 2.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | DESY | SLAC | UCSC | UK Groups |
| CHESS1-AMS | 0 |  |  | 20 |
| CHESS1-TJ | 70 |  | 0 | 0 |
| CHESS2-AMS | 20 | ? | ? | 50 |
| Total | 90 |  | 30 | 70 |

Table 2 Financial contributions to the chip submissions in kEUR

# Impact on detector mechanics and electronics

It is recognized that the schedule does not permit a complete redesign of the mechanics to opmise for the use of CMOS sensors. Considerable compromise is envisioned in order to facilitate re-use of the bulk of the work already done for the mechanical systems. The layout does not change from that proposed for conventional strips in the sense that the planes remain in the same place: the principle alteration is from two planes of stereo to one of pixelated strips. It is argued that by design the geometry is so similar, that to a significant degree in the barrel region can use the same mechanics as the LoI layout, the same services concept, with only moderate changes required. In the forward region the situation is more complex as wedged sensors are not envisioned for the CMOS option. Whilst an outline early concept for an implementation for the forward region is sketched here, it remains a major task for the second year of the programme to understand in detail how the forward region can work with rectangular detectors. For the forward region there are significant mechanical simplifications as well as complications, so this is anticipated as being a tractable problem, but it is acknowledged that this is a significant change and that the effort required to fully understand it is not negligible.

The goal for the first year of the programme on the mechanical side was ‘ basic study of mechanical implications’.

## Barrel Region

### Barrel stripCMOS module

The barrel stripCMOS module is shown in the figure below, it consists of four silicon sensor elements, bonded to a single hybrid, which has the ABC’ read-out chips, an HCC and a DC-DC convertor. The hybrid is a flex-rigid and acts both as the electrical hybrid and the mechanical stiffener for the module. Each of the four sensor modules consists of five independent reticules each with an independent CMOS sensor. Each ABCn’ services two such reticules, a total of ten ABCn’ per hybrid. The number of wirebonds is vastly reduced compared with the planar detectors as (synchronous) data sparsification happens in the periphery of the sensor reticules. The sensors are directly bonded to the staves, so the good heat transfer properties with the planar design are retained.

Each strip is 1.8[[1]](#footnote-1)cm long and the strips are on a 40m pitch. A strip is divided into 32 elements, providing z information for a hit.



Four modules on a stave, three showing reticule layout above and below the stave (which is invisible) and one showing the hybrid with ABCn’ read-out ASICs

The performance of the LoI layout using CMOS sensors has not been simulated, but some estimates of the likely performance can be made from scaling arguments and earlier work on CMOS sensor response to tracks. Some simulation work has been done to understand occupancies. The table shown earlier in this report gives estimates of the comparison between CMOS and planar for the barrel region. Several assumptions are made regarding geometric efficiency, not enumerated here. An example is that it is easier to eliminate the gap at z = 0 for CMOS sensors in the barrel region, but there are more z gaps between sensors for the CMOS case. With a different geometry of CMOS module these could be reduced to zero, but the number of modules would double and this seems a high price.

### StripCMOS Barrel Stave

The modules are alternately tiled on opposite sides of the stave, with the module at z=0 protruding beyond the end of the stave. This arrangement is similar to the planar detector, but considerably simplified and allows actual overlap of sensitive regions at z=0. This also allows the contraction of the stave to be allowed for in the centre of the stave which could be exploited to simplify the end of stave region (but doesn’t need to be). Mechanically the stave core is almost identical to the planar design, with the major change being to the service tape on the surface. These would be no more complex than the existing design, but would be different. The bulk of the effort on the existing tapes has been to understand radiation hardness, manufacturing methodology, size stability etc.. Changing the actual layout is a significant but not a long task. It would also mandate reprogramming the tape testing robot.

18 modules are attached to each stave. The total power consumption is comparable to the baseline planar stave, the total data rate is reduced as the z information does not require a two separate hits to be encoded, but only a few extra bits on a single hit. The DC-DC convertor in this model would be redesigned to provide power for just one module. The ongoing HCC design is being done with possible use with a CMOS data structure in mind. It is anticipated that the module mounting robot could be reprogramed and with a new set of jigs used to mount CMOS modules just as easily as planar.

Whilst the heat dissipation remains relatively symmetric on either side of the stave it is not identical to the planar design, so some simulation and measurement work will be needed to verify that the stave does not change behaviour with the alternate module layout. Some additional work on redesign of the end of stave services may be needed as it is not yet certain all the services will remain identical. They should however be extremely similar so this should not be a major task. In fact the total data rates should be reduced (two binary hits are replaced with one with z address), so if anything the services might simplify.

### Geometric Inefficiency and Pattern Recognition

This issue applies equally to barrel and forward strip regions and is not repeated in the sections relating to the forward region.

The number of planes required to ensure high efficiency tracking and low ghosting is complex to evaluate as, in part, it depends strongly on the algorithmic methods employed. The CMOS option described replaces 10 planes of single sided detector with 5 of pixelated layers, which could adversely affect many algorithms. However the required number of planes depends not only on the number and efficiency of individual planes, but also on the quality of information the planes are providing. The strip CMOS option improves the r-φ resolution by almost a factor of two, the z-resolution by a factor of five, and the two hit resolution by a factor of two to three in r-φ . This is close to being a pixel detector in terms of segmentation with a strip-like read-out: it is possible that with appropriate algorithms, and including the pixel layers, that the five planes of strip CMOS would provide better pattern recognition than 10 of planar. The planar area ambiguity in (r-φ) -z associated with a hit is reduced by a factor of ten and there is also a smaller but also large improvement in the two hit resolution. Whilst not currently planned, it would be possible with stripCMOS to provide two hit resolution in z of 1.2mm, ie multiple hits from within a single strip.

The plot below (from R.Jansky, thesis) shows the mean number of tracks as a function of angular displacement from the centre of a hadronic jet. At the radius of the strip tracker the first bin in this plot represents a physical separation of about 3mm between tracks. This is a 75 CMOS strips wide distance, about 35 resolvable separate (r-φ) regions with a mean number of hits of 1.3 for a 1TeV jet. Magnetic bend will improve things further. With 20k background hits from the uninteresting events in a beam crossing this gives 0.4 background hits in the same 75 strip region. It is reasonable to anticipate that a detailed study will prove favourable in terms of pattern recognition even with a reduced number of planes when the two track resolution and improved resolution is fully exploited.



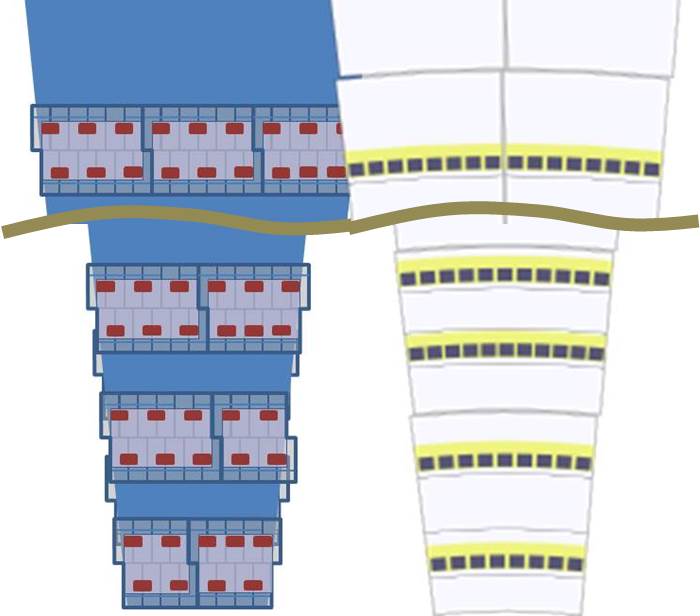
## Forward Regions

In the forward region the basic layout is unaltered from the planar design; as with the barrel region the support mechanics and services concept is also essentially unaltered. The sensors are tiled onto similar petals as would be used for planar sensors.

There is one major change in the forward region compared with planar. Because it is not practical to design wedge shaped sensors in CMOS, a non-pointing geometry is adopted. The basic sensor is identical to that for the barrel region, but the wafers are cut into different sizes of reticule blocks. Effectively modules of different shapes are built based on 1.8cm x 1cm tiles. The use of non-pointing geometry is being considered even in the case of planar sensors, the pattern recognition uses space points, which are provided with better precision by CMOS sensors, so there is no fundamental problem with this approach.

### Forward stripCMOS module

The forward modules are built from two strips of 1.8cm tall reticule blocks. The size of these is determined by their position on the petal. The barrel module is a particular case of the forward module design, unifying the forward and barrel efforts with concomitant efficiency gains expected. The figure shows an example of a module construction, which is described in the barrel section. Also shown is how these modules build up a wedge shaped coverage. The stepped edges result in extra silicon being required compared with a wedge shaped tiling, but this is ameliorated to an extent because the overlaps between rear and front planar sensors are eliminated.



CMOS Petal (left) Planar Petal (right)



Example of CMOS forward Module. 4-4 (two rows of four un-seperated reticules offset by half a reticule). Hybrid has 4 ABCn’.

### StripCMOS Petal

There are eighteen rows of modules on each petal, which are alternately tiled on opposite sides of the stave to reduce geometric inefficiencies. Within each row there are up to three different module types, the difference between them being the number of sensor reticules and correspondingly the number of ABCn’ ASICs.

This arrangement is similar to the planar detector, but considerably simplified as there are large gaps between sensors on each side. These gaps can be used to mount the HV switches and possibly the DC-DC convertors, though it is proposed to put those on the modules. It would also be possible to simplify the EoS region by exploiting available space between the last two rows of modules.

Whist the gaps between modules can simplify mechanical aspects of the design, there is increased overlap between adjacent petals due to the edges of sensors being non-radial. This increase has not

# Programme status

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# Bibliography

|  |  |
| --- | --- |
| [1] | ATLAS Collaboration, “Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment,” 2014. |

1. This number will depend on the final sensor design and will affect the number of modules per stave and the dead space fraction. It will not affect the concepts. [↑](#footnote-ref-1)