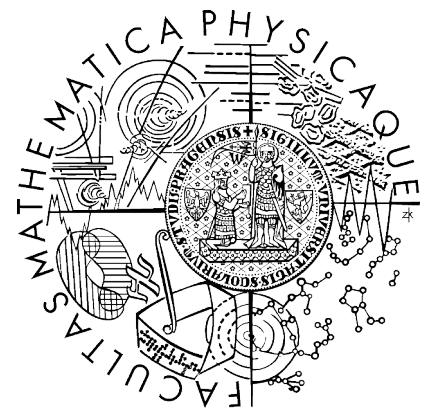


# The ATLAS Tile Calorimeter, its performance with pp collisions and its upgrades for high luminosity LHC

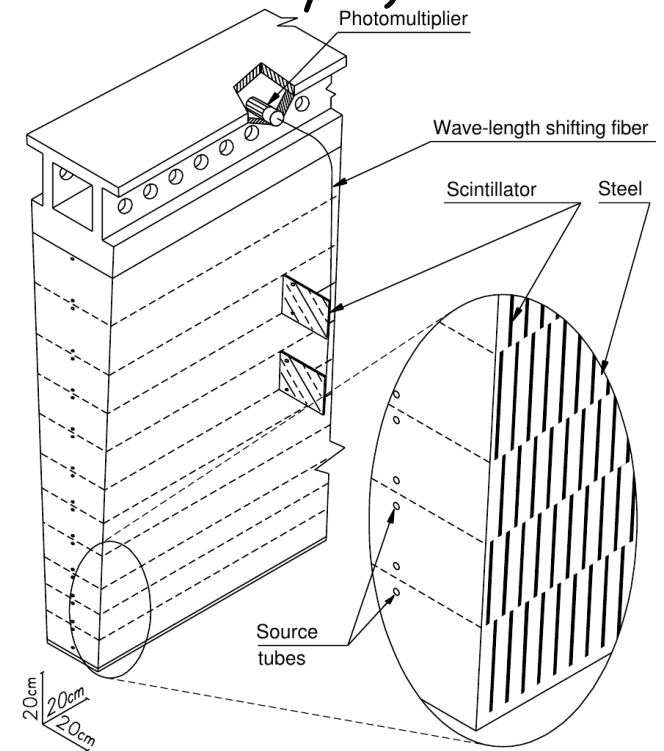
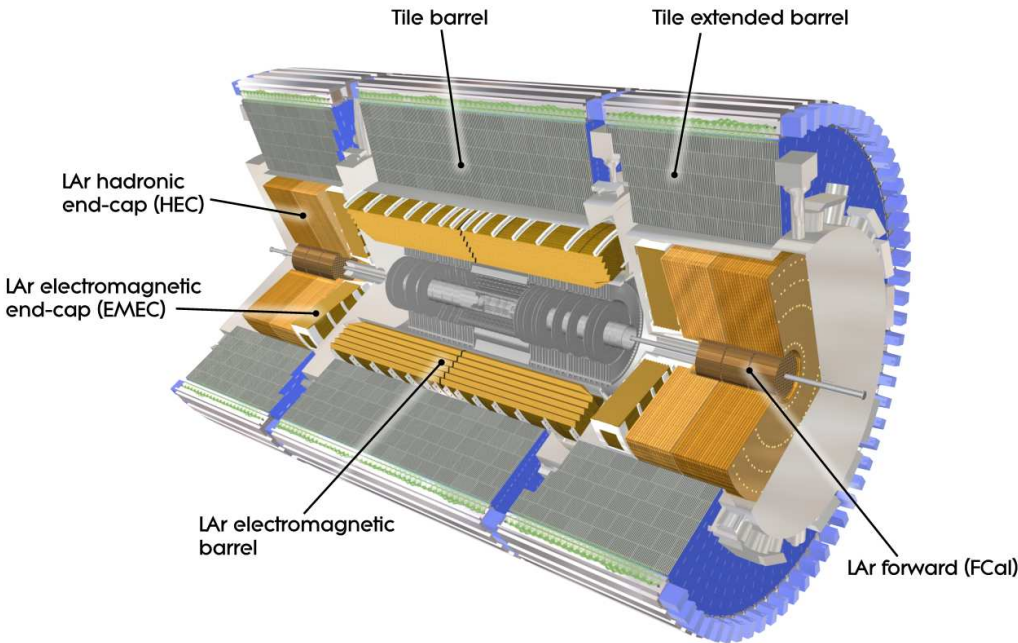
Tomas Davidek (Charles University),  
on behalf of the ATLAS Collaboration



# Tile Calorimeter

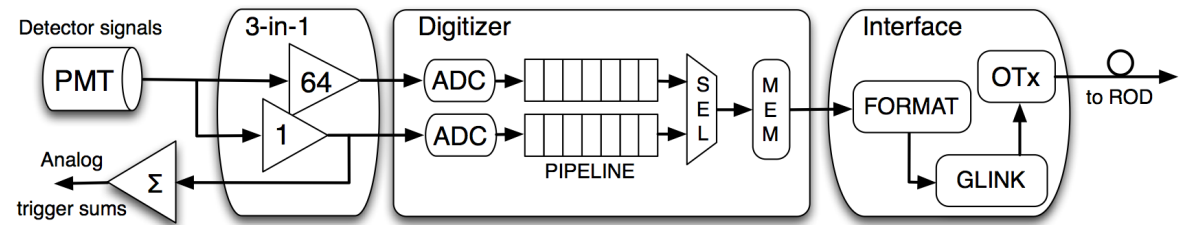
- Sampling iron/scint calorimeter
  - light from tiles collected by WLS fibers and routed to PMTs, pulse shaped and digitized; 2 channels per cell
  - 3 radial layers,  $7.4 \lambda_{\text{int}}$  in total
  - $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$  ( $0.2 \times 0.1$  in the last radial layer)

- Hadronic calorimeter in ATLAS central region ( $|\eta| < 1.7$ )
- Central Long Barrel and two Extended Barrel sections surrounding the LAr barrel emg and hadronic end-cap calorimeters

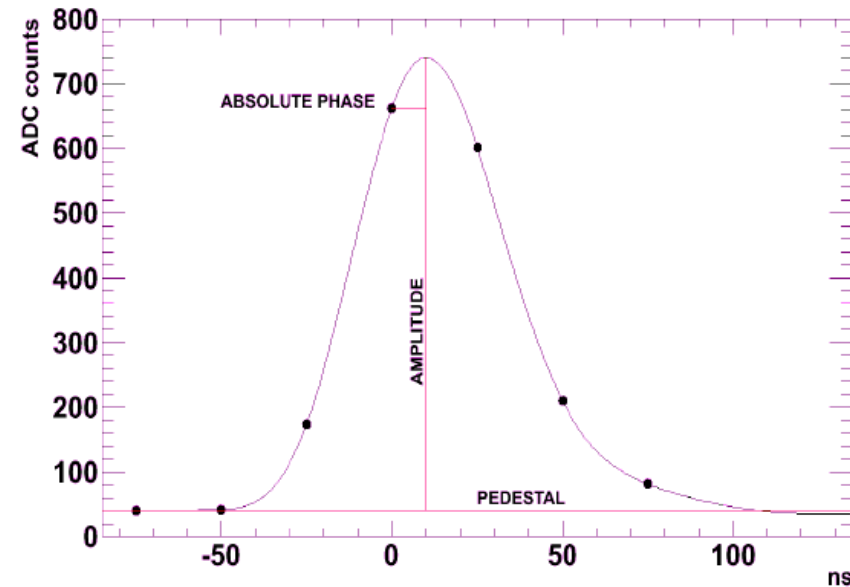


# Signal processing

- **Analog path:** signals are summed up and sent directly to Level-1 trigger



- **Digital path:**
  - signal split into two gains (1:64)
    - good signal-to-noise ratio for small signals (muons)
    - dynamic range up to 1.6 TeV energy per cell
  - shaped signals sampled every 25 ns, stored in pipeline memories and sent off-detector when Level-1 trigger accept is received
  - amplitude, time and quality factor reconstructed in Readout Drivers



# Calibration (1)

- Three dedicated systems to calibrate different stages of signal propagation

- Cesium

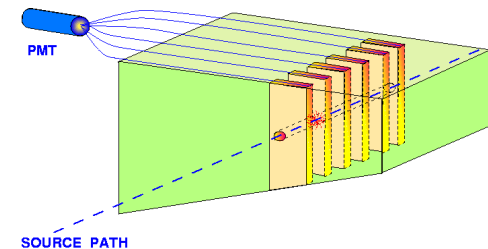
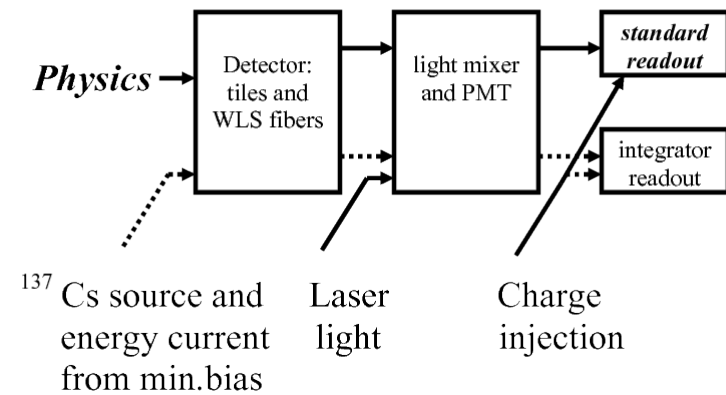
- calibrates optics, PMT gain and „slow“ electronics by passing the radioactive source through the whole detector; primary tool to set EM scale
- readout path shared with minimum bias system that averages signals from collisions over several msec

- Laser

- illuminates every PMT, calibrates PMT gain and „fast“ readout electronics
- also used for time monitoring during physics data taking

- CIS

- calibrates electronics by injecting pulses of known charge, measures amplitude [ADC] to charge [pC] conversion coef.



# Calibration (2)

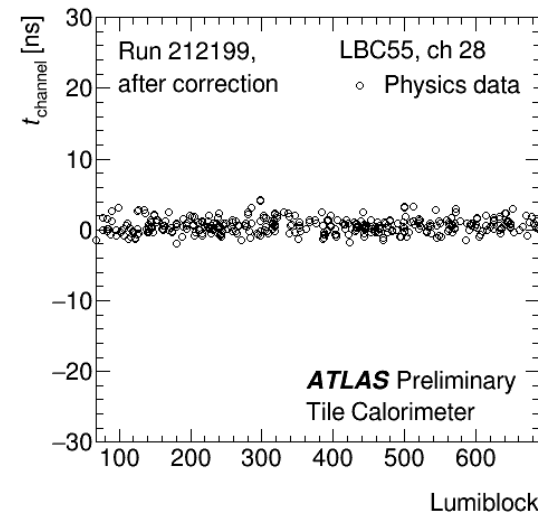
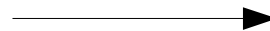
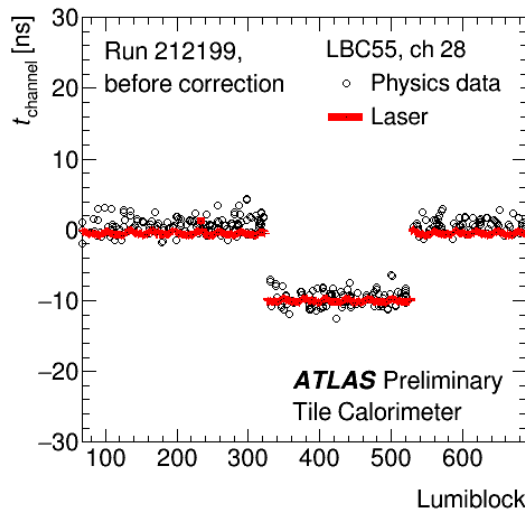
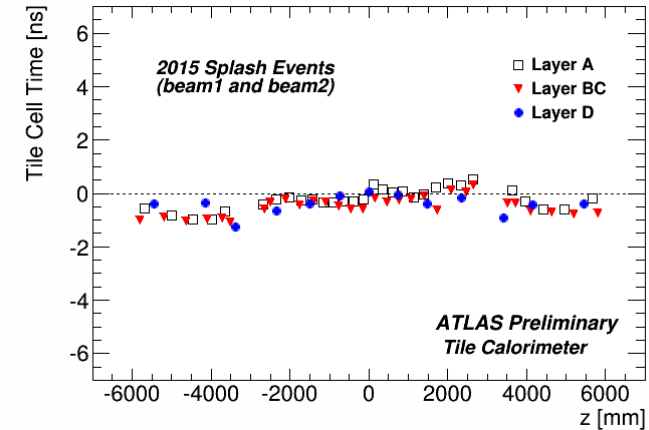
- Channel energy calibration (EM scale):

$$E [\text{GeV}] = A [\text{ADC}] \times C_{Cs} \times C_{las} \times C_{CIS} [\text{pC/ADC}] \times C_{TB} [\text{pC/GeV}]$$

measured with electrons  
at testbeams

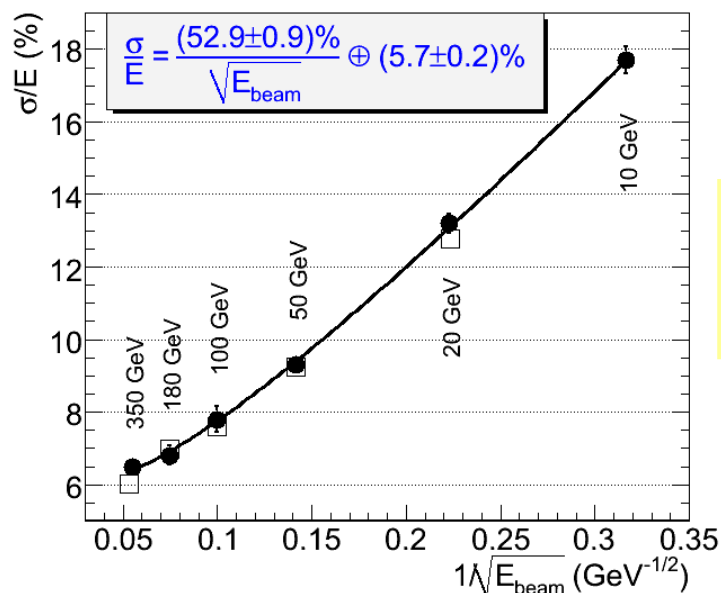
- Time calibration

- initially set with lots of high-energetic muons passing the calo parallel to beam axis (splashes)
- later fine-tuned with jets
- monitored during physics data taking with laser, eventual corrections performed before the data are reconstructed for physics analysis

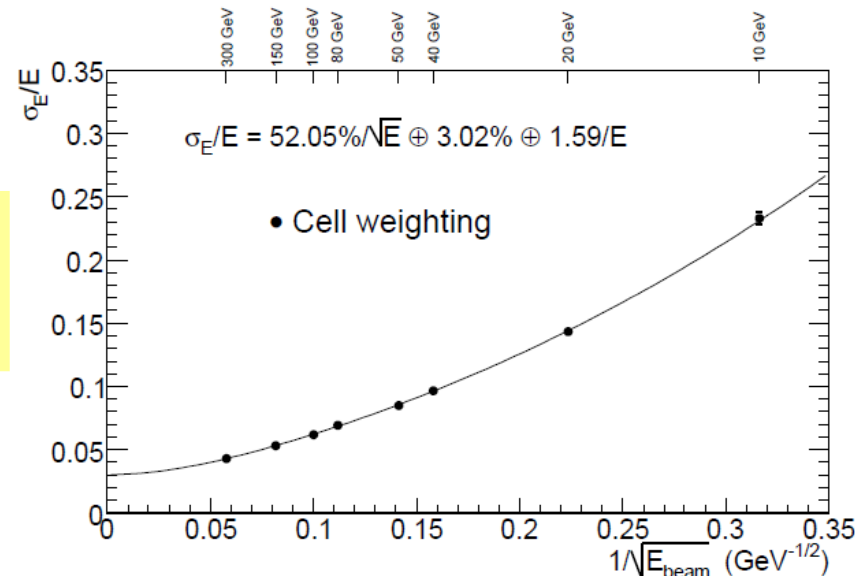


# Energy resolution

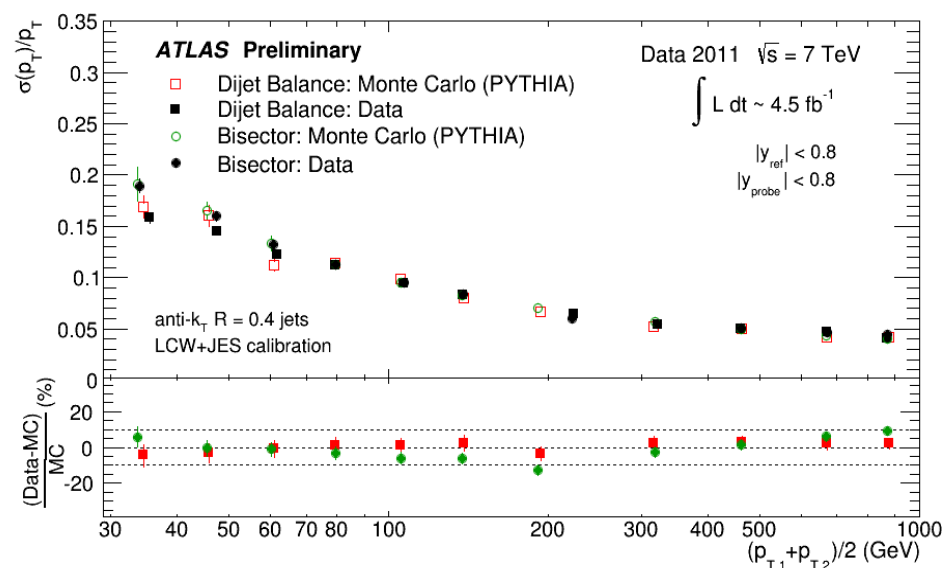
- Standalone testbeam ( $\eta=0.35$ , equivalent depth  $7.9\lambda_{\text{int}}$ )
- Combined EM LAr+Tile prototypes testbeam ( $\eta=0.25 \rightarrow 10.5\lambda_{\text{int}}$ )



pions in testbeam,  
calorimeters at EM  
scale

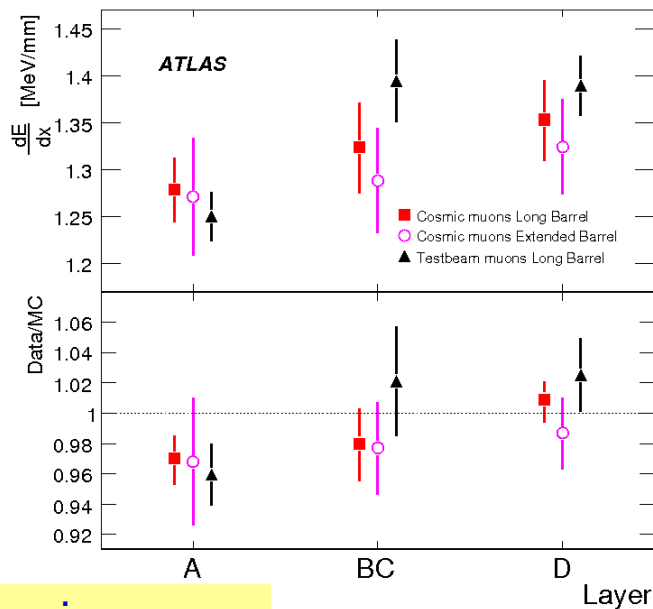


- Performance in ATLAS - jet resolution close to design
  - constant term  $\sim 3\%$
  - resolution for low- $p_T$  improves after pile-up corrections
  - slightly better results obtained with LCTopo

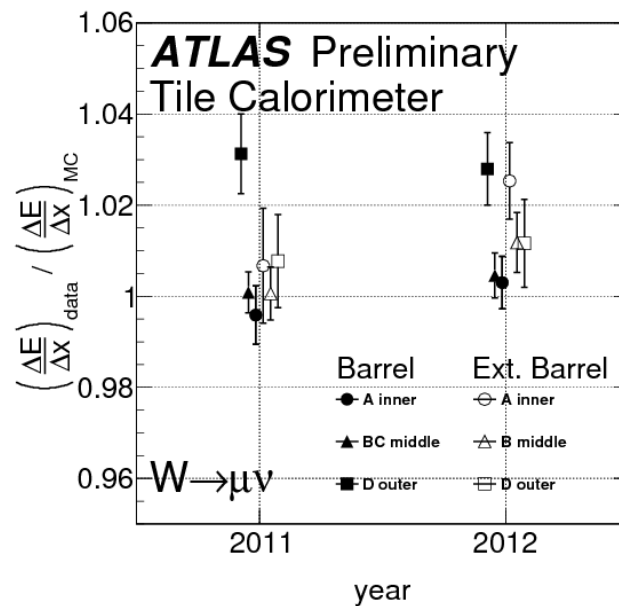


# Electromagnetic scale validation (1)

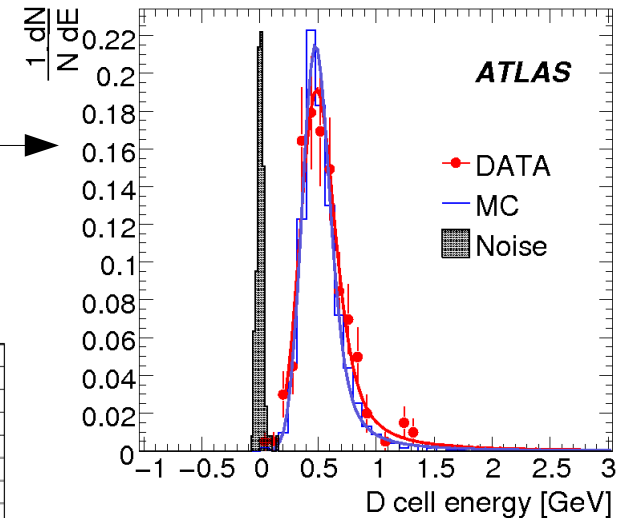
- Due to very good signal-to-noise ratio, isolated muons (cosmic rays or from collisions) represent a good tool to validate the EM scale



cosmic muons



collision muons



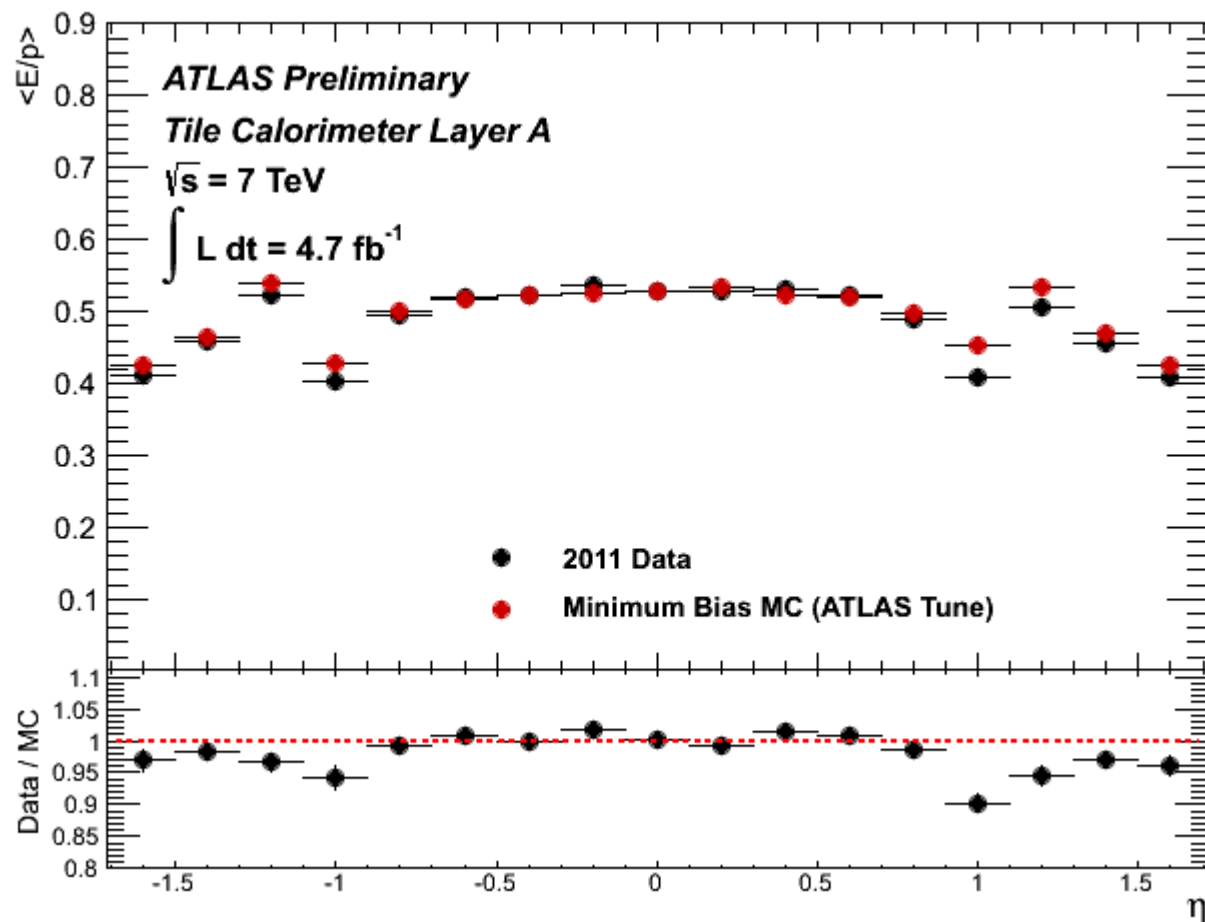
- Very good stability of the cosmic muon response in 2008 - 2010
- Similar results obtained in several analyses, maximum difference between radial layers 4%

	$R_{2008}$	$R_{2009}$	$R_{2010}$
LB-A	$0.966 \pm 0.012$	$0.972 \pm 0.015$	$0.971 \pm 0.011$
LB-BC	$0.976 \pm 0.015$	$0.981 \pm 0.019$	$0.981 \pm 0.015$
LB-D	$1.005 \pm 0.14$	$1.013 \pm 0.014$	$1.010 \pm 0.013$
EB-A	$0.964 \pm 0.043$	$0.965 \pm 0.032$	$0.988 \pm 0.014$
EB-B	$0.977 \pm 0.018$	$0.966 \pm 0.016$	$0.988 \pm 0.014$
EB-D	$0.986 \pm 0.012$	$0.975 \pm 0.012$	$0.982 \pm 0.014$



# Electromagnetic scale validation (2)

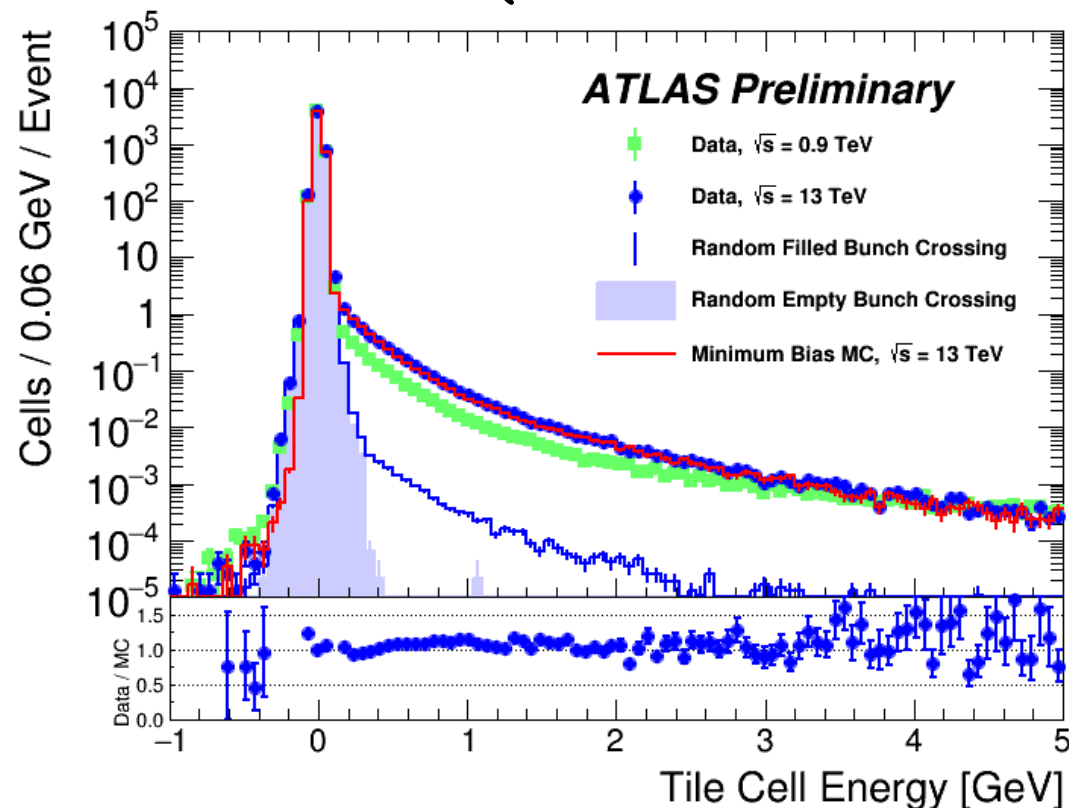
- E/p measurements with isolated charged hadrons
  - hadrons showering predominantly in Tilecal 1st radial layer (A)
  - good agreement with MC description





# Cell response in collision data

- Distribution of the energy deposited in TileCal cells from pp collision data ( $\sqrt{s} = 13$  TeV and 0.9 TeV)



- events with just one reconstructed primary vertex are shown
- Pythia minimum bias MC is overlayed
- good description data/MC

Further TileCal performance plots available on

- <https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TileCaloPublicResults>
- <https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTile>

# Upgrade

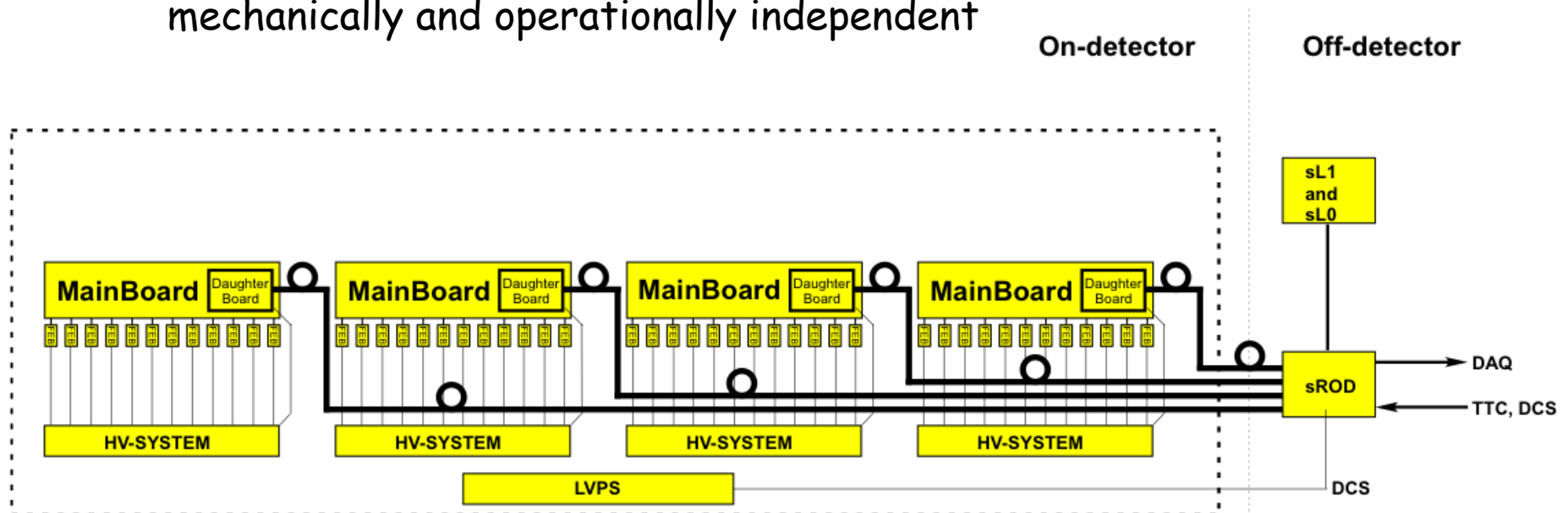
# Upgrade plans (1)



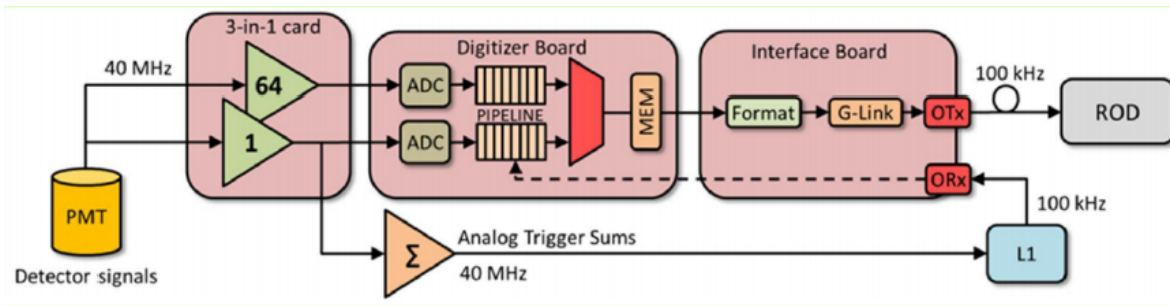
- **Phase 0:** all power supplies were replaced. Reliability improved, number of trips dramatically reduced, also electronic noise slightly reduced → better performance in Run-2
- **Phase 1:** replacement of the gap/crack scintillators due to material ageing
- **Phase 2:** major upgrade of the whole readout electronics system

# Upgrade plans (2)

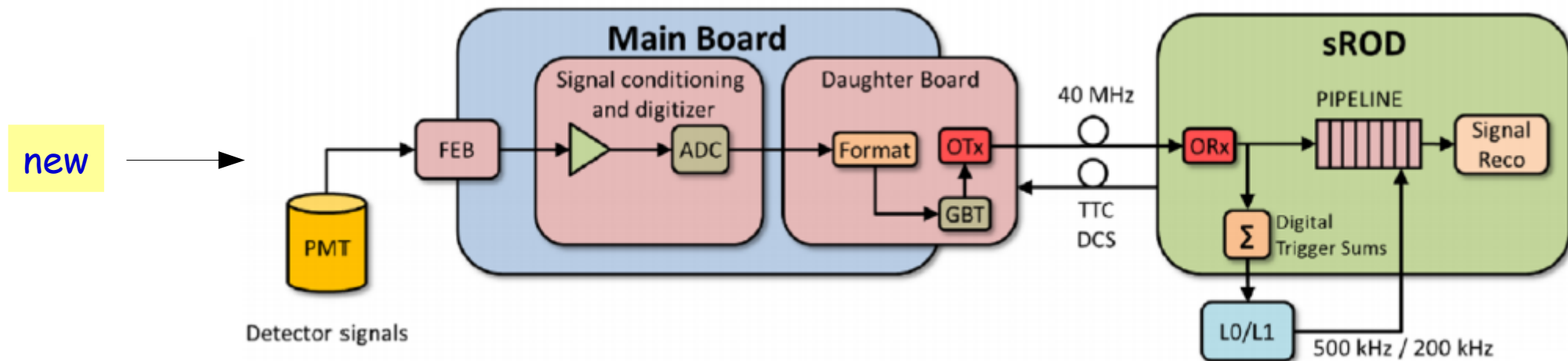
- Major TileCal electronics upgrade for the HL-LHC (Phase II)
  - higher radiation tolerance, faster and more modern electronics
  - allow better precision and finer granularity of the ATLAS trigger → all Tile signals digitized and sent off-detector @ bunch-crossing rate (40 MHz), requiring high bandwidth **readout philosophy changed !!**
  - increase redundancy and reliability
    - current electronics superdrawers split into 4 „mini-drawers”, mechanically and operationally independent



# Current vs new signal flow



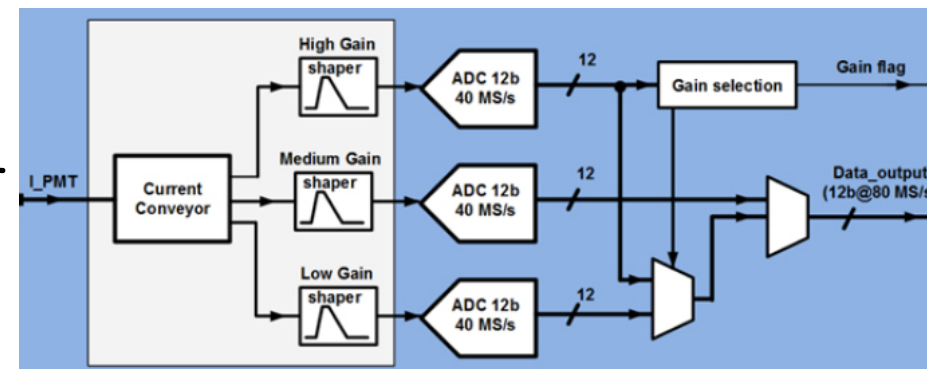
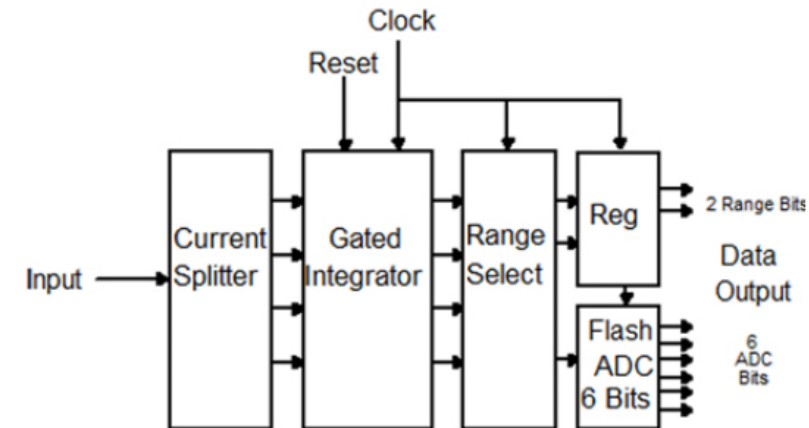
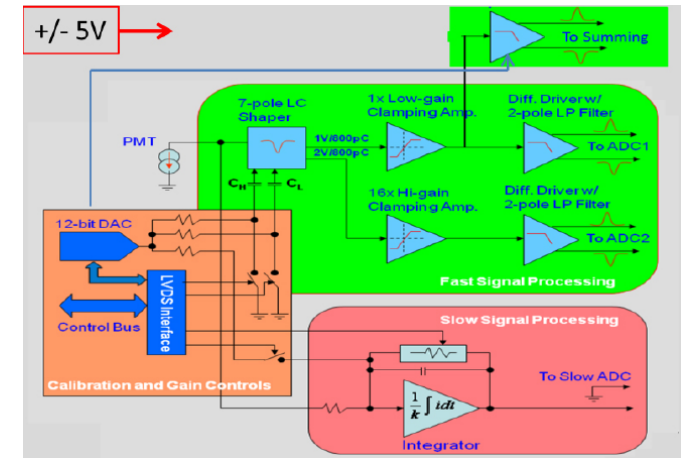
current



- Each Mainboard serves 12 channels (PMTs)
- Daughter boards communicate with off-detector electronics (sROD)
  - controlled by two Kintex-7 FPGAs
  - sent out digitized signals (at 40 MHz rate compared to current O(100) kHz) & receive slow control commands and route them to Mainboards

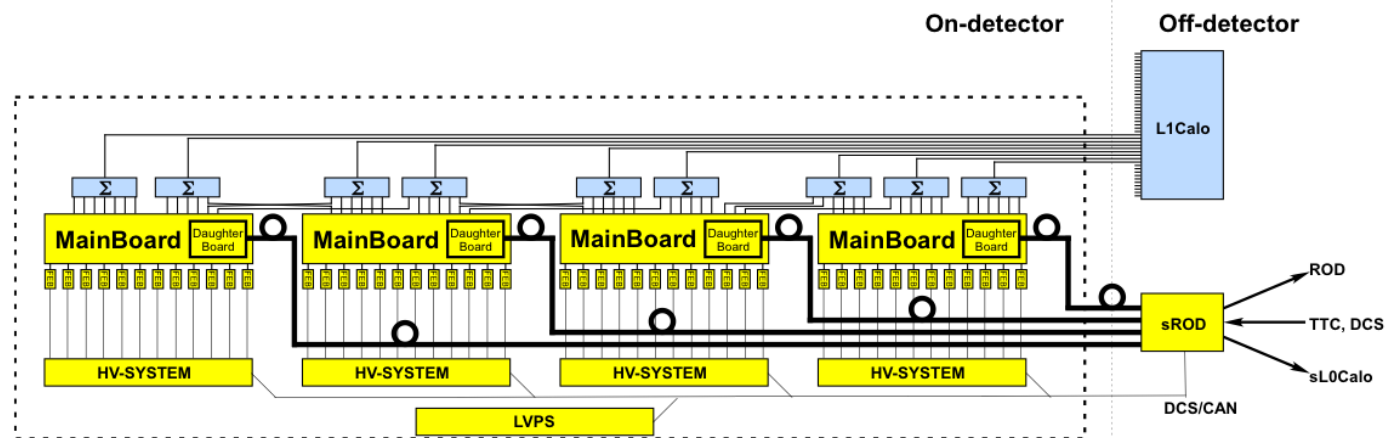
## Front-end board options

- Modified 3-in-1
  - pulse shaped and digitized with 12-bit ADC and 2 gains (1:32)
  - also provides CIS and slow integration (Cs and minimum bias)
- Charge Integrator and Encoder (QIE)
  - based on ASICs
  - no pulse shaping, digitization with 6-bit ADCs and 4 gains
- FATALIC
  - combination of two ASIC chips
  - pulse shaped and digitized with 12-bit ADCs and 3 gains (1:8:64)

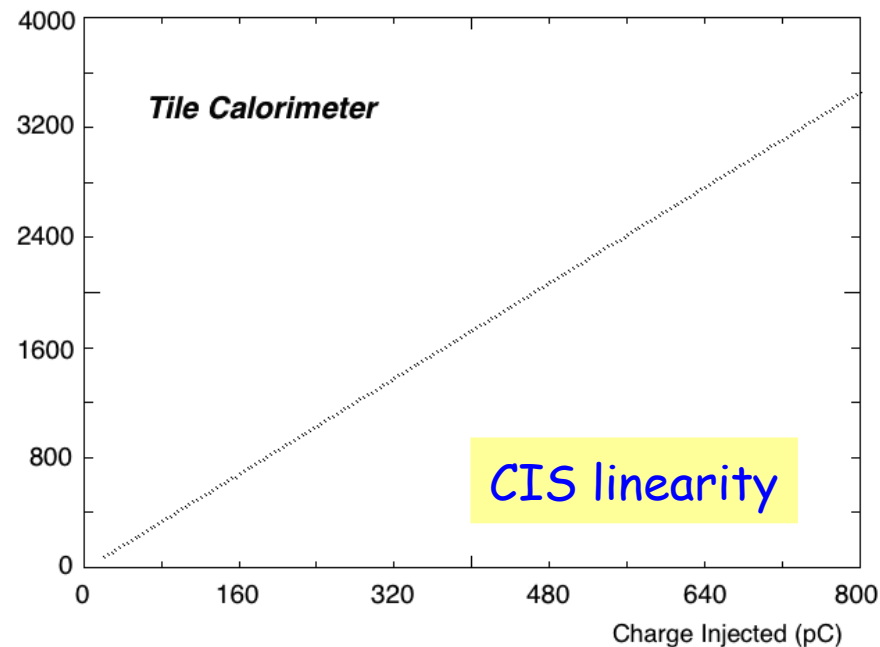
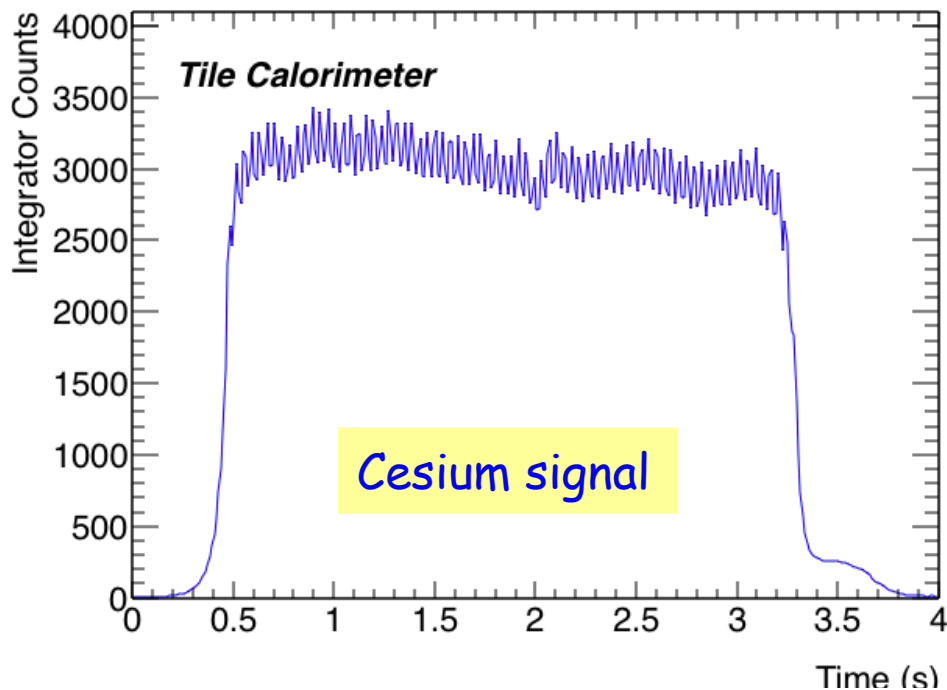


# Demonstrator (1)

- A hybrid prototype, compatible with both current and new electronics



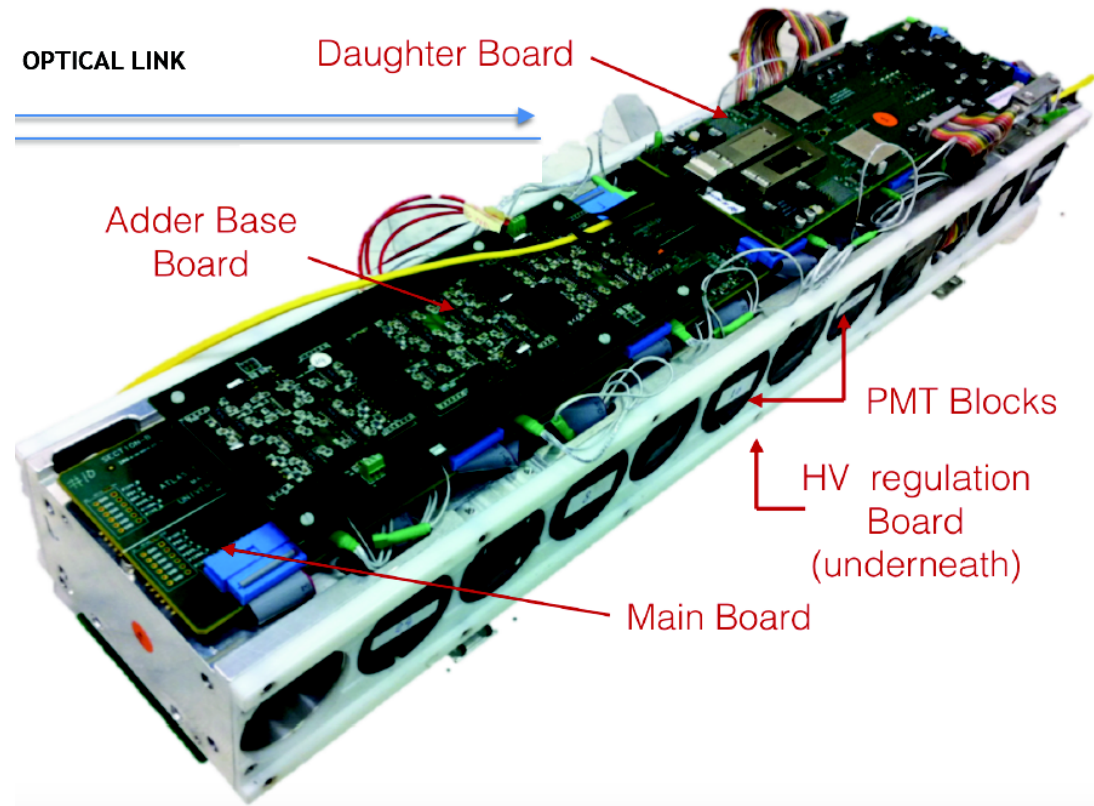
- Already built and tested in labs ...





# Demonstrator (2)

- ... as well as in testbeam (autumn 2015)
- Further intensive tests and two testbeam campaigns are planned this years, especially with other FEB options
- After successfull tests the demonstrator should be inserted in a Tile calorimeter module in ATLAS, maybe already at the end of this year



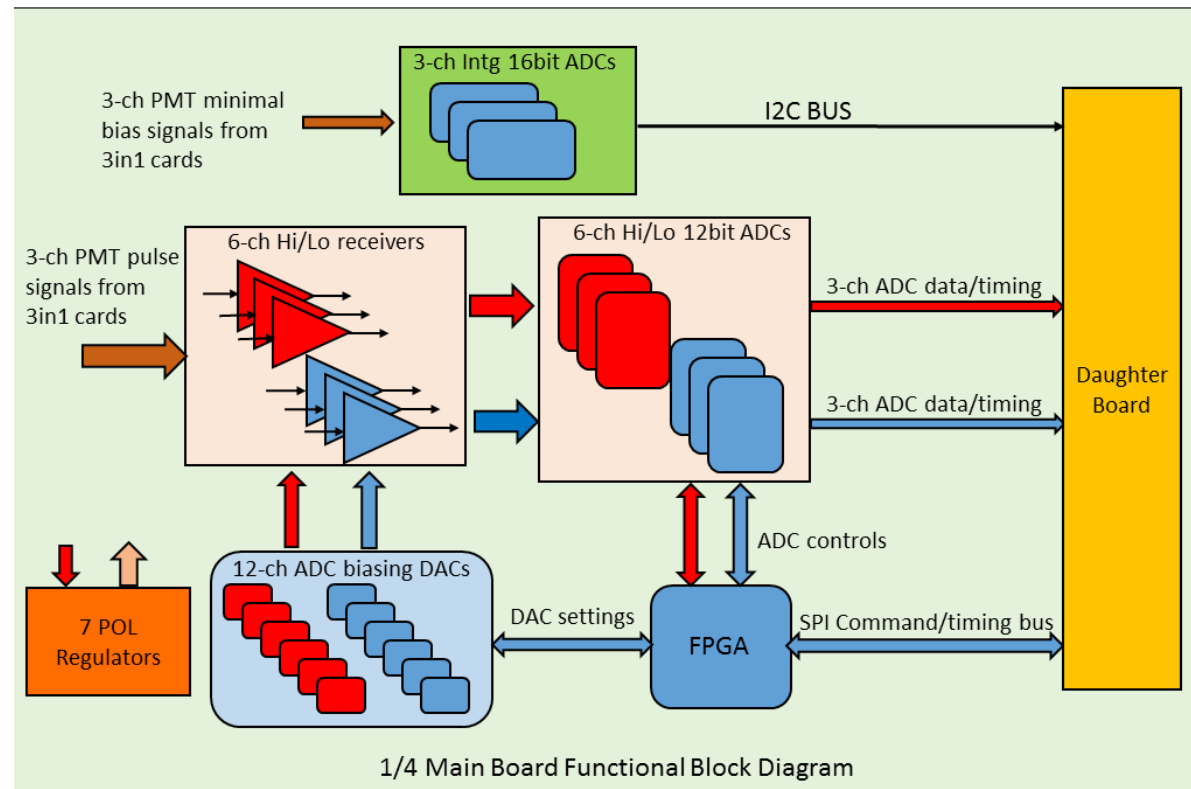
# Conclusions

- ATLAS Tile Calorimeter performs very well during LHC Run-1 and Run-2 so far, its contribution to many physics analyses is essential
- Calibration systems achieved precision better than 1%
- After detector consolidation during winter shutdown, we are even in better shape, looking forward for new Run-2 data !!
- For high luminosity LHC, Tilecal is on schedule to replace the readout electronics
  - intensive tests ongoing, demonstrator to be inserted in ATLAS at the next detector opening
  - optics system is expected to suffer from moderate radiation damage  
→ negligible impact on jet performance

# BACKUP

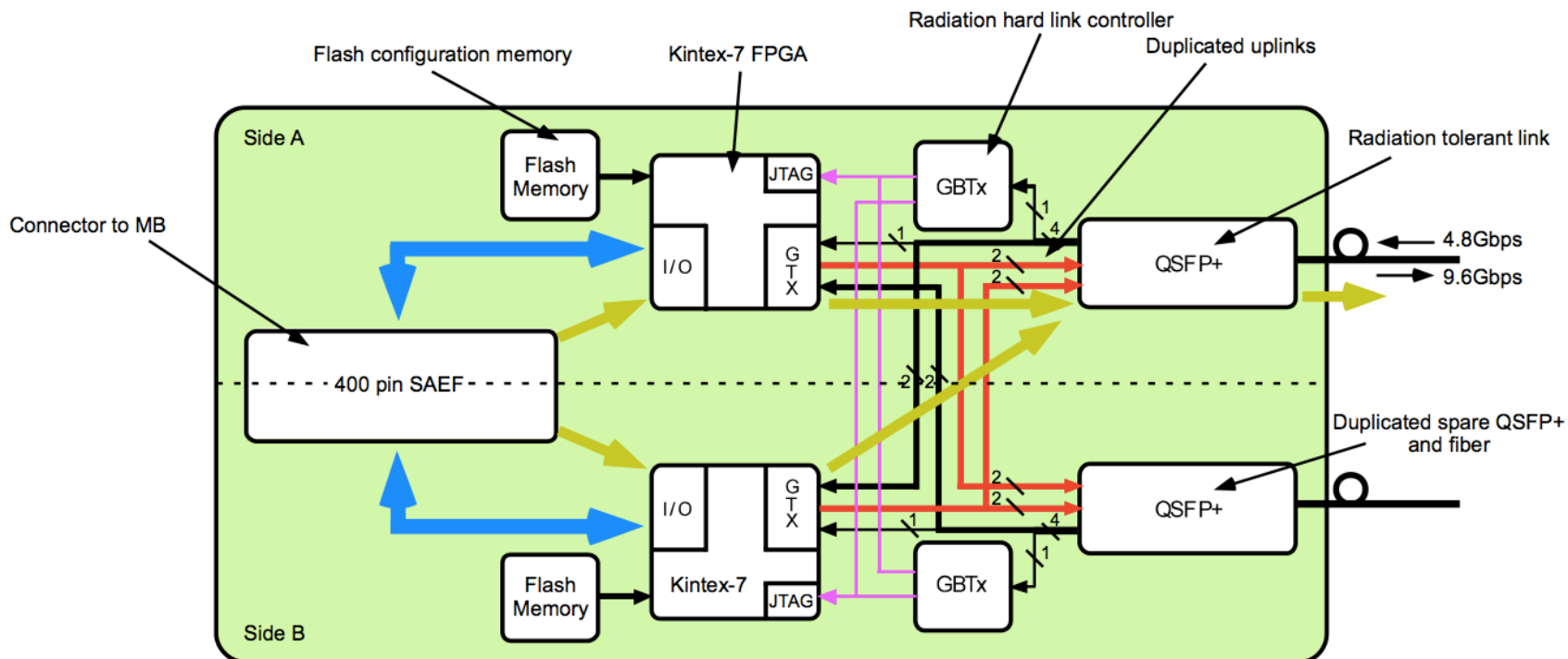
# 3-in-1 & Mainboard

- Diagram of  $\frac{1}{4}$  of a Mainboard for the 3-in-1 front-end option for the TileCal Demonstrator. Each quarter of the Mainboard serves 3 front-end channels for a total of 12 channels per Mainboard.
- for each channel it provides 16-bit ADCs for the slow integrator readout, receivers and 12-bit ADCs for high and low gains
- the interface with the back-end to transfer the data and received configuration and control signals is done through the Daughter board.



# Daughter board

- The board is divided in two parts which can be operated independently. Each half can readout up to 6 front-end channels.
- The communication with the Mainboard is done through a 400 pin FMC connector. The interface with the PreProcessor in the back-end is done through two redundant QSFP connectors.
- The system is managed by two Kintex-7 FPGAs while two GBTx chips are used to recover the system clock and provide remote reconfiguration of the FPGAs.



# Pre-Processor system

- Tentative block diagram of a Pre-Processor (PPr) system
  - one PPr system is able to process the data from 8 TileCal superdrawers. The PPr module is composed of a carrier with four mezzanine boards. The TDAQI provides interface with the FELIX (Front End LI nk eXchange) for DAQ and Trigger, Timing and Control.
  - depending on the final trigger level structure, the TDAQI will send preprocessed information to the Level 0 only (L0 option) or also to the Level 1 trigger Calorimeter systems (L0/L1 option).

