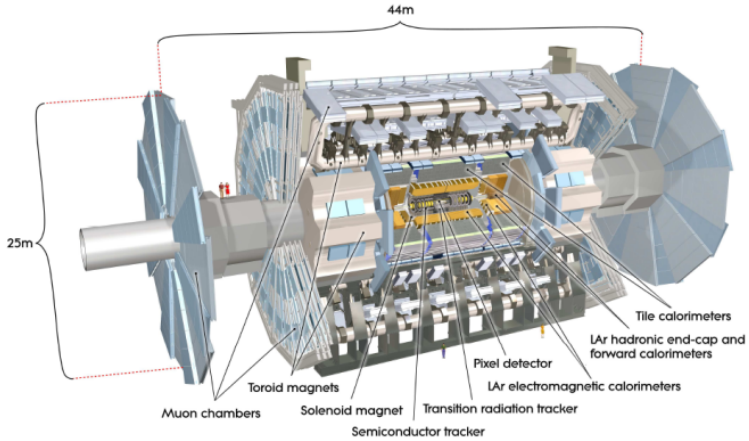


Future upgrades of the ATLAS detector for the High Luminosity -LHC (mostly ITk)

Sergio Díez Cornell
DESY

DESY

ATLAS EXPERIMENT

DESY LHC discussions, Hamburg, 08 June 2015

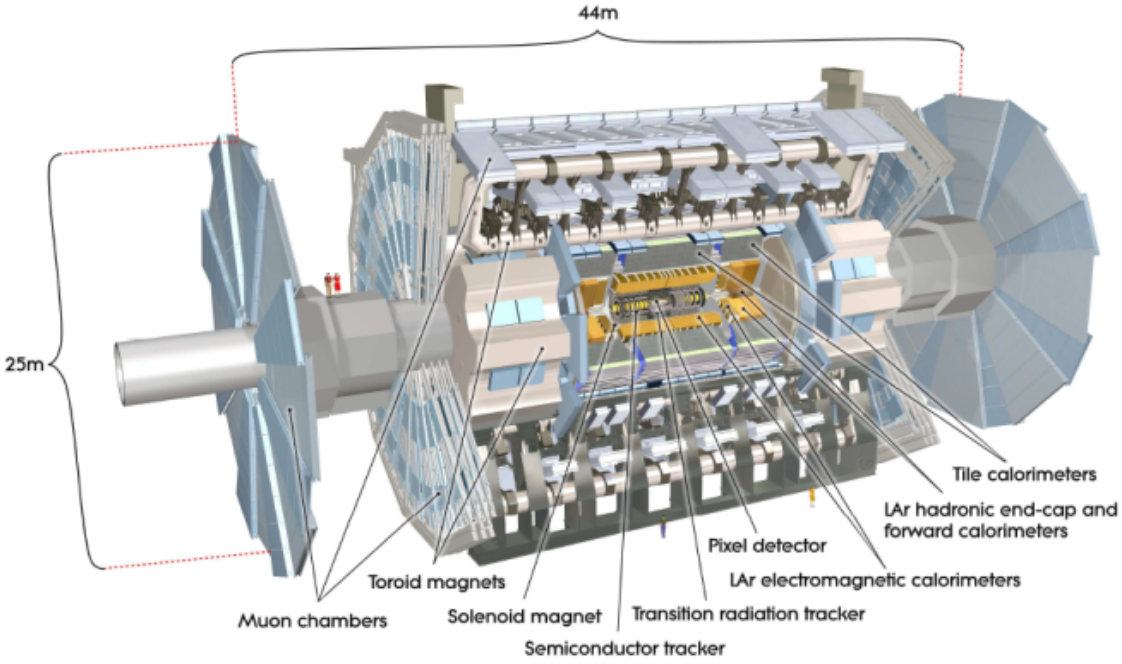
ATLAS

ATLAS detector

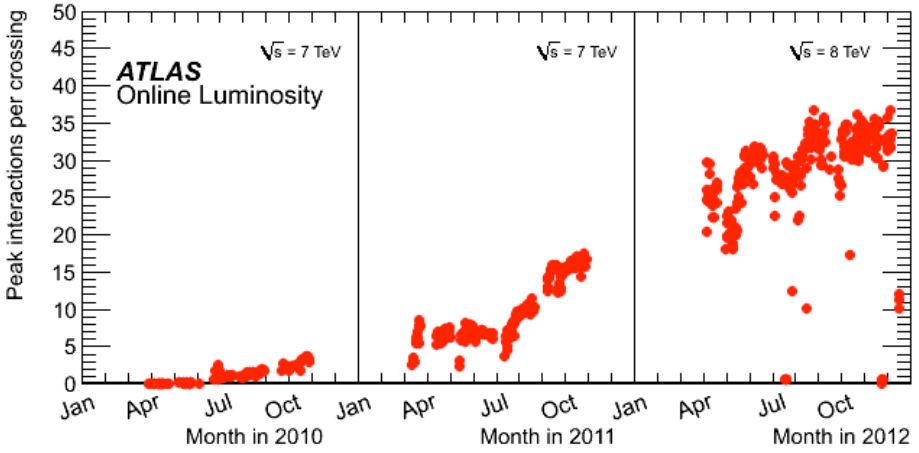
General purpose detector of the LHC

Sub-components:

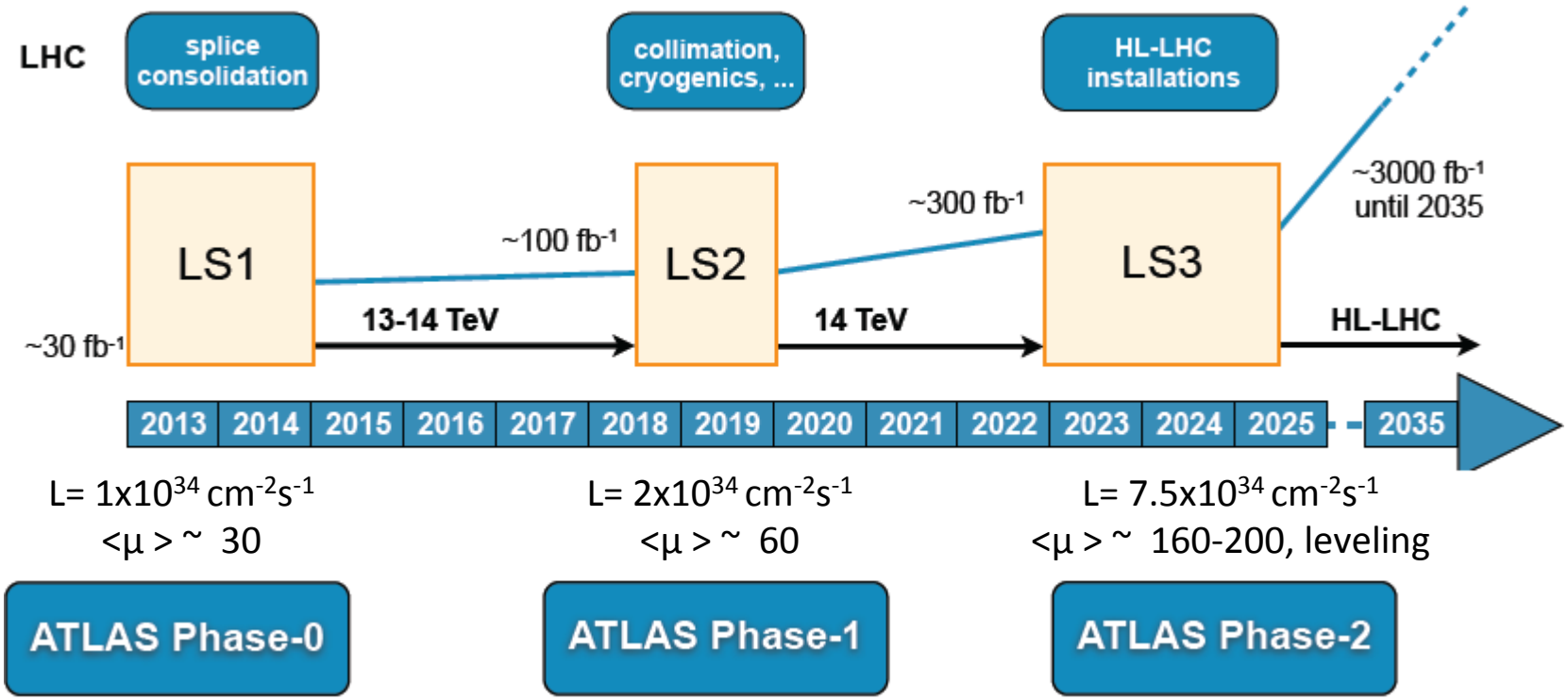
- Magnets
- Muon chambers
- Hadronic and EM calorimeters
- Inner detector
  - TRT, SCT, pixel



Outstanding performance so far!



The LHC schedule and future ATLAS upgrades



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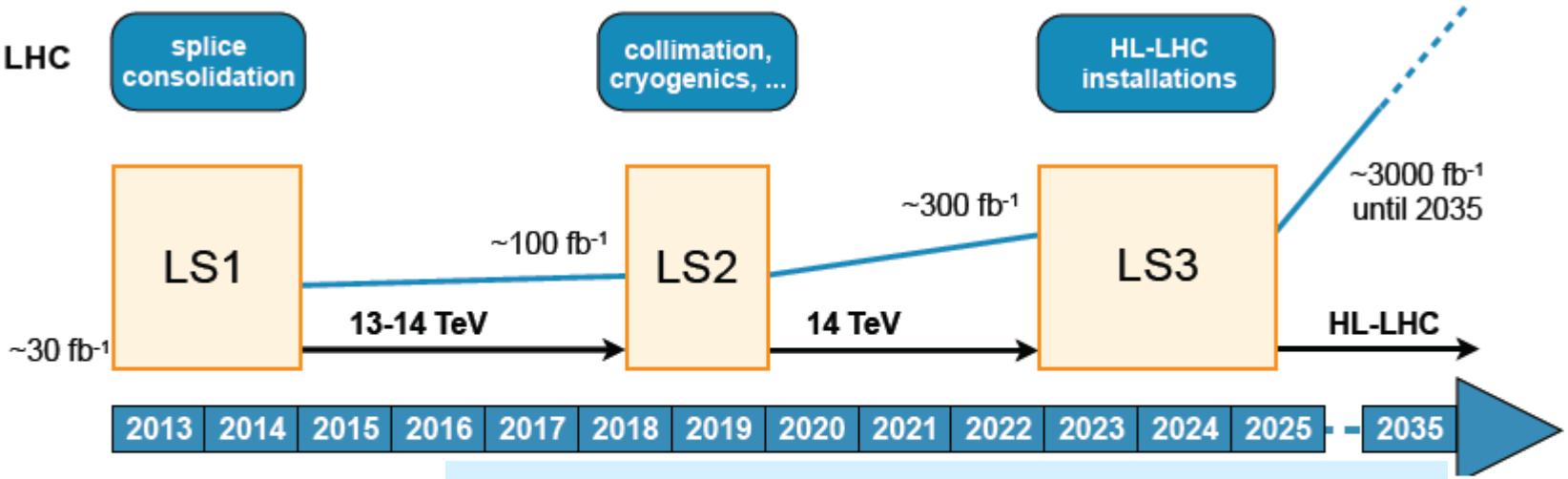


L= $1x10^{34}$ $cm^{-2}s^{-1}$

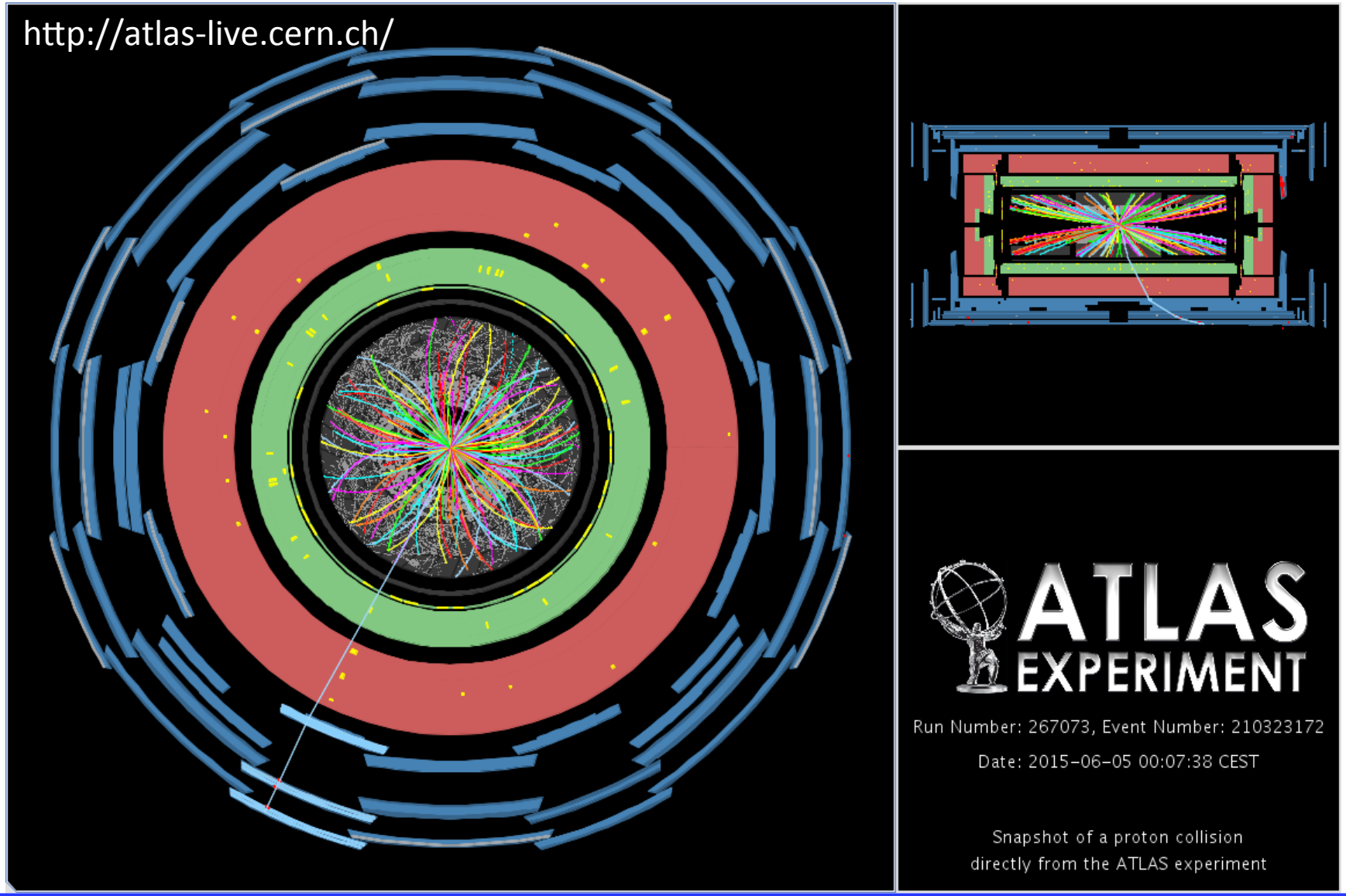
<μ > ~ 30

ATLAS Phase-0

Phase-0 upgrades

New Insertable pixel b-layer (IBL) and pixel services
New Al/Be beam pipe
New Inner Detector cooling
Upgrades to Level-1 Central Trigger
Detector consolidation (e.g. calorimeter power supplies)
Add specific neutron shielding
Finish installation of EE muon chambers staged in 2003
Upgrade magnet cryogenics

The LHC schedule and future ATLAS upgrades



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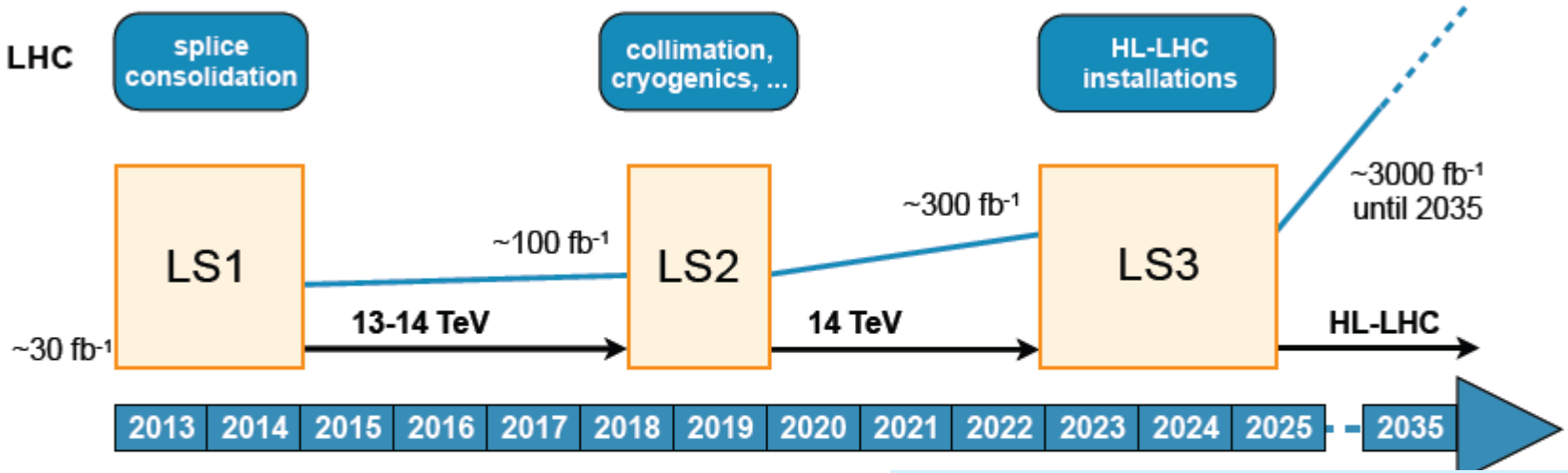


L= $1x10^{34}$ $cm^{-2}s^{-1}$
<μ > ~ 30

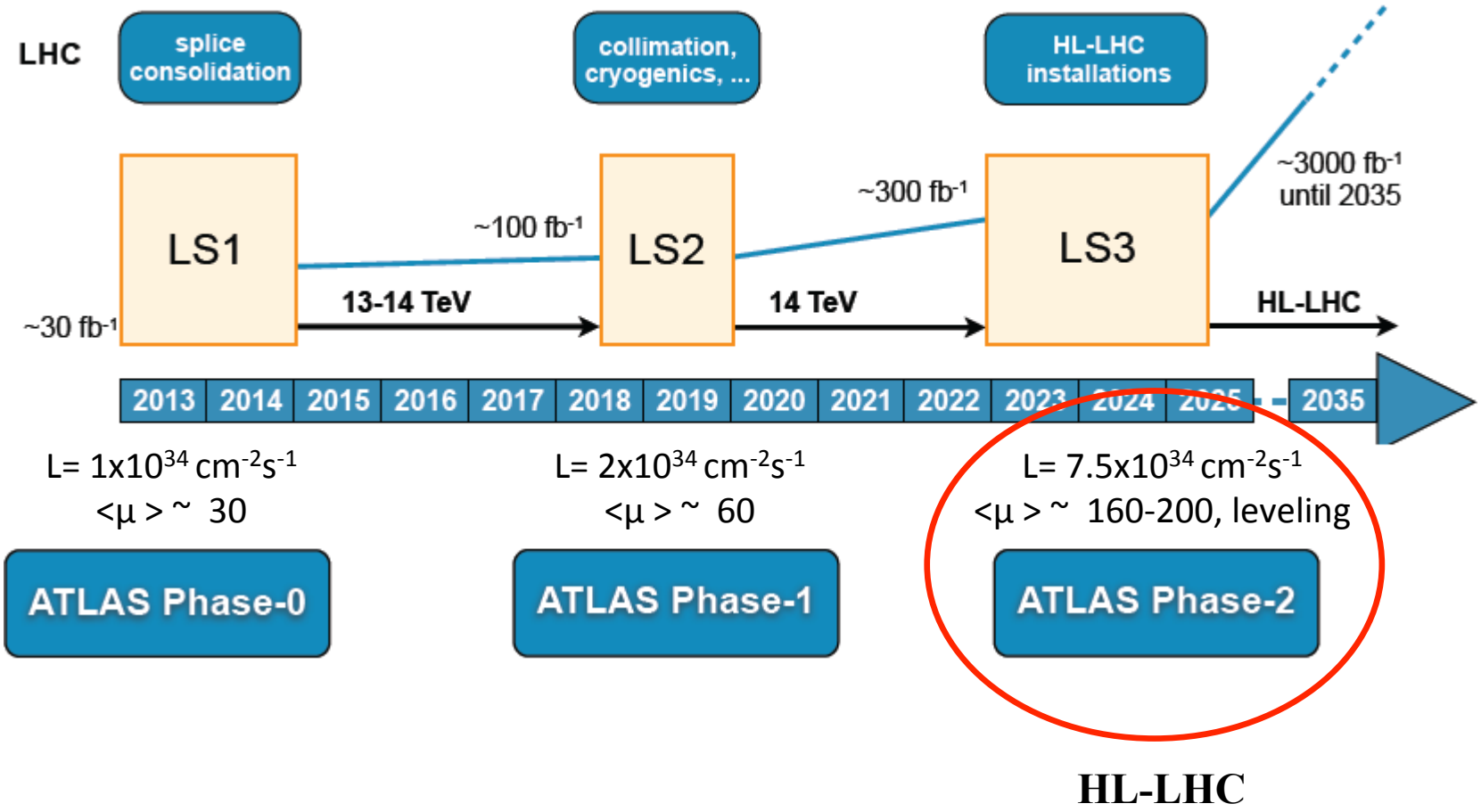
ATLAS Phase-0

L= $2x10^{34}$ $cm^{-2}s^{-1}$
<μ > ~ 60

ATLAS Phase-1

Phase-1 upgrades
New Small Wheel (NSW) for the forward muon Spectrometer
High Precision Calorimeter Trigger at Level-1
Fast TracKing (FTK) for the Level-2 trigger
Topological Level-1 trigger processors
Other Trigger and DAQ upgrades
ATLAS Forward Physics (AFP), proton det. at ±210 m

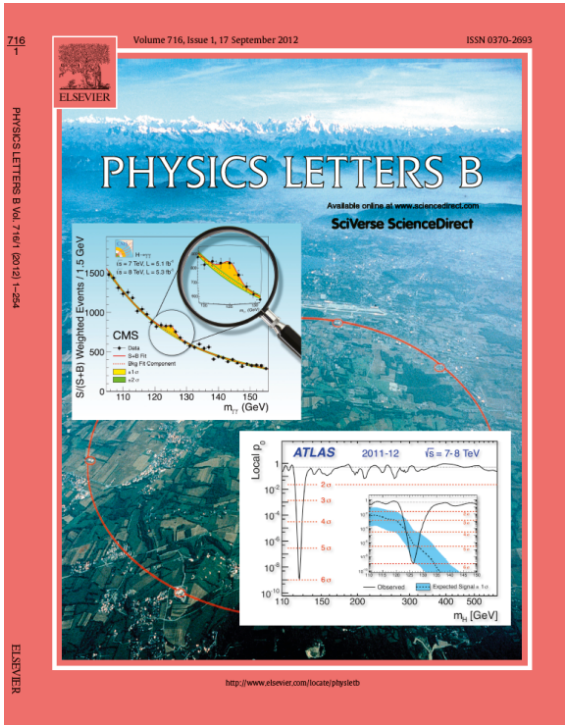
The LHC schedule and future ATLAS upgrades



HL-LHC

Motivation for HL-LHC

- Motivation:
  - Measurements on the 126 GeV Higgs boson
    - Improved precision of Higgs couplings measurements
    - Access couplings with new final states through rare channels (such as H→μμ)
    - Higgs-like self-coupling studied on new channels (such as HH →γγbb)
  - Probe for signatures of new physics (SUSY, extra dimensions) well into TeV region
    - Weak production of new particles potentially more important
  - Weak-boson scattering as another probe for EWSB beyond SM



Physics Letters B (716), 17th Sept 2012

Major upgrades on all detectors to maintain their excellent performances

Goals for HL-LHC

Physics

Study EWSB Mechanism	precision meas's of Higgs couplings (5-30%), Higgs self-coupling
Probe for signatures of New Physics	SUSY, Extra Dimensions, ...
Measure rare decay modes	Higgs, B, top, ...

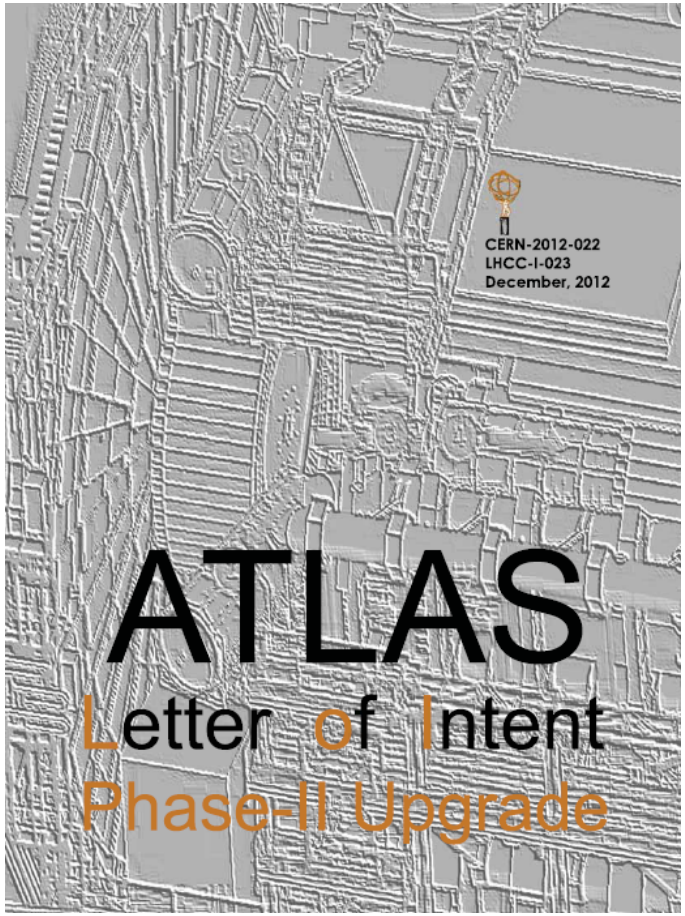
Detector Requirements

Example Physics/Detector Motivation	Requirement
complex SUSY cascades	Trigger & reconstruct low p_T e/μ
$H \rightarrow \tau\tau$	Trigger on τ's
High-mass gauge bosons	Good lepton e/μ momentum resolution at high p_T
Complex SUSY cascades	Identify Heavy Flavors
Resonances in top pairs, W, Z, H	Reconstruct leptons & b's in boosted topologies
VBF, Missing ET	Preserve acceptance in forward region
Efficient tracking with small fake rates	Radiation Tolerance and Granularity
Impacts Front End electronics	Compatibility with new trigger system

Hal Evans

The ATLAS Phase-II upgrade

- Upgrades on ATLAS sub-detectors
  - Tracking
    - Major revision, new Inner tracker including LVL1 trigger capability + new services
  - Calorimetry
    - New Front and back-end electronics, including trigger, new forward calo if proven necessary, fix LAr hadronic cold electronics if necessary
  - Muon system
    - Increase trigger capability in the big wheels, add additional trigger inner layers in the barrel. New FE electronics
  - Trigger/DAQ
    - Major revision
  - Common systems
    - New TAS (collimator) and forward shielding, major infrastructure consolidation, including safety systems



http://cds.cern.ch/record/1502664?ln=en

ATLAS Phase-II LoI released on Jan 2013

The ATLAS Phase-II upgrade

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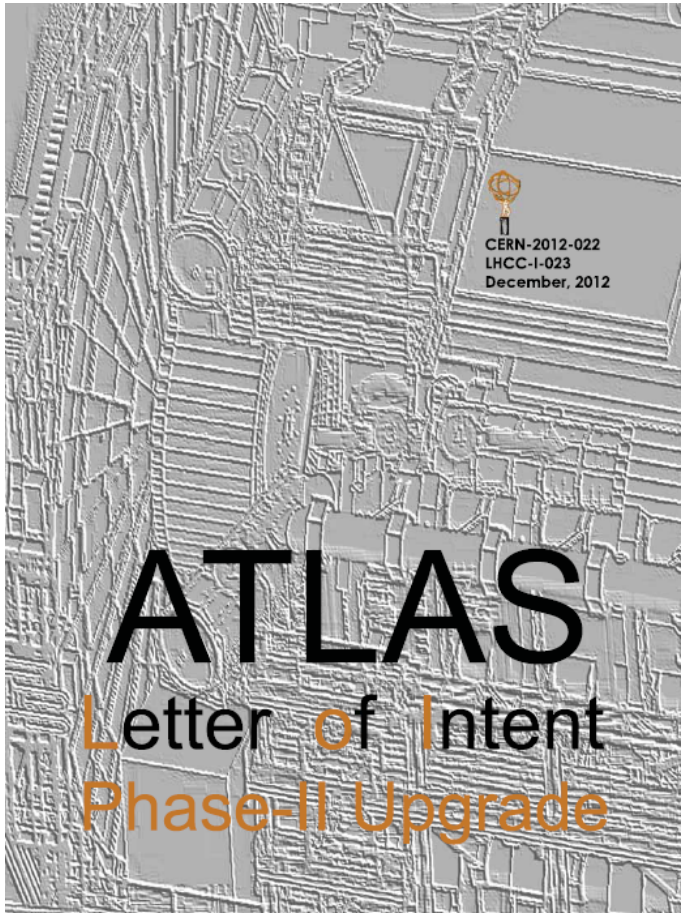
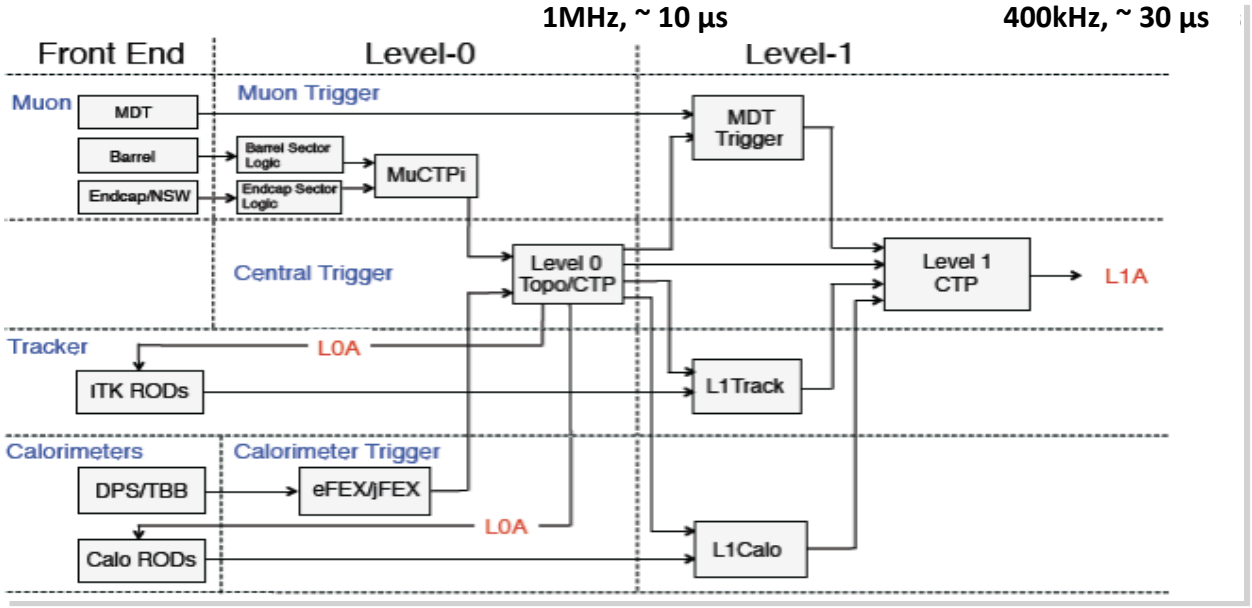


http://cds.cern.ch/record/1502664?ln=en

ATLAS Phase-II LoI released on Jan 2013

New Phase-II L0 and L1 trigger



- 2-level system at Phase II
- Phase-I L1 becomes Phase-II L0, new L1 includes tracking
- Make use of improvements made in Phase 1 (NSW, L1Calo) in L0
- Introduce precision muon and inner tracking information in L1 (better muon p_T resolution, track matching for electrons,...)
- Move part of the "offline" High Level Trigger (HLT) reconstruction into the early stage of trigger (additional p_T info on triggering leptons, reduce L1 rates)
- Requires changes to detector FE electronics feeding trigger system
- Drives ITk bandwidth requirements.

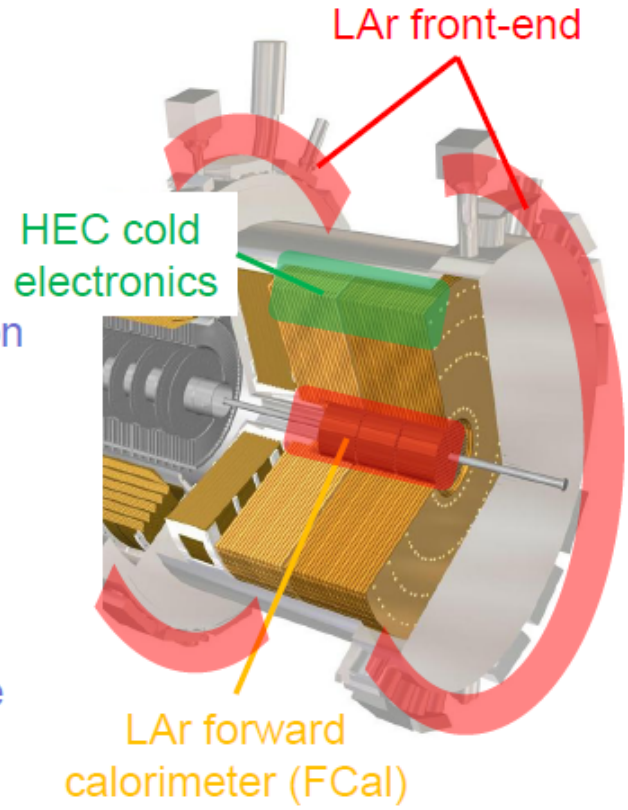
LAr Calorimetry upgrades

- The following LAr Calorimeter components require an upgrade for the HL-LHC phase:
  - LAr front-end electronics
  - LAr back-end electronics
  - HEC low-voltage power-supplies

  } *necessary* due to:
  - new ATLAS trigger scheme in Phase-II
  - radiation tolerance
  - ageing of components

- The HEC cold electronics inside the endcap cryostat is not foreseen to be replaced

- LAr detector upgrade:
  - high-granularity sFCal → high Phase-II cost option
  - Si/W 4D precision timing detector on front face of endcap at $2.4 < \eta < 4$ → high cost option
  - MiniFCal: LAr/Cu, Si/W, Diamond/Cu
    → LAr/Cu MiniFCal in normal/low cost option in case FCal performance and/or operation are degraded



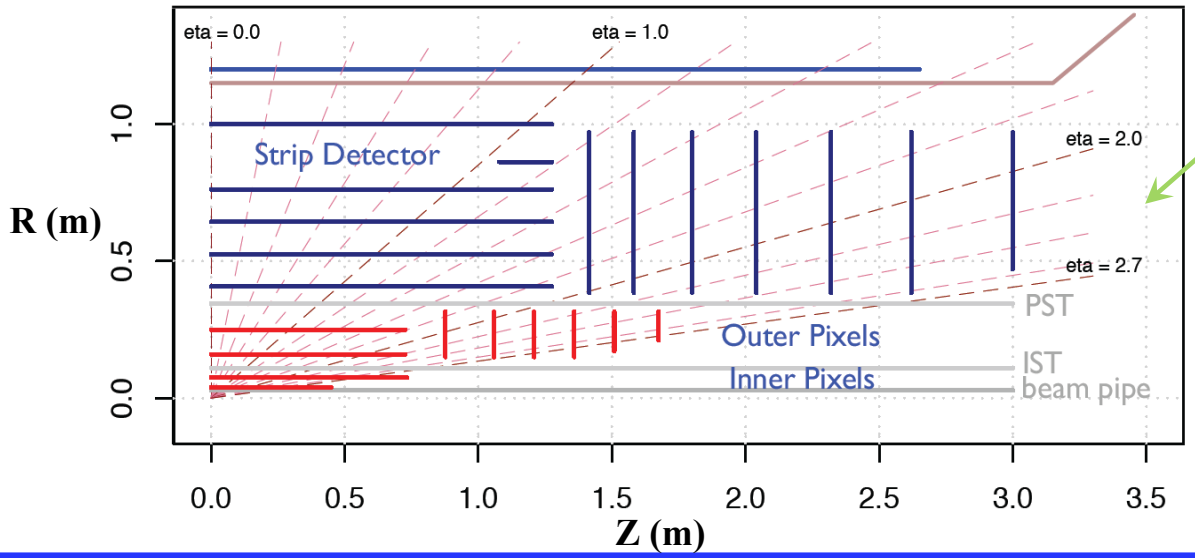
A. Strässner, AUW Apr 2015

A new ATLAS silicon tracker

- Challenges for silicon sensors
  - Higher granularity to keep same low occupancy
  - Higher radiation tolerance to deal with increased radiation environment
  - Novel powering solutions to power efficiently x7.5 more channels
  - Reduce material and cable count in the tracking volume to keep detector performance
  - Reduce pitch to improve performance at high p_T
  - Reduce cost per sensor to cover larger area (~ 200 m^2)

Replacement of ATLAS Inner detector by an **all-silicon tracker**

"LoI layout" for the Phase-II Silicon tracker (Jan 2013)



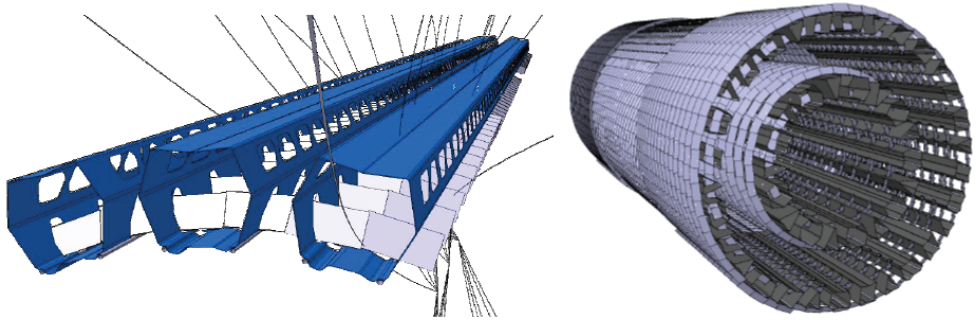
Strip detector "Staves" in the barrel
"Petals" in the endcaps

	Silicon Area	Channels [10^6]
Pixel	8.2m^2	638
Strip	193m^2	74

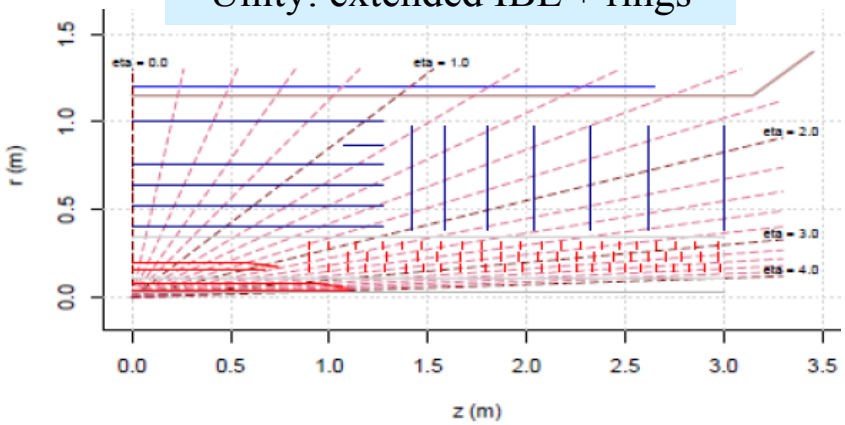
ITk pixel layouts

- MANY different pixel layouts under consideration:
  - LoI, LoIVF
  - Rings, ringsVF
  - Extended Inner barrel
  - Unity
  - SLIM
  - Alpine
  - HV-MAPS

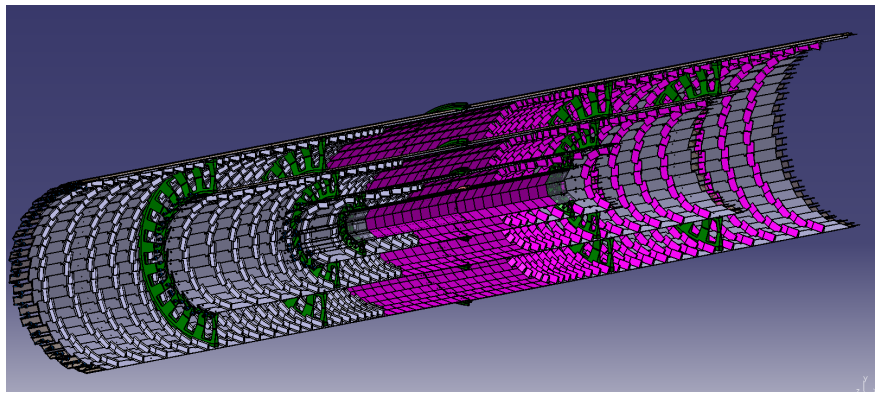
SLIM: Stiff Longeron for ITk Modules



Unity: extended IBL + rings



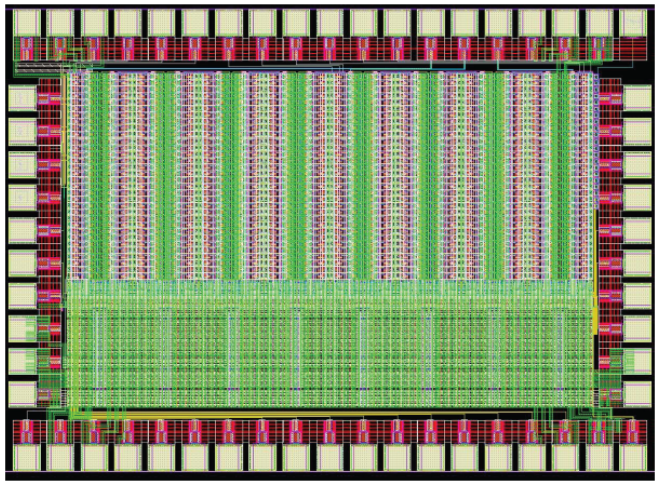
Alpine: rings not included



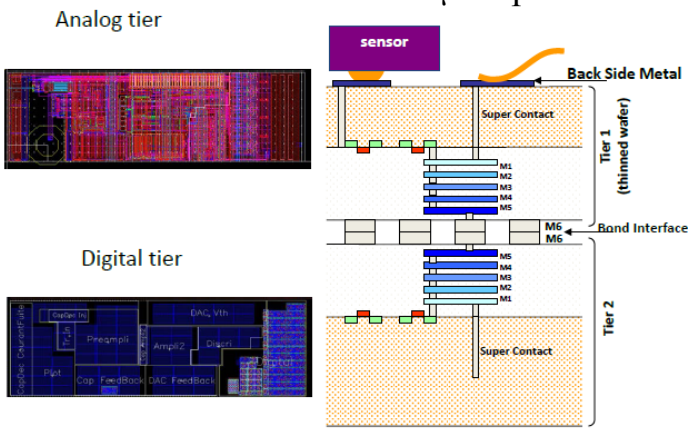
Pixel sensors and FEE

- Pixel sensors:
  - Two outer layers: planar n-in-n, n-in-p pixels (150 μm thick)
    - Operational at the expected fluences, cheap, large number of vendors
    - HV CMOS another alternative, especially for outer 5th layer
  - Several options still open for the sensor technology on the 2 innermost layers (<150μm thick to take advantage of increased granularity)
    - **Planar n-in-n**: lower cost, high yield, multiple vendors
    - **3D**: Low depletion V even after irradiation, extremely rad-hard, more expensive
    - **Diamond**: Promise lower capacitance, rad-hard, low dark current (no cooling?), expensive
- Front-End Electronics:
  - Outer layers: **FE-I4-C** (50x250 μm^2 pixel size)
  - Inner layers (25x150 μm^2 pixel size)
    - **65 nm CMOS:** RD65 to develop the next generation of chips
    - **3D integration** (Trough Silicon Vias, TSV)
    - Prototype ASICs fabricated on both technologies with good performances
    - Extensive R&D in progress, wait for appropriate time to make decisions, cost is a driver

65 nm test chip with 16 x 32 pixels (pixel size 25x 150 μm^2)

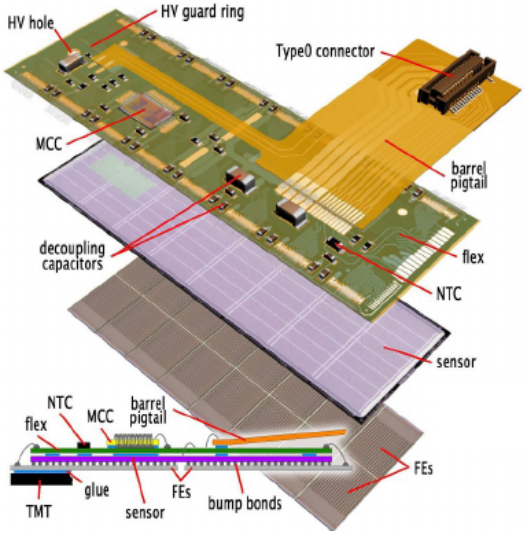


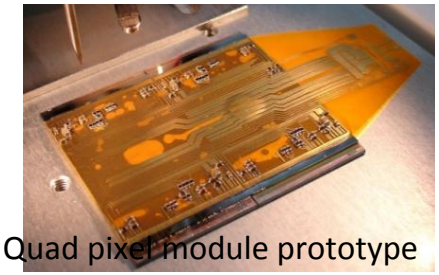
TSV ASIC for 50x166 μm^2 pixels



Pixel modules, interconnects, powering

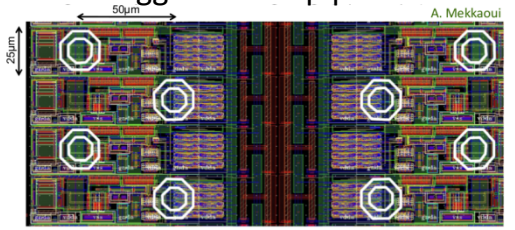
- Current baseline pixel module layout based on existing solutions
  - Hybrid pixel approach with planar or 3D sensors under investigation.
  - CMOS monolithic approaches emerging and interesting for larger radii
- 3 different flavors of modules:
  - **2-chips modules** (4 x 2cm^2) for the 2 innermost layers
  - **4-chip modules** "quads" (4 x 4cm^2) for the 2 outer layers and disks
  - **Hex modules** (6 x 4cm^2) for the disks
  - Shared COM and CLK line for all chips in the module, but several dedicated data outputs
  - Strong prototyping effort with FE-I4-B ASICs
- Interconnections: **flip chip bump bonding**
  - Bump pitch 50 μm, staggering of bump pads for 25 x 125 μm^2 pixels
  - Many alternatives, widely demonstrated with FE-I4-B and 65 nm CMOS for 25 x 125 μm^2
- Powering: **Serial power baseline**, on-chip DC-DC under investigation





Quad pixel module prototype

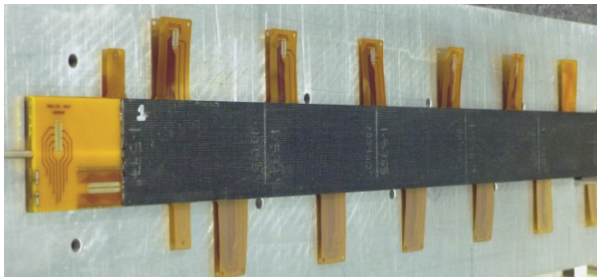
65 nm CMOS prototype ASIC with staggered bump pads



Pixel support structures

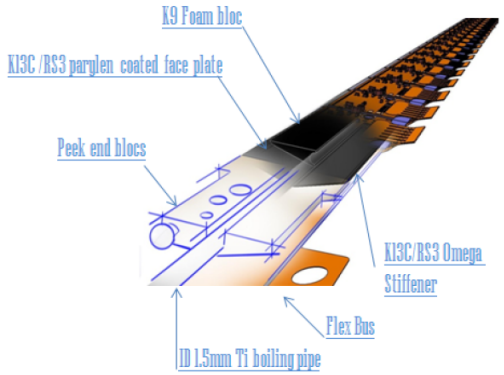
- Many alternatives driven by different layouts
- Improved IBL stave for outer layers
  - Alternative: flat stave
    - 1.4 m stave with embedded tapes recently fabricated
  - Other approaches for different layouts (SLIM, Alpine)

1.4m flat stave

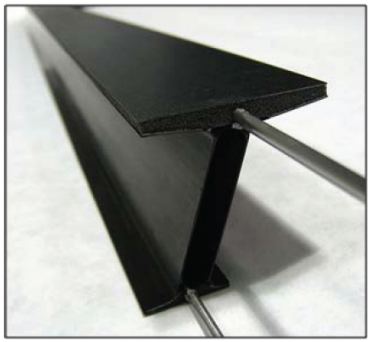


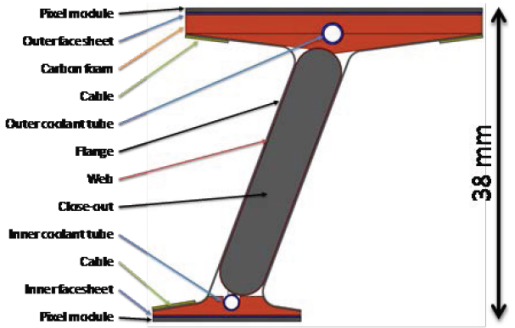
- I-beam staves for 2 innermost layers
  - Carbon composites and thin Ti cooling pipes
  - Accommodates both layers in the same structure, stiff, low material budget, fast replacement
  - 1000 mm I-beam TM prototype already fabricated with excellent performance

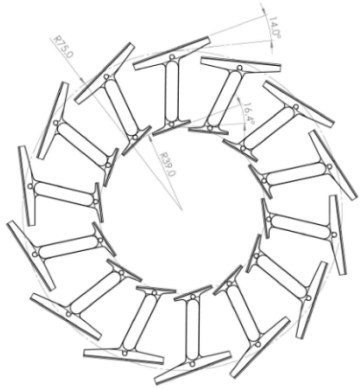
IBL stave



I-beam stave concept and prototype

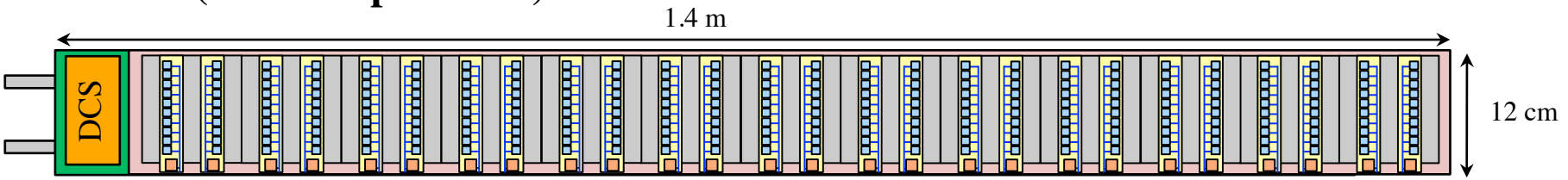






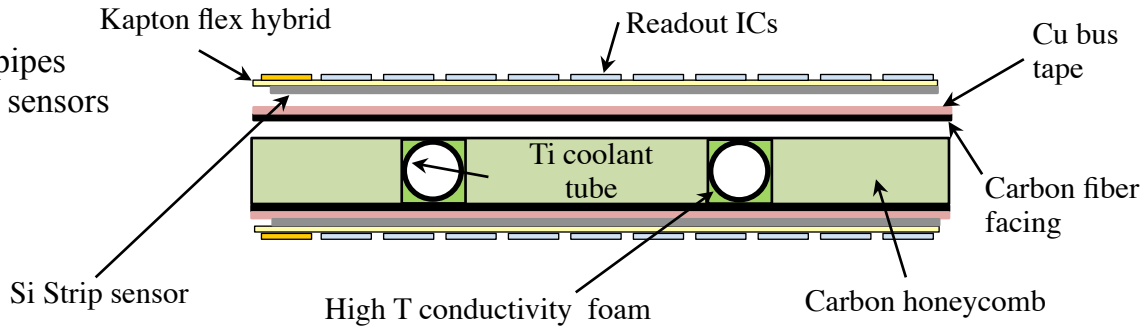
The strips tracker: stave and petal concept

Barrel stave (short strip version):



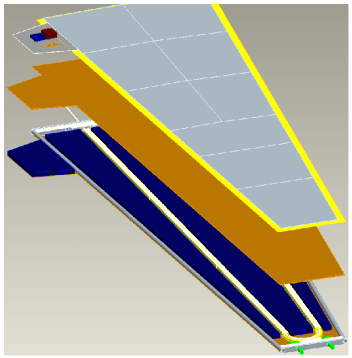
- Designed to minimize material
  - Shortened cooling paths
  - Module glued to stave core with embedded pipes
  - No substrate or connectors, hybrids glued to sensors
  - Minimizes cable count
- Designed for large scale assembly
  - Simplified build procedure
- All components testable independently
- Aimed to be low-cost

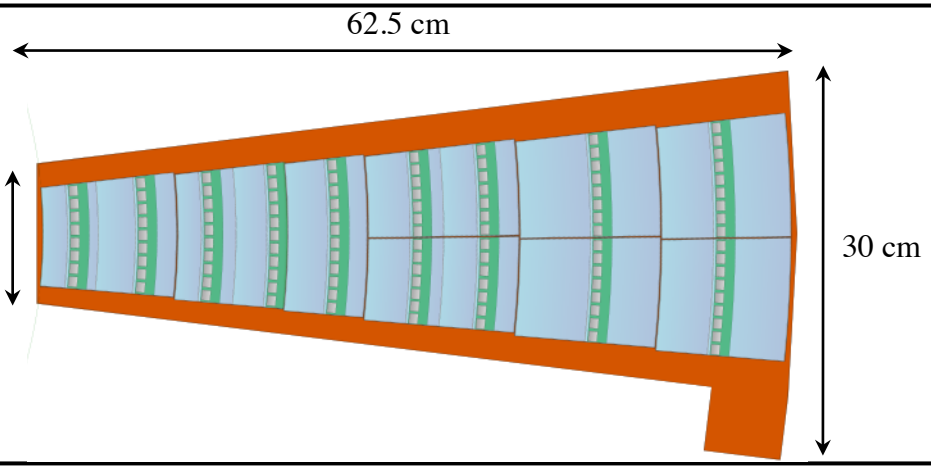
Stave cross-section:



Endcap petal:

- Follows barrel design
- 9 sensor modules per side (6 flavors of modules, 13 flavors of hybrids)





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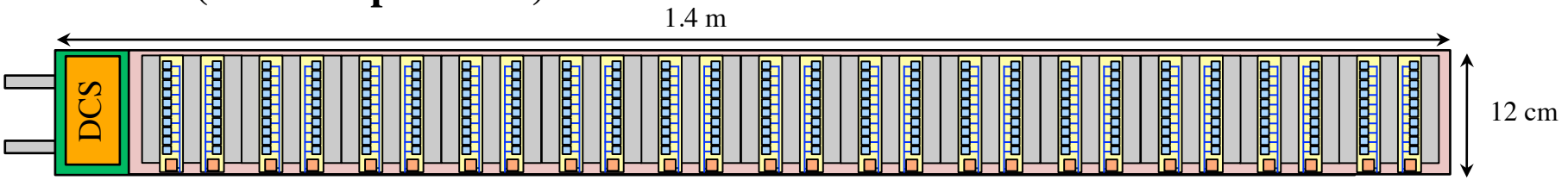

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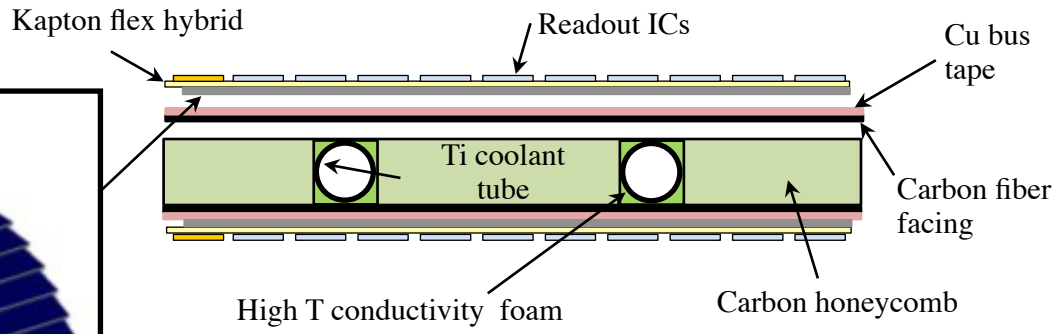
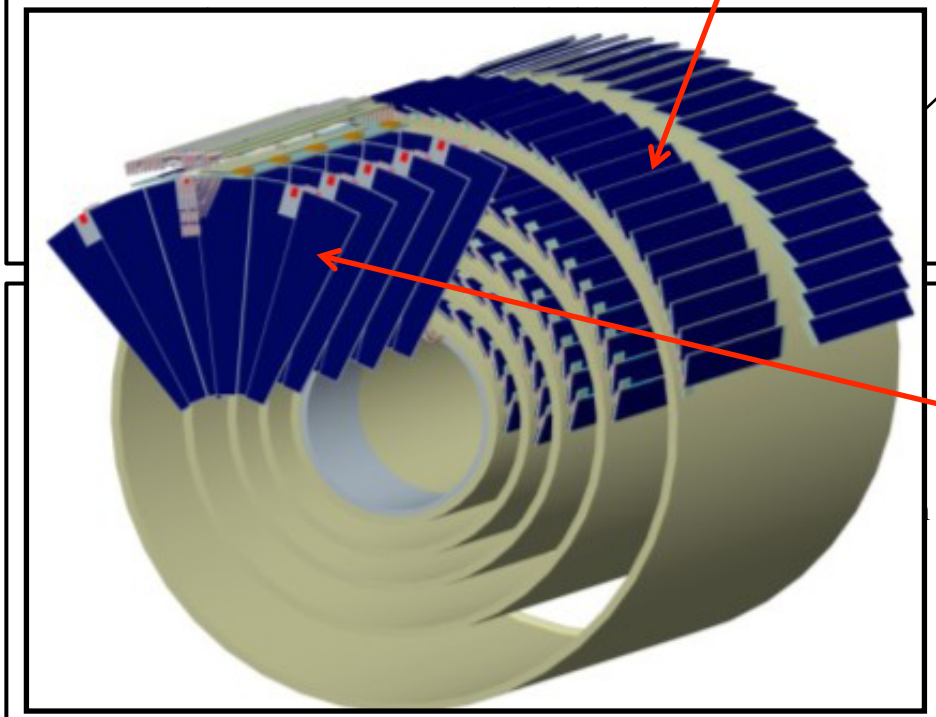
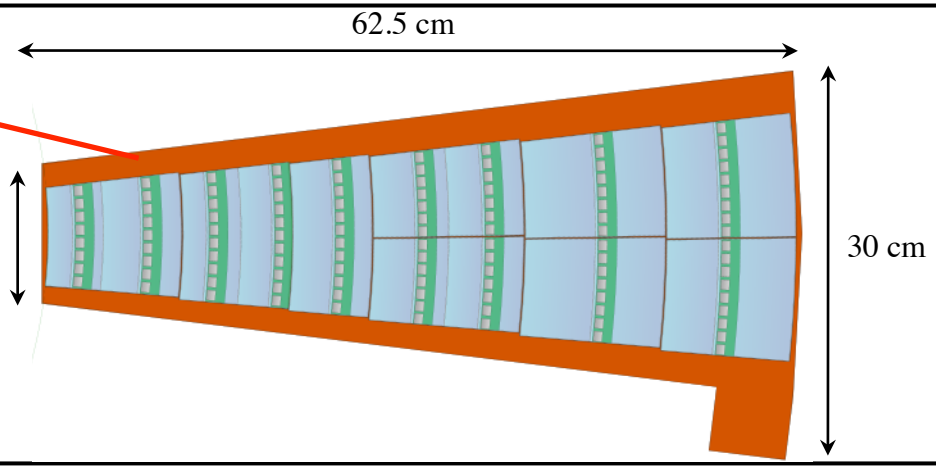
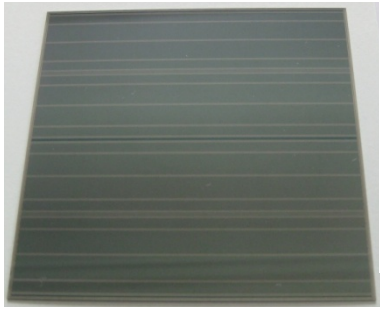


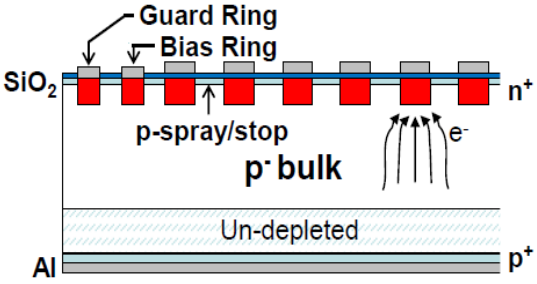




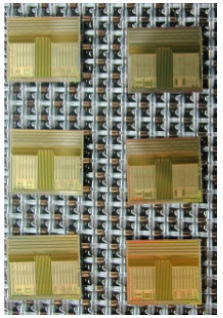
Strip module prototypes

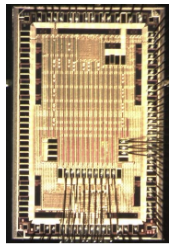
- **Silicon sensors**: n^+ strips in p-type substrate (n-in-p)
  - Collects electrons (as opposed to current p-in-n), depletes from segmented side, single-sided process
  - 9.75x9.75 cm^2 sensors fabricated on 6" wafers in collaboration with Hamamatsu Photonics
  - Barrel: rows of 1280 strips, 74.5 µm pitch, 2.5 cm long (short strips), 5 cm long (long strips)
  - Meet electrical specifications, also after irradiation

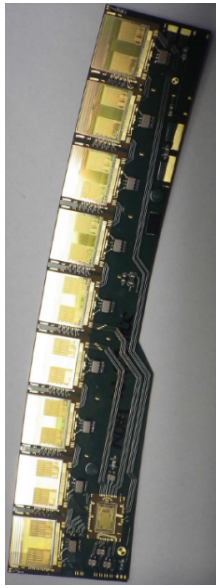




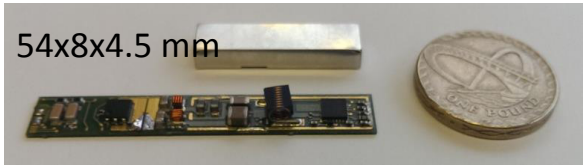
- **Readout and control electronics:** ABCN130 and HCCs (130 nm CMOS from IBM)
  - **ABCN130**: 256 binary readout channels per ASIC, connected to sensor strips via wirebonds, mounted on **low-mass flex hybrids** (substrate-less, no connectors)
  - "Star" versions of ABCN130 and HCCs on preparation in order to cope with 1 MHz L0 trigger rate







- **Power and protection circuitry**: DC-DC converters (DC-DC)
  - **Buck DC-DC converters**: custom low-mass inductor and shield + FEAST ASIC (0.35µm LDMOS)



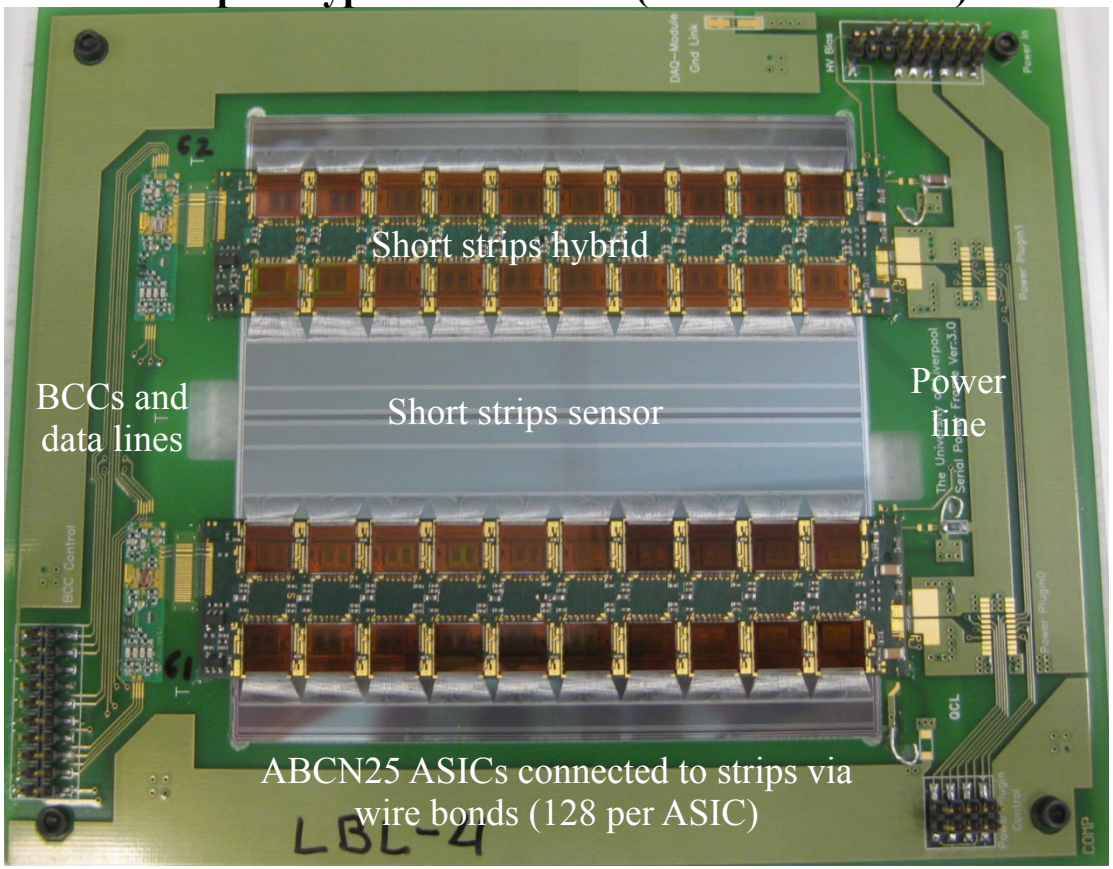
Silicon microstrips modules

Barrel short strips modules:

9.75 x 9.75 cm sensors

4 x 1280 strips (2.45 cm long, 74.5μm pitch)

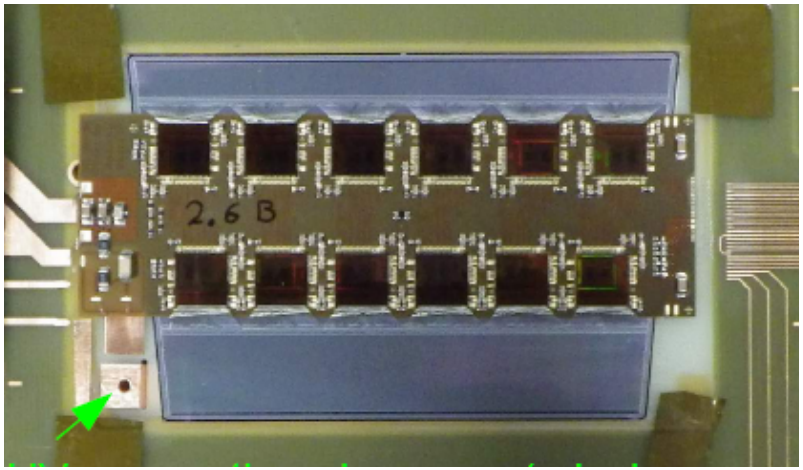
Former prototypes use ABCN25 (128 channels each)



~21000 strip modules required for the tracker

Endcap modules:

Different sizes along r dimension (this one: 2 x 768 strips (2.45 cm long, max. 75 μm pitch))



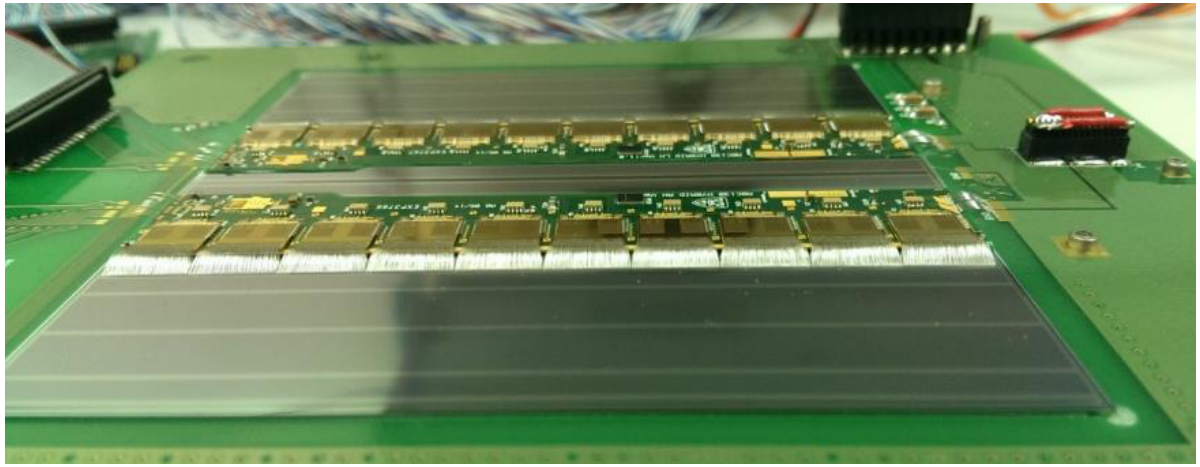
Fully testable modules, ready for stave assembly

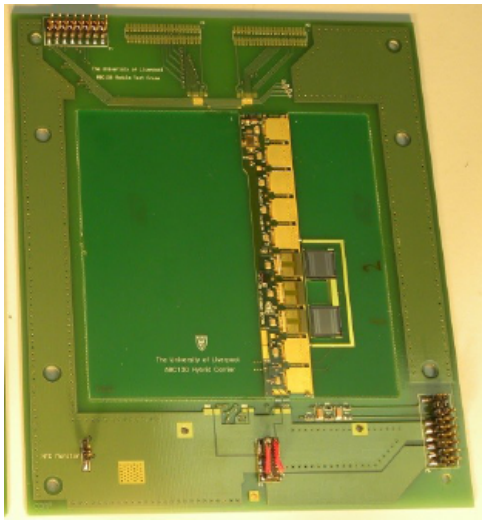
Module construction designed for large scale production even at prototyping stage

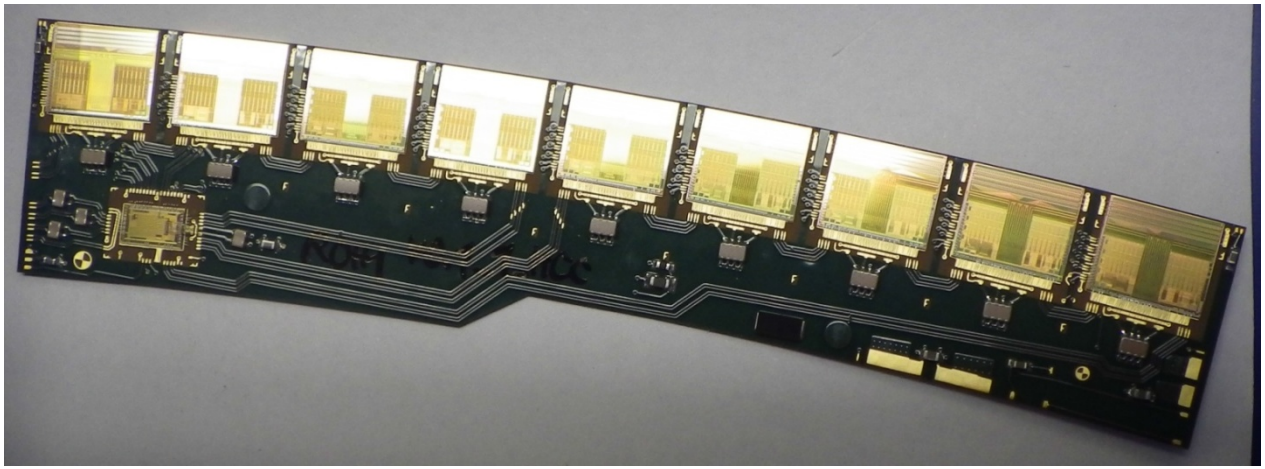
More than 100 modules produced so far by the stave community (> 20 institutes worldwide)

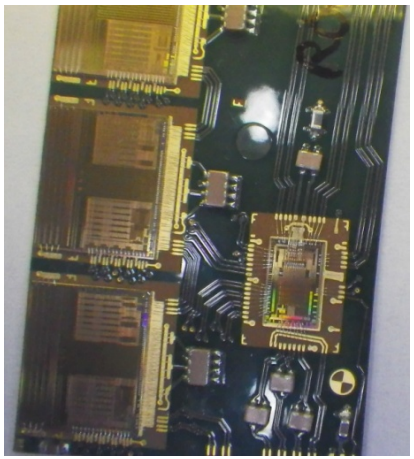
Silicon microstrips modules

- First ABCN130 barrel and endcap prototypes being produced





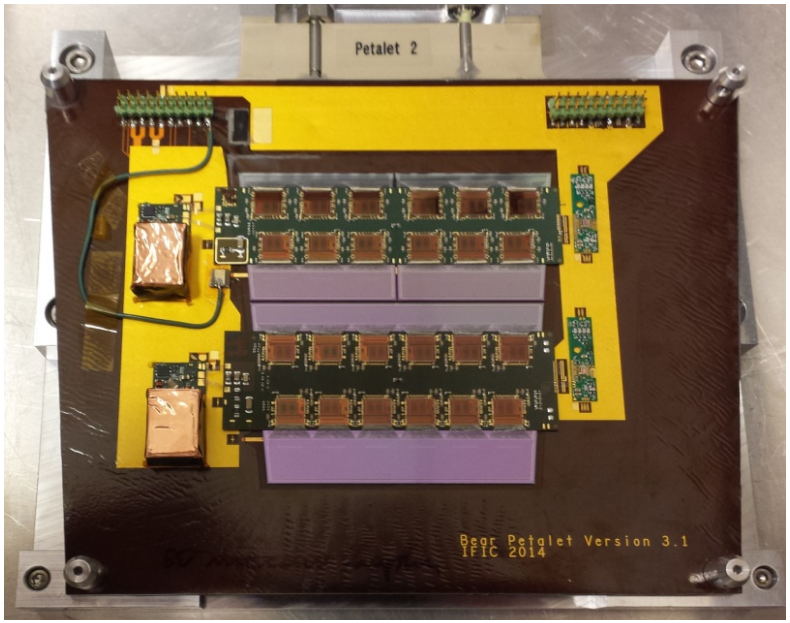


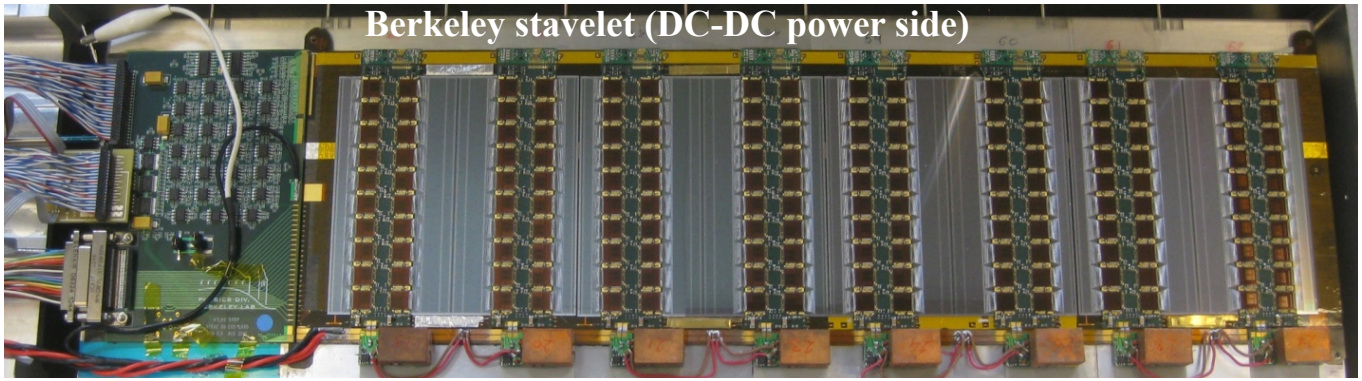


Staves and petal structures

"Stavelets" and "petalets": shortened short strip prototypes

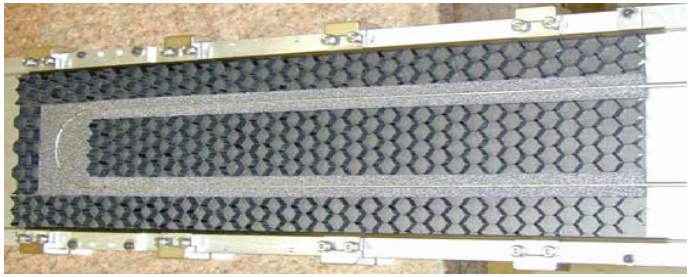
- Key test bed for electrical testing, powering, protection, G&S, understanding complexity of building and handling procedure,…
- Single- and double-sided serial and DC-DC powered prototypes built and tested so far, each with unique features
- DC-DC powering selected as a LV power, serial power backup option

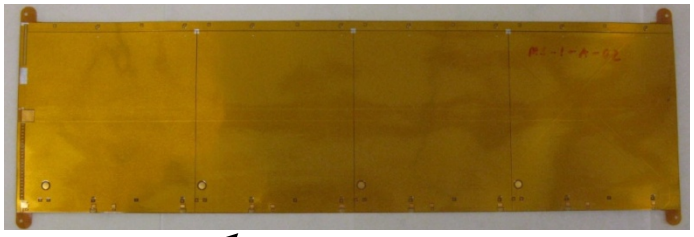


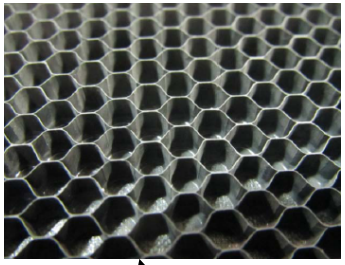

Berkeley stavelet (DC-DC power side)

Support structures for strip modules

- Support structures (cores): low mass, embedded cooling pipes, optimized for thermal performance, resistance to deformations, flat structure
  - Carbon composites: very flexible class of materials, reasonable Xo, good thermal properties, variable CTE
- Bus tapes: Flexible circuits with power, data, and control traces along the staves and petals
  - Kapton-Cu-Kapton-Cu-Kapton (+adhesives) layers, 150 µm thick total
  - Co-cured with carbon fiber facings

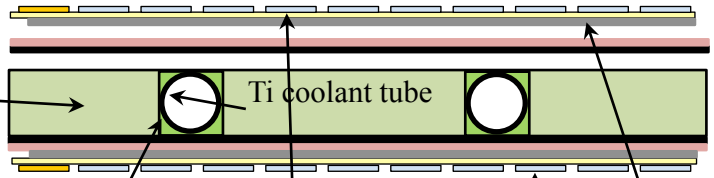






Carbon honeycomb

Stave cross-section

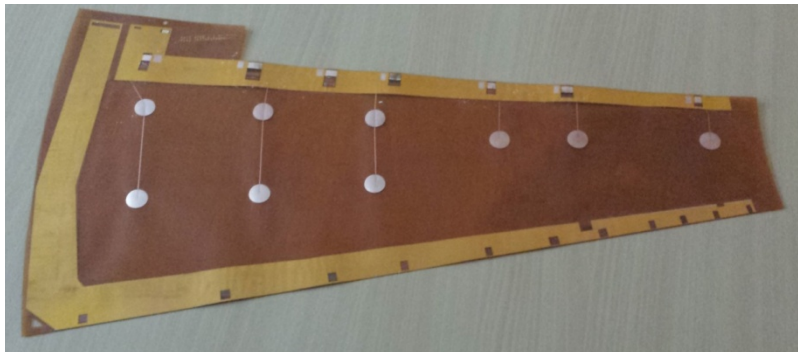


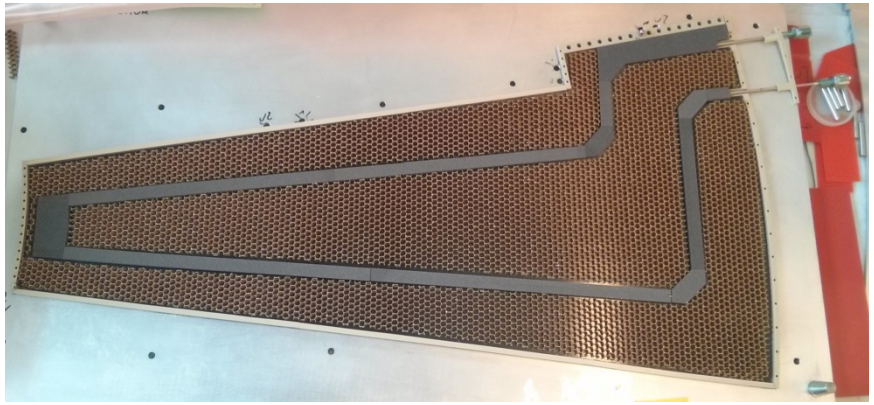
Cu bus tape (co-cured with facings)

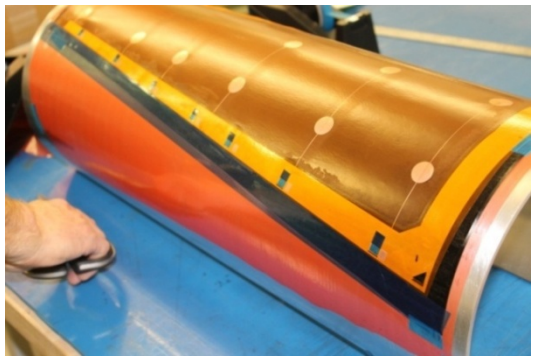
Carbon fiber facing (3 lay-ups) 0-90-0

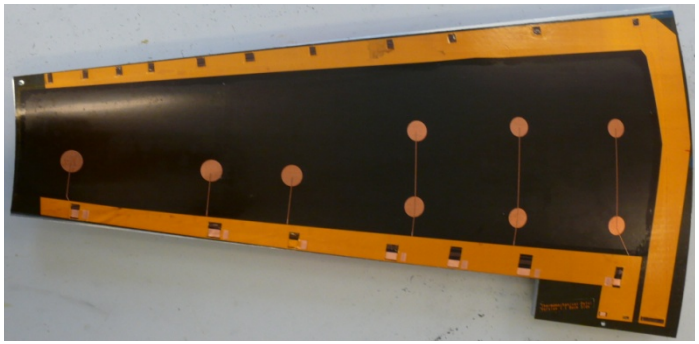
Support structures for strip modules

- Support structures (cores): low mass, embedded cooling pipes, optimized for thermal performance, resistance to deformations, flat structure
  - Carbon composites: very flexible class of materials, reasonable Xo, good thermal properties, variable CTE
- Bus tapes: Flexible circuits with power, data, and control traces along the staves and petals
  - Kapton-Cu-Kapton-Cu-Kapton (+adhesives) layers, 150 µm thick total
  - Co-cured with carbon fiber facings



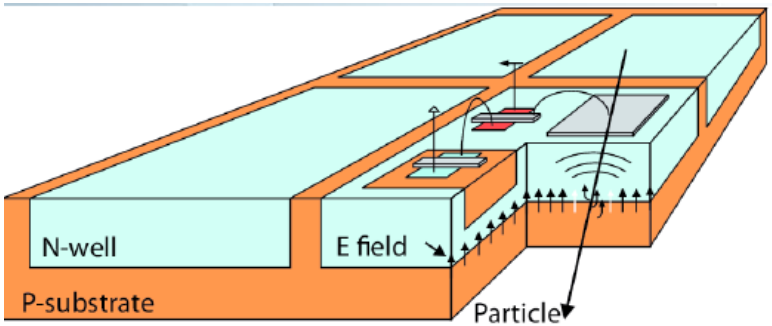




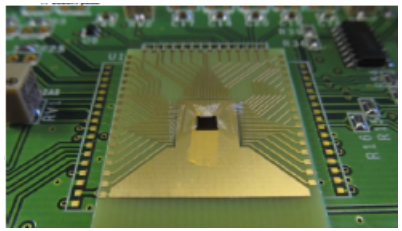


HV/HR CMOS alternative

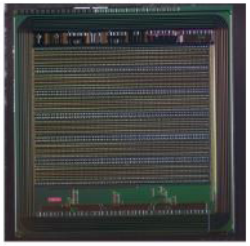
- HV/HR CMOS technologies are an attractive alternative to classical Si pixel and strips particle detectors
  - System-on-a-chip: integrated FEE (or sections of it)
  - Very few interconnections
  - Lower material
  - Potentially big cost savings
  - Less cooling, lower operating voltages
  - Radiation tolerance may be an issue, among others (schedule, re-design tasks,...)
- Pixel and strips are investigating the feasibility of their use on the Phase-II upgrade
  - In principle, easier to implement on the pixel region
    - Outer 5th layer?
  - Extensive design and radiation hardness programs ongoing
    - Several prototypes already in hand
    - Dedicated AUW sessions, a lot of information there

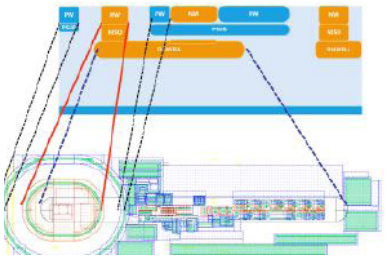


HV CMOS device


HVStripV1 prototype for strip detector

LF 150nm prototype for pixel detector

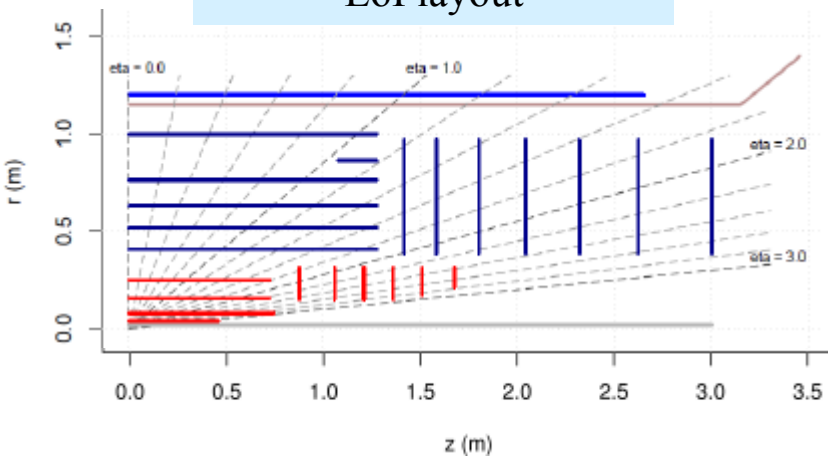




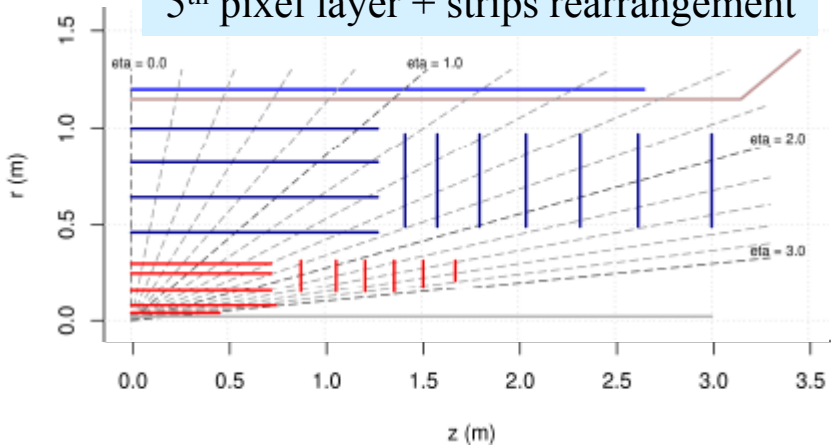
ITk layout task force: 5th pixel layer

- The ITk collaboration established as a top priority for 2015 to come with a final layout for the ITk
  - One of the biggest changes in LoI under discussion is the increase of pixel volume to allow a 5th pixel layer
  - Increase to ~25m^2 of pixels (LoI layout 8 m^2)
  - The savings in the strip detector may make up for the extra cost in the pixels
  - Strip layout options are obviously strongly coupled to the pixel layout and requirement task force outputs
    - Increase of pixel radius: removal of stub + 1 strip barrel layer, reduction of EC petal strips size

LoI layout

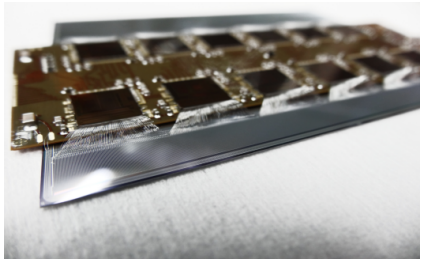


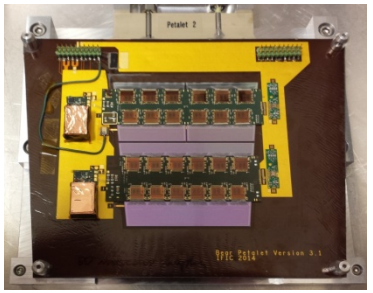
5th pixel layer + strips rearrangement

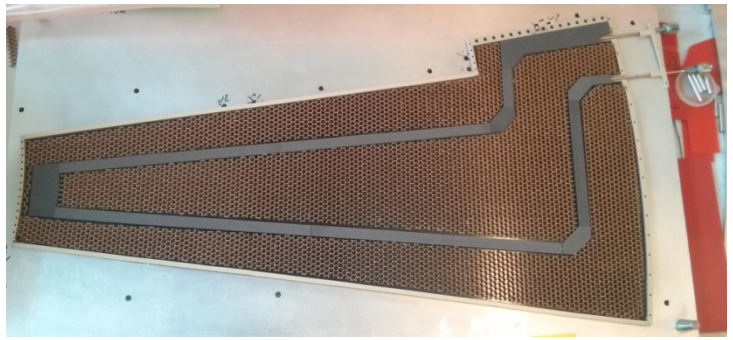


DESY strips activities in the phase-II upgrade

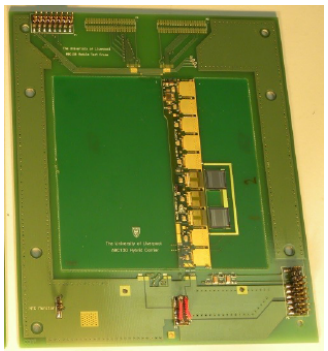
- Endcap module assembly and testing
- Module mounting on petalets and petals
- Petalet and petal core manufacture
- Electrical design of stave/petal GBT PCBs
- Electrical testing of petalets/petals
- CAD layout of strip petals
- ITk layout task force
- Leadership role in recent and future strips test beams
- CMOS activities for strips
- Overall project planning
  - Strips project leader and 2 activity coordinators

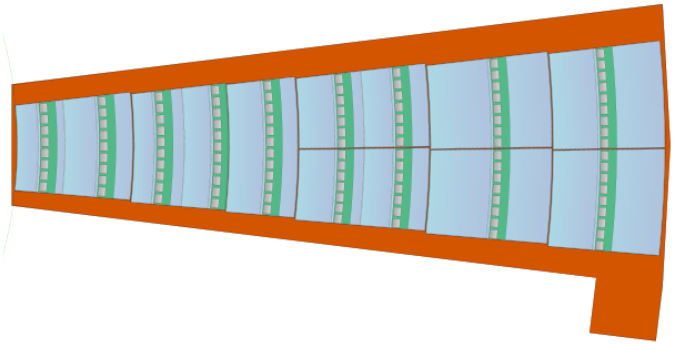






- Ultimately, one of the strip endcaps will be assembled at DESY
  - Petal core manufacture
  - Module assembly and test
  - Module mounting and test
  - Petal assembly and test
  - QA and QC





Outlook

- Despite being still far in time, ATLAS (phase-II) upgrade is a vibrant community covering a very wide range of activities

- ITk is the most expensive element of the ATLAS upgrade
  - Heavy involvement of DESY ATLAS group, in particular in the strips endcaps
    - The goal is to produce a full endcap here!
  - ITk layout is rapidly evolving, planning to converge on a final layout by the end of 2015
    - Re-assessment of proposed technologies once this decision is taken
  - Not so much time!
    - Strips TDR: end 2016
    - Pixel TDR: end 2017

Backup

Backup slides:

- Phase-I NMW project
- Phase-I FTK
- ITk radiation fluences
- Alpine layout
- SLIM layout
- High η coverage for ATLAS and “rings” layout
- Pixel sensor technologies
- CMOS for strips and pixels
- DESY ATLAS group
- CERN’s particle accelerator chain

NSW for Phase-I

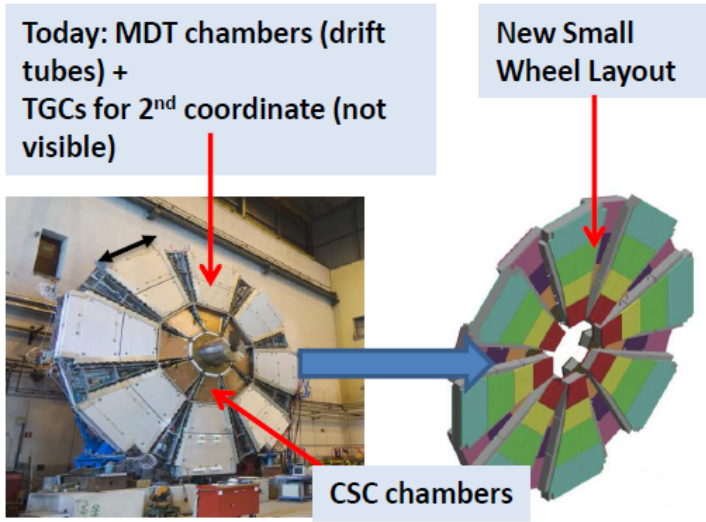
Introduction

Why?

To replace the present Innermost station of the Muon Endcaps in LS2 (2018/19)
The NSW addresses

- *high fake L1 trigger rate for high-pt muons*
- *loss in tracking efficiency*

at luminosity beyond 10^{34} s^{-1} cm^{-2} with the present Small Wheels.



New Small Wheels will be equipped with sTGC and MicroMegas (MM) detectors:

sTGC primary trigger detector

Bunch ID with good timing resolution
– additional suppression of fakes

Based on proven TGC technology;
Pads & strips, instead of only strips as in current detector

Good space resolution providing track vectors with < 1 mrad angular resolution , redundant tracking

MM primary precision tracker

Space resolution < 100 µm independent of track incidence angle

Good track separation due to small 0.5 mm readout granularity (strips)

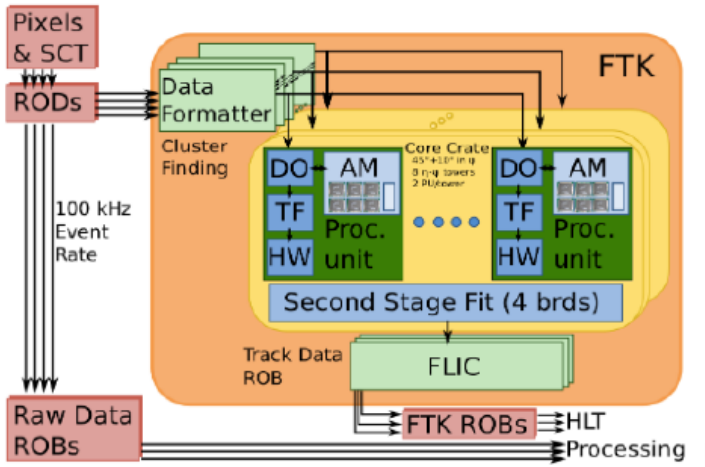
MM 2nd coord will be achieved by using ± 1.5° stereo strips in half of the planes

Provide independent track vector – redundant triggering

M. Bianco, Apr 2015 AUW

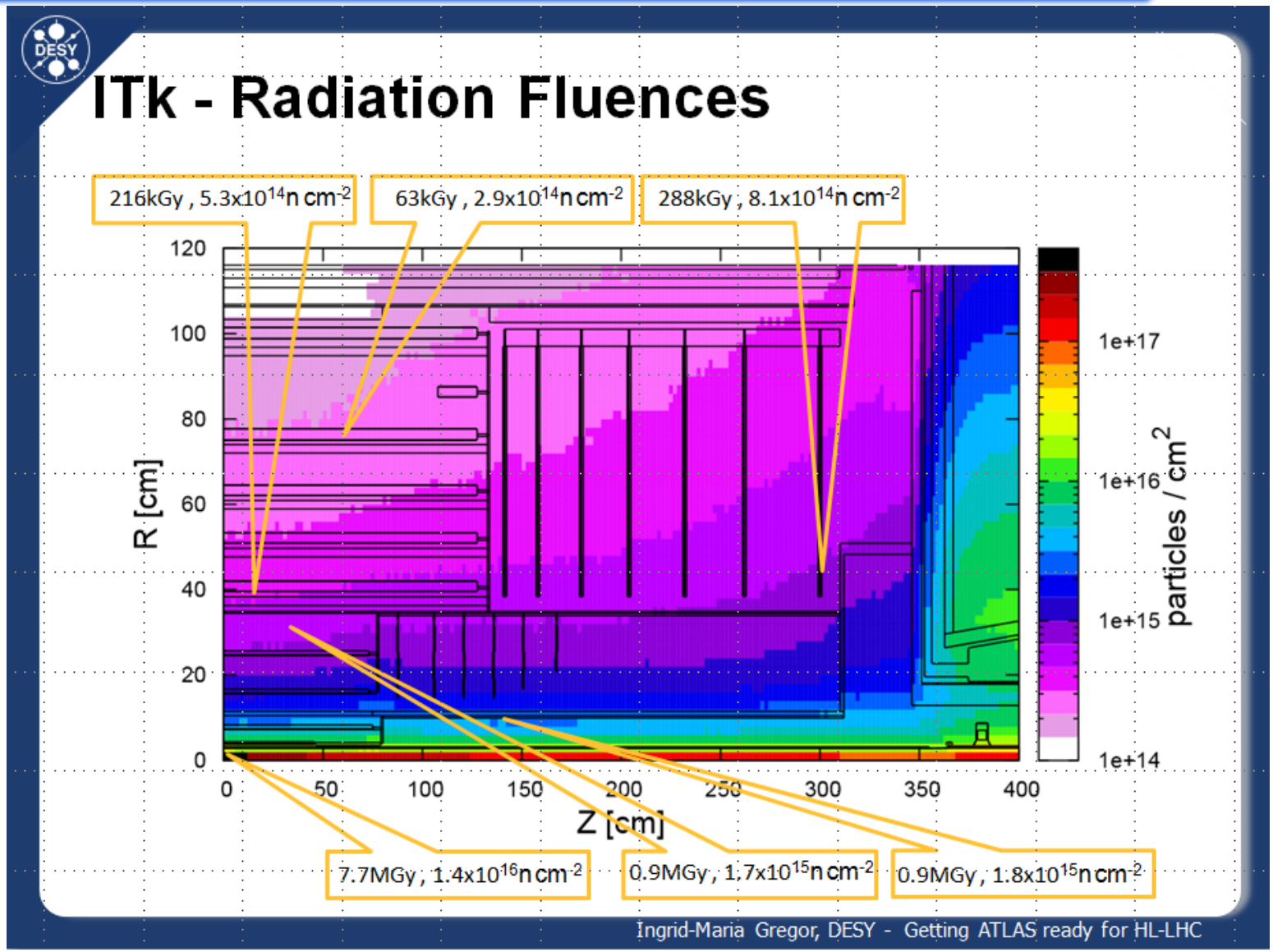
FTK phase-I

- New element of the trigger system, will be commissioned in 2016
- Reconstruct charged particles trajectories in the silicon detectors (Pixel & SCT) for $p_T > 1GeV$ and $\eta < 2.5$
- Process all level-1 (L1) accepted events (in ~100 μs)
- Outputs tracks for use in high level trigger



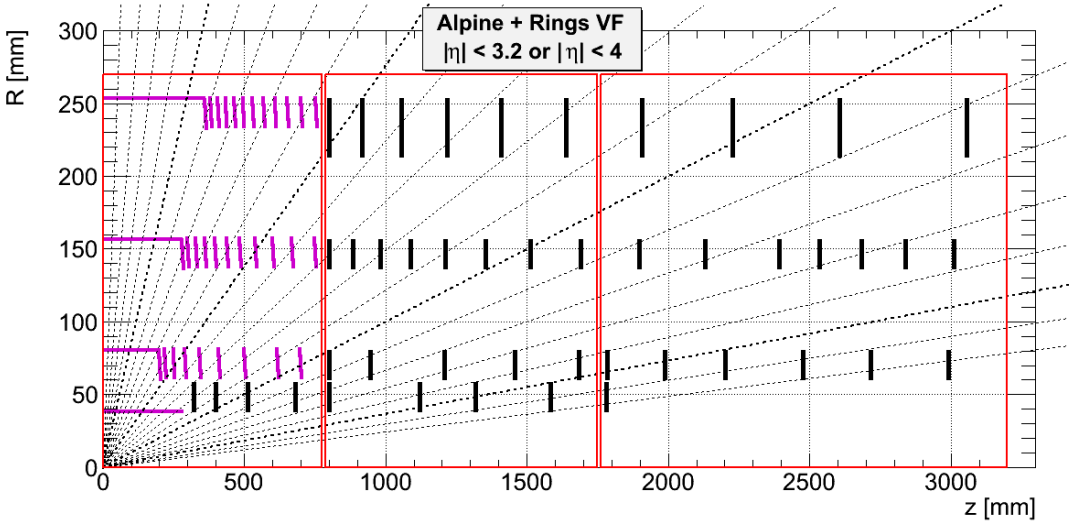
- DESY contributions:
  - extensive work on the Event Data Model, crucial for trigger algorithms to begin studying the improvements when using FTK tracks
  - generate pattern bank for use in associated memory (AM)
  - tests of the Second Stage Board
  - help in general commissioning at CERN

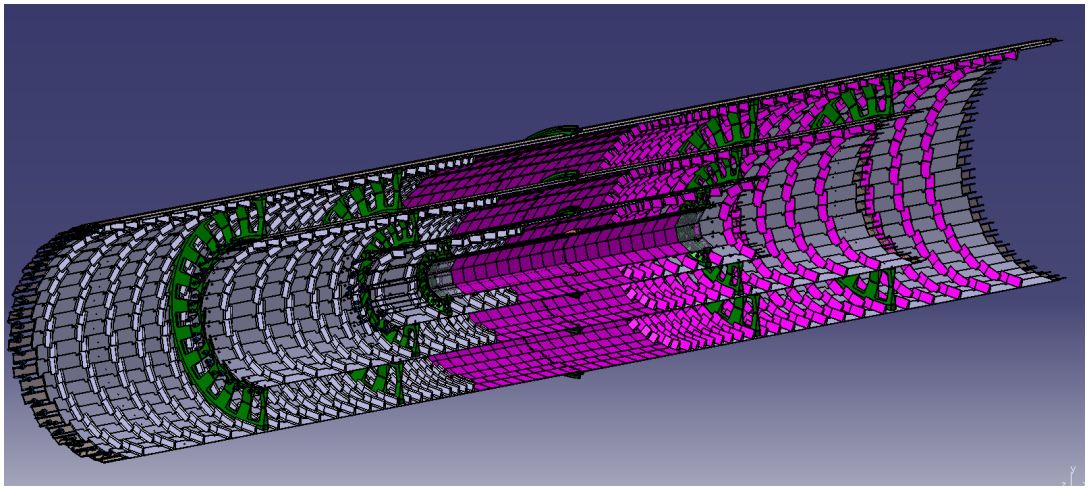
ITk radiation environment (LoI layout)



ITk pixel layouts: Alpine layout

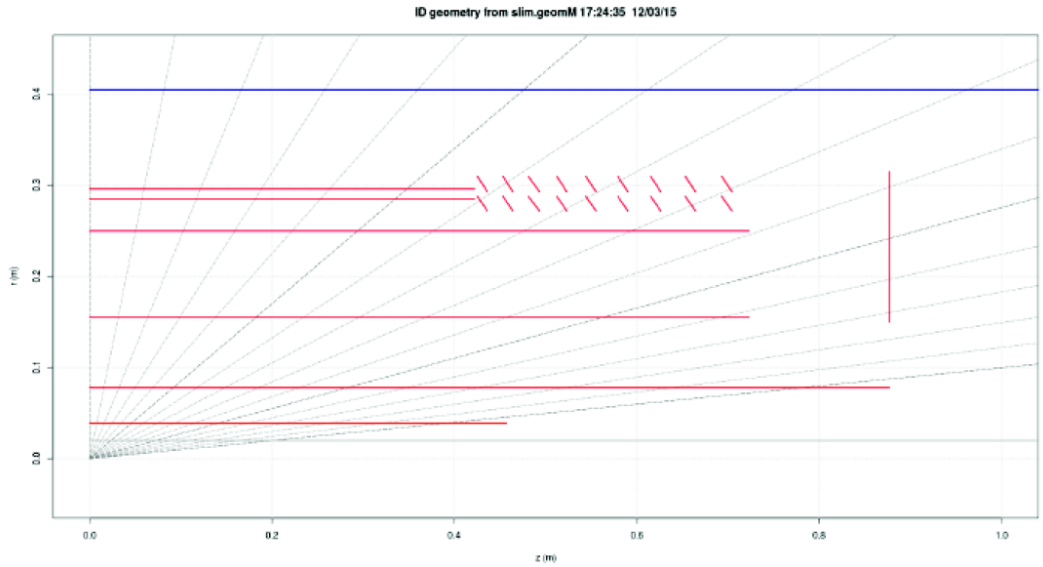
- Alpine + rings:

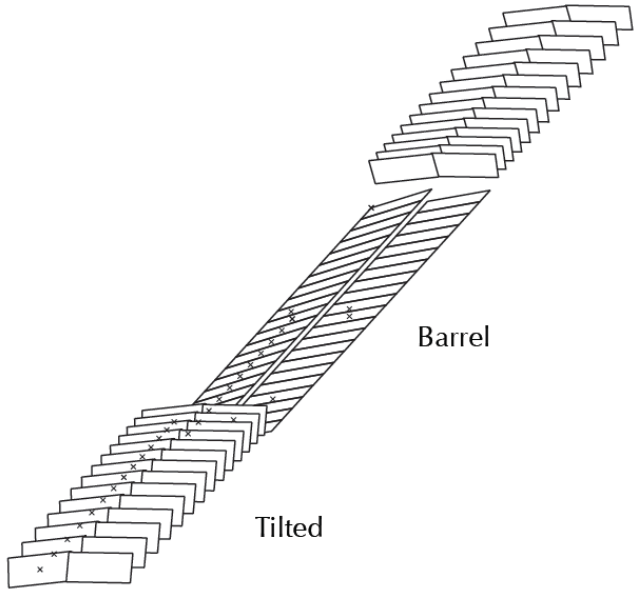


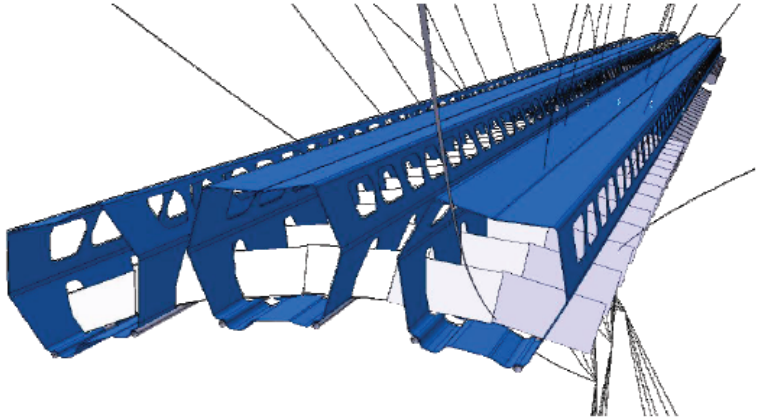


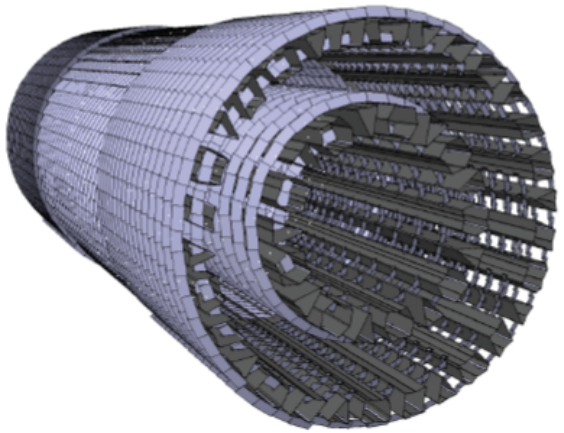
ITk pixel layouts: SLIM layout

- Stiff Longeron for ITk Modules (SLIM)









Initially developed for 5th Pixel Barrel layer (CMOS)

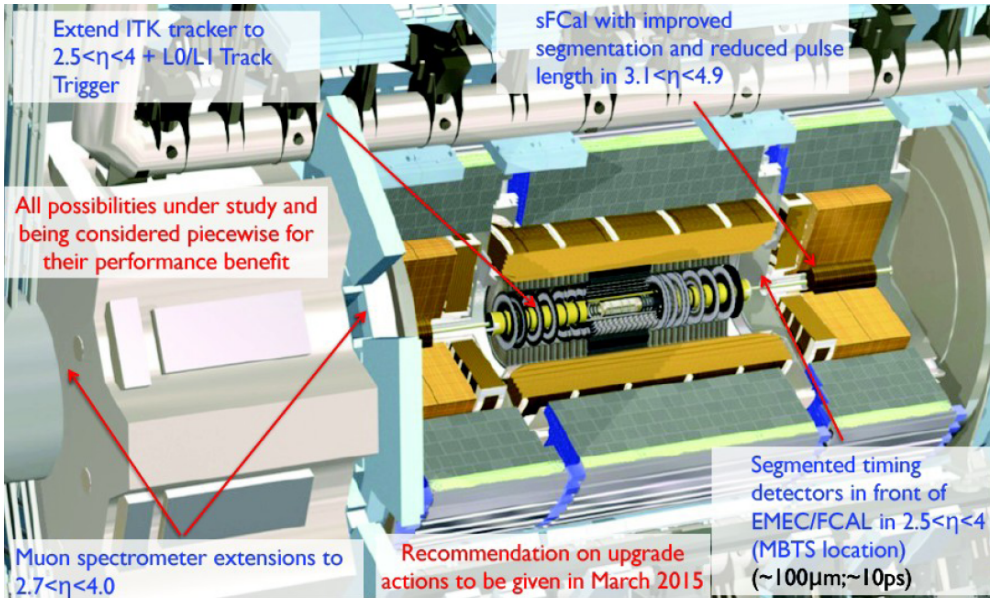
Evolved to be compatible with other sensor technologies

High η coverage for ATLAS

Potential benefits from an extension to large η:

- VBF Higgs production
- Vector Boson Scattering
- Double Higgs production
- Top background rejection (in ttH, H →WW)
- At object level: MET reconstruction
- Pile up jets rejection

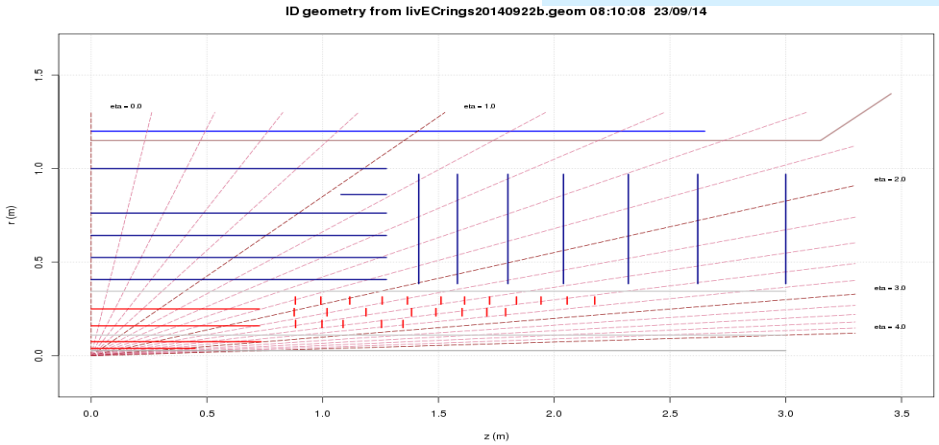
Possible scenarios considered by high-η task force

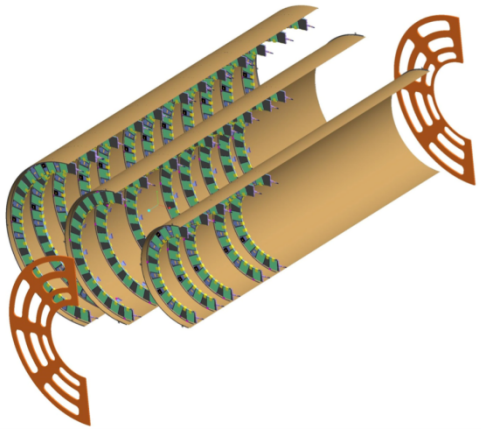


ITk pixel layouts: EC pixel "rings" layout

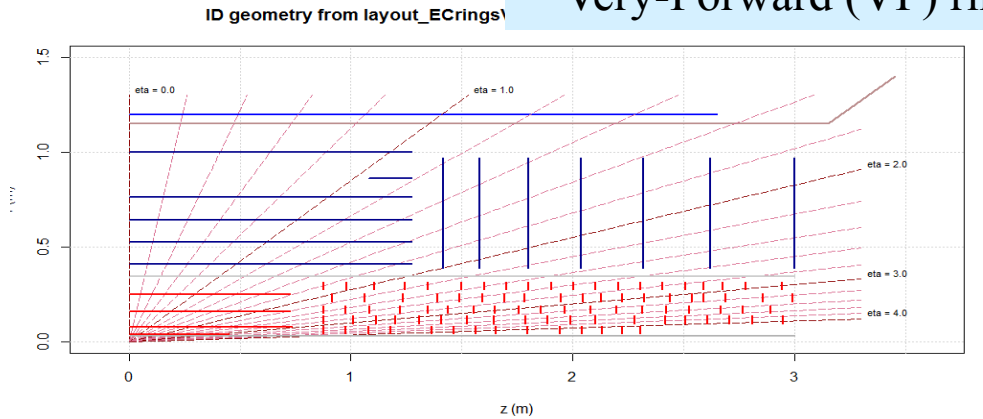
- Higher η coverage possible to be implemented in most layouts by adopting the "rings" pixel layout for the EC: single rows of quad modules placed on rings at different radii

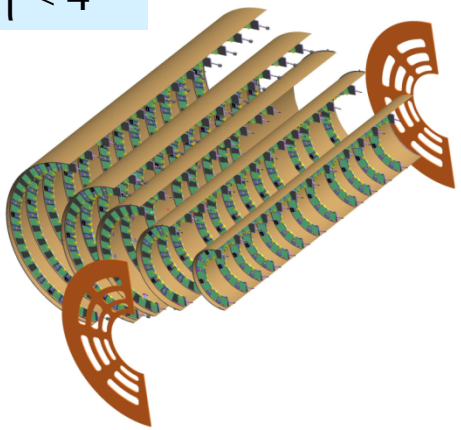
Baseline "rings" layout: η < 2.7





Very-Forward (VF) rings layout: η < 4



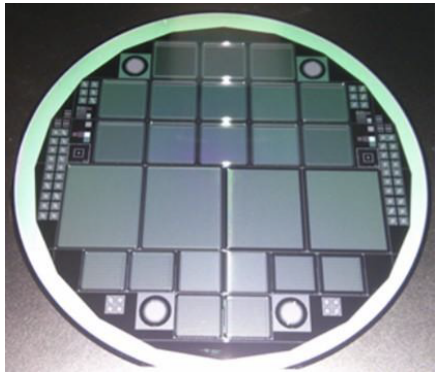


Pixel sensor technologies

- Several candidate technologies for pixel detector
  - Oxygenated n-on-n, 3D, diamond, HV/HR CMOS for outer pixel layers

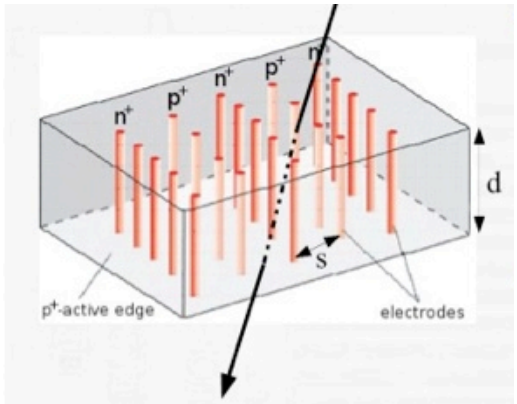
Planar pixel sensors (PPS)

"Classic" sensor design
Oxygenated n-in-n
200μm thick
Minimize inactive edge by shifting guard-ring underneath pixels (215 μm)
Radiation hardness proven up to 2.4×10^{16} p/cm^2
HV might need to exceed 1000V



3D silicon

Both electrode types are processed inside the detector bulk
Max. drift and depletion distance set by electrode spacing
Reduced collection time and depletion voltage
Low charge sharing

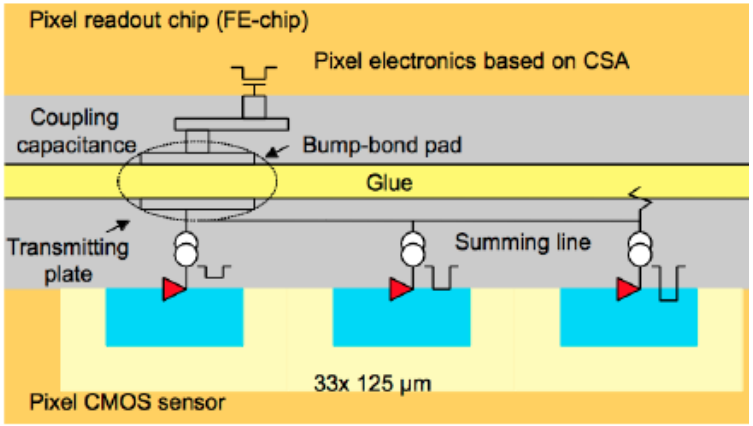


Diamond sensors

Good radiation tolerance
Low capacitance (noise) no cooling
BUT expensive
Used in ATLAS beam monitoring, current and replacement in 2014

CMOS pixels

Why CMOS pixels ?



Commercial process in large 8 or 12 inch wafers

Potentially much cheaper than customer HEP sensors

Potentially much cheaper bonding processes available (capacitive coupling gluing, oxide/Cu-Cu bonding)

Smaller pitch due to separation between CMOS sensor/analog tier and digital tier: sub-pixels in CMOS tier

Thin sensor (15-100 um) reduce clusters at large eta: improve cluster size, two track resolution, sensor radiation hardness

For initial prototypes FE-I4 digital tier is available, for final FE-RD53 will be suitable

Low occupancy layers (outer pixel layers, even strips) can be made in one tier with classical column or periphery readout architecture reducing the cost for large areas.

A.Rozanov AUW week 22.04.2015

CMOS Demonstrator Working Group

- RD started by Heidelberg-Berkley-Bonn-CERN-Geneva-Marseille since 2012
- From June 2014 in the framework of ITK Pixel Module under chair of Norbert Wermes (Bonn) with many institutes: Karlsruhe-Berkley-Bonn-CERN-Geneva-Marseille-Gottingen-Prague-IRFU-Glasgow-Oxford-Liverpool-INFN-Genova-Milan-SLAC-UCSC-…….
- Address the development of Demonstrator Pixel module at end of 2015
- Goal of preparing CMOS pixel option in the ITK Pixel TDR in 2017
- Two main technology are explored for creating depletion region: HV (10-20 ohm cm substrate and 30-90 v applied) or HR (0.1-3.0 Kohm cm substrate) or both

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CMOS strips

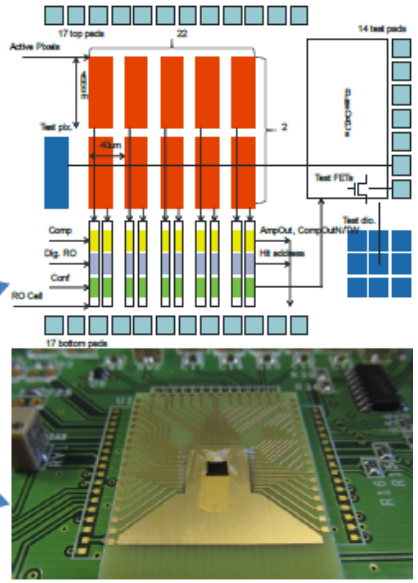
First Year Efforts

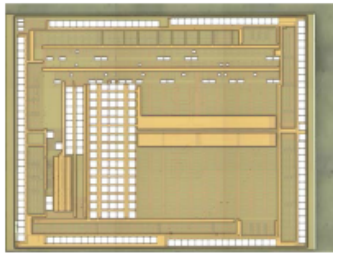
The goal of 1st year work is to understand the properties of signal (radiation tolerance, timing resolution, power, noise), pixel layout, and on-sensor readout architecture.

Had 3 chip submissions to figure out basic sensor properties:

- HVStripV1 by Ivan Peric (Karlsruhe/KIT)
  [AMS-350, Available since July 2014]
- CHESS-AMS by H. Grabas et al (UCSC), A. Dragone et al (SLAC)
  [AMS-350, Available since November 2014]
- CHESS-TJ by R. Turchetta et al (RAL)
  [TowerJazz-150, Available since April 2015]

Note: we are working on TowerJazz and AMS designs only.
Standard ρ ~20 Ω-cm (AMS, HV) and ~1000 Ω-cm (TJ,HR)





Transistors, amplifiers, passive pixel arrays, active pixel arrays

Vitaliy Fadeyev, Apr 2015 AUW

DESY ATLAS group

All ATLAS group activities

- **Detector activities**:
  - SCT operations
  - ALFA
  - IBL
  - FTK
  - test beam
  - Phase-2 upgrade: preparation for the strip endcap
- **Software and computing**:
  - Inner detector software
  - Tier 2, NAF, condition database
- **Object performances, physics analysis and modelling:**
  - electron/photon ID
  - jets and missing energy
  - Standard Model: Z, photon, WW and jets, minimum bias
  - Top: $t\bar{t}$+jets, top properties, $t\bar{t}$ resonances, single-top FCNC
  - Higgs: SM $H \rightarrow \gamma\gamma$ and $Z\gamma$, BSM Higgs
  - Generator and PDF: mass production and validation, generator tuning, derivation and impact studies of PDF
  - Exotics: search for prompt lepton jets

CERN's particle accelerator chain