

Lab session on pixel front-end characterization

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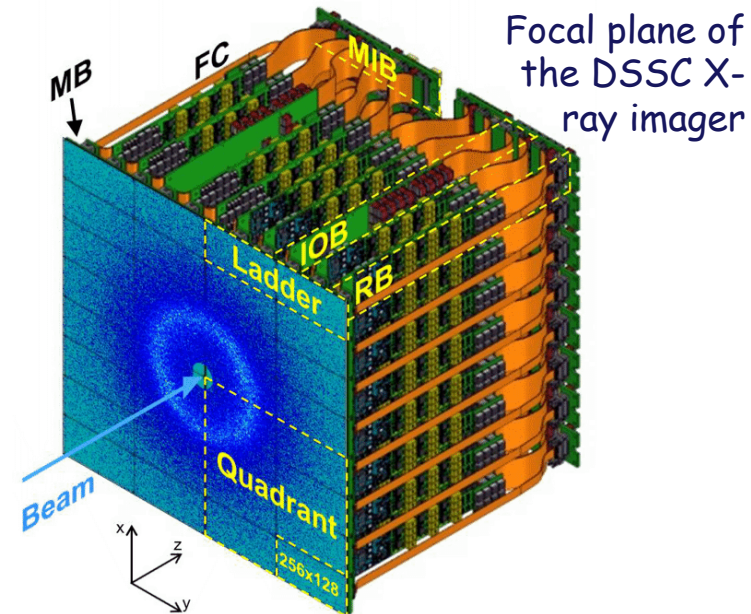
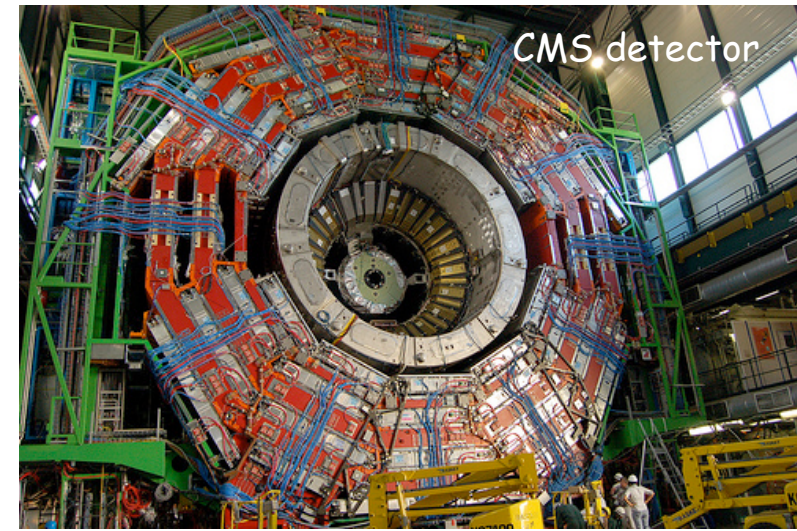
**Intelligent Front-End Signal Processing for
Frontier Exploitation in Research and Industry**

Hamburg, Germany, 14-25 September 2015



Focus of the lab

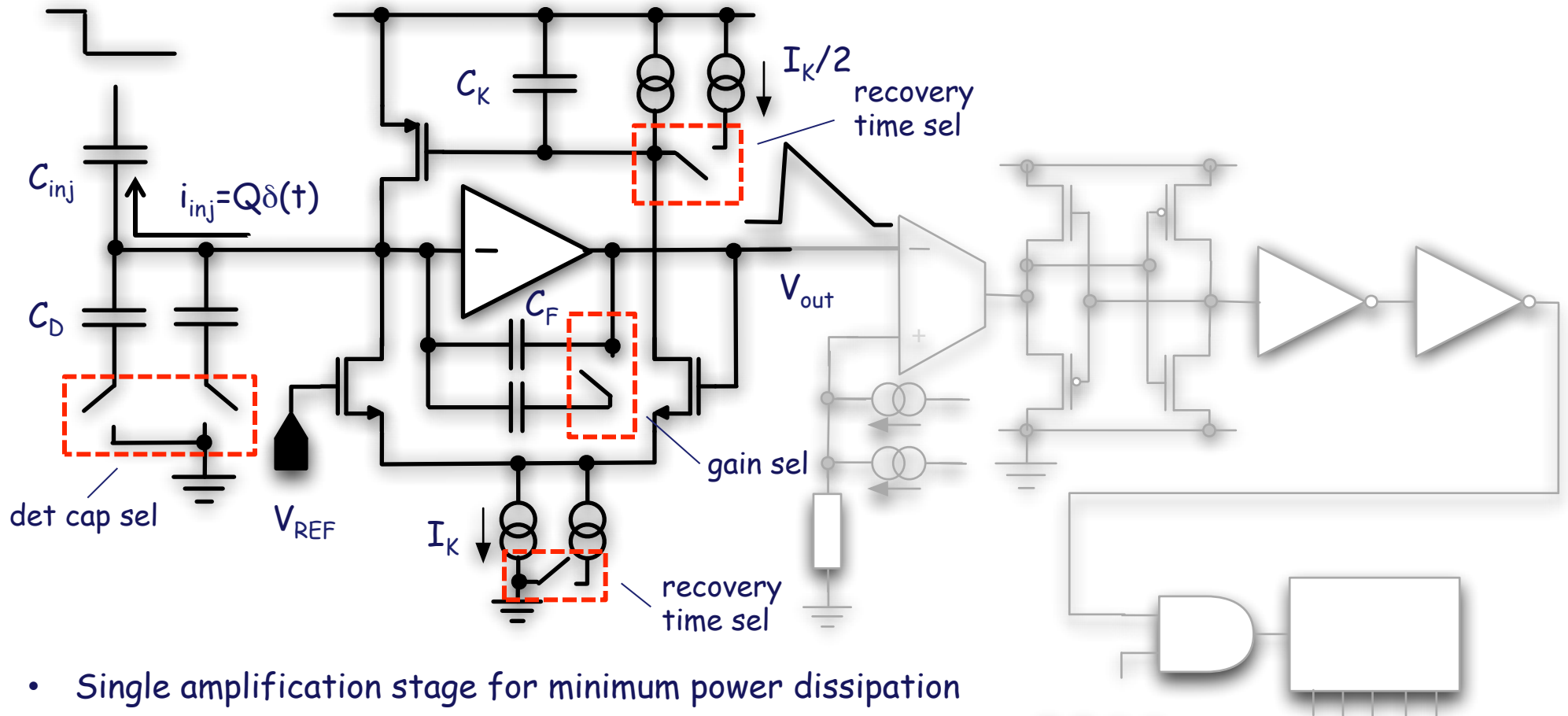
- Pixel front-end ASICs are located at the very beginning of the signal processing chain in pixel based detectors used in many fundamental and applied research fields
- Experimental characterization of front-end circuits in advanced microelectronic technologies is an integral part of the implementation of modern radiation detection systems
- The focus of the lab will be the characterization of a front-end channel for pixel detectors in a 65 nm CMOS technology
- The circuit under test, a prototype for the CMS phase 2 upgrade, was developed in the framework of the Italian CHIPIX65 and the international RD53 collaborations



Pixel front-end specs for HL-LHC

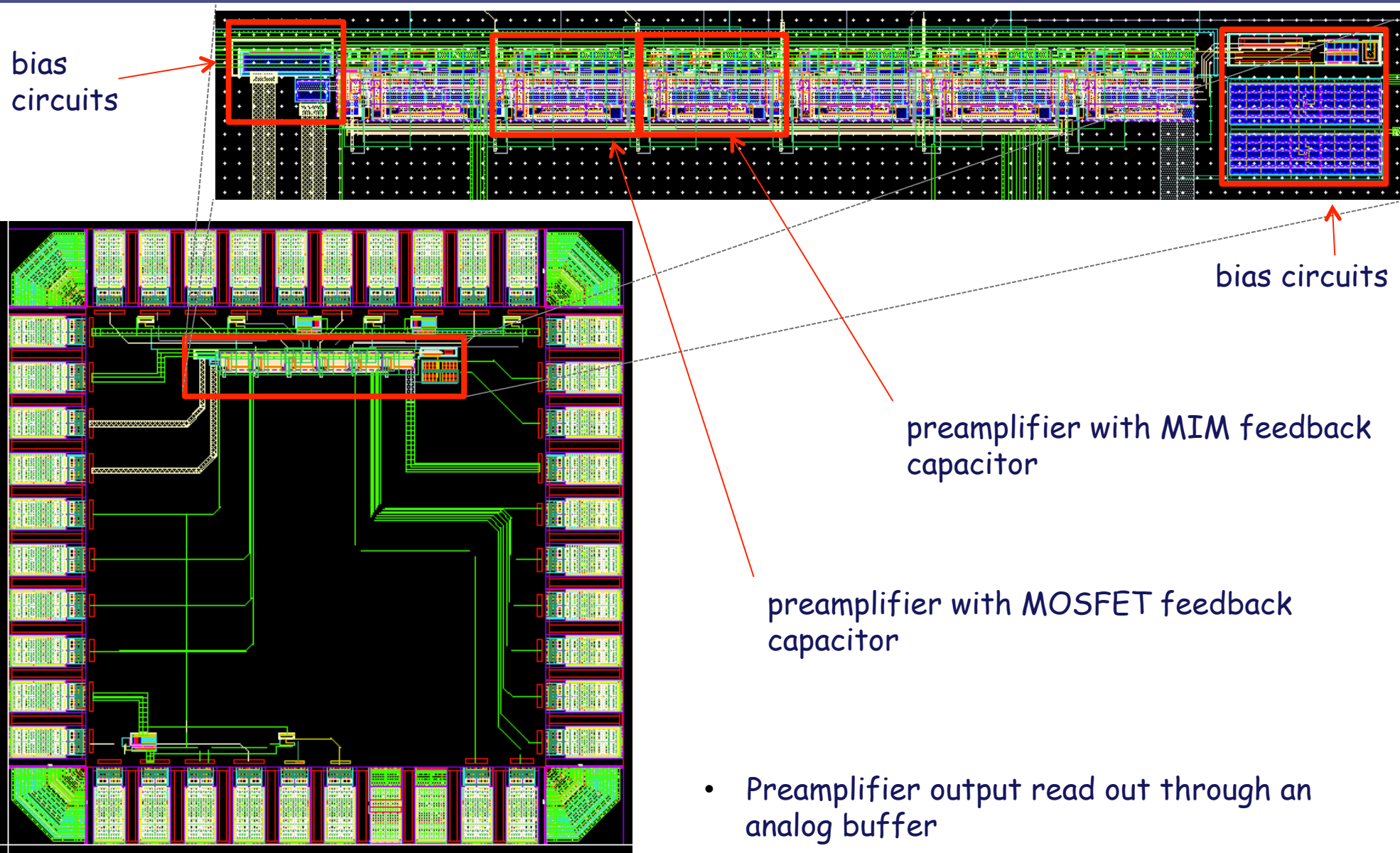
- In the phase 2 upgrade of the ATLAS and CMS experiments at the LHC, the inner layers of the pixel trackers will have to face some serious challenges
 - very high hit rates: $1 - 2 \text{ GHz/cm}^2 \rightarrow$ need of intelligent pixel level data processing
 - very high radiation levels: 1 Grad total ionizing dose, 10^{16} neutrons/cm² fluence
 - very high trigger rates: 1 MHz
 - small pixel cells: $50 \times 50 \text{ um}^2$ (or $25 \times 100 \text{ um}^2$) $\rightarrow$ improve resolution and reduce occupancy
 - small power dissipation: $\sim 10 \text{ uW}$ per cell (including analog and digital sections)
- Optimum front-end design requires a trade-off between noise, area, speed, power dissipation, amount of in-pixel functions
- The **65 nm CMOS process** in its low power (LP) flavor is optimized for a reduced leakage and a small power consumption (at the price of a lower speed)

Channel schematic



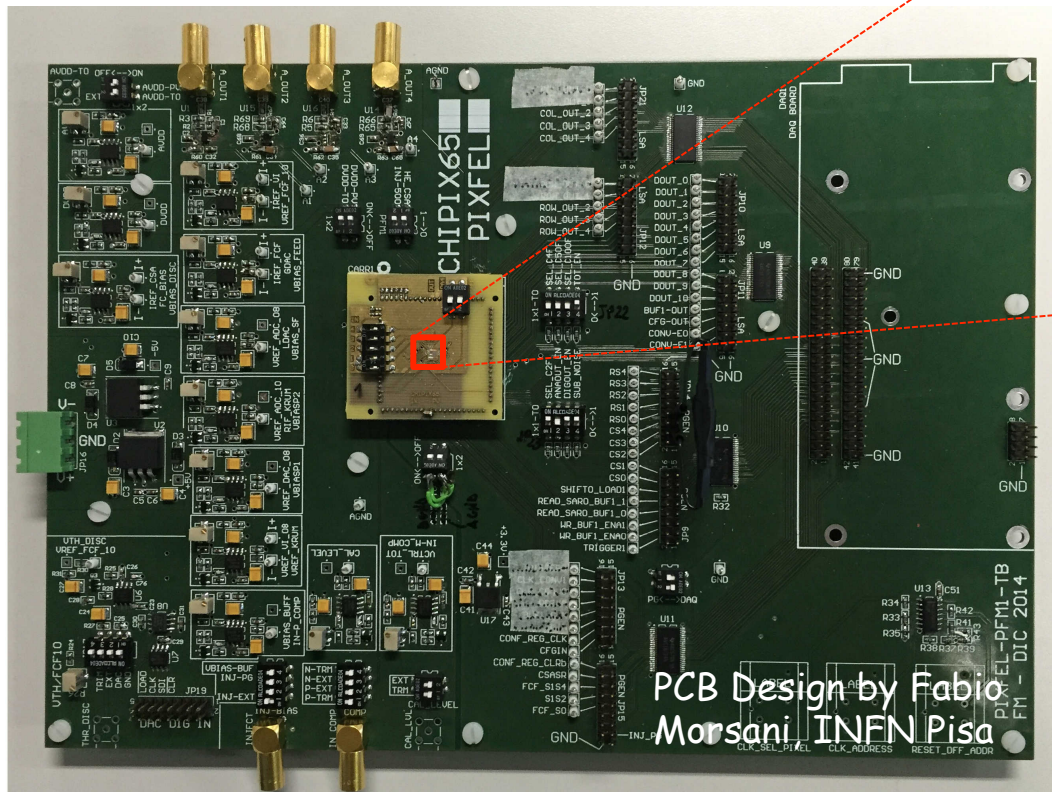
- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current
- 30000 electron maximum input charge, ~450 mV preampli output dynamic range
- Selectable gain and recovery current

Circuit layout

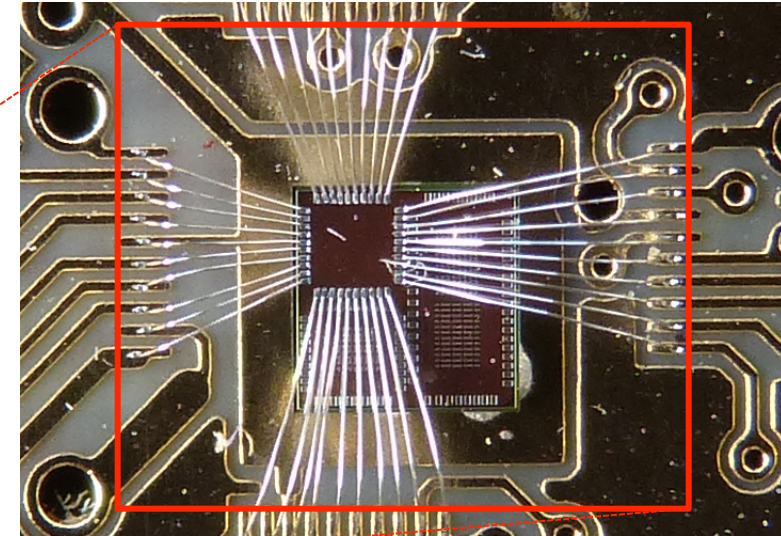


Test setup

- 2 mm x 2 mm chip including two different versions of a charge preamplifier with Krummenacher-style feedback network



PCB Design by Fabio Morsani INFN Pisa



- Chip on a small daughter board mounted on a test PCB, including dip switches for channel configuration: gain, time to baseline, input capacitance for detector emulation

Instrumentation and prerequisites

- Simple bench top instrumentation is required for measuring gain, ENC, response of the channel in presence of a leakage current: power supply, digital scope, arbitrary function generator
- No previous experience in pixel front-end characterization is required
- Basic knowledge on electronic circuit operation and standard electronic instrumentation is a prerequisite

