Lab 6 & 7

- FPGA configuration using HDL
- Interface to FPGA using Ethernet and Python

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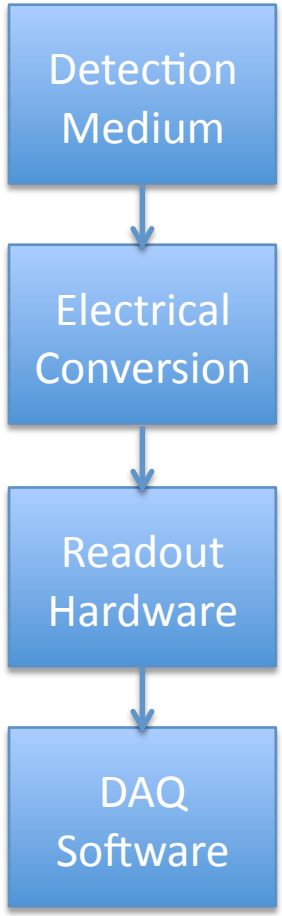
Overview

- Intended to be a **introduction** to:
  - configuring programmable logic (FPGA) using a HDL (VHDL)
  - Readout using a scripting language (Python).
- Uses cosmic ray muons and scintillation detectors to provide signals.
  - (Astro Particle Physics in miniature…)



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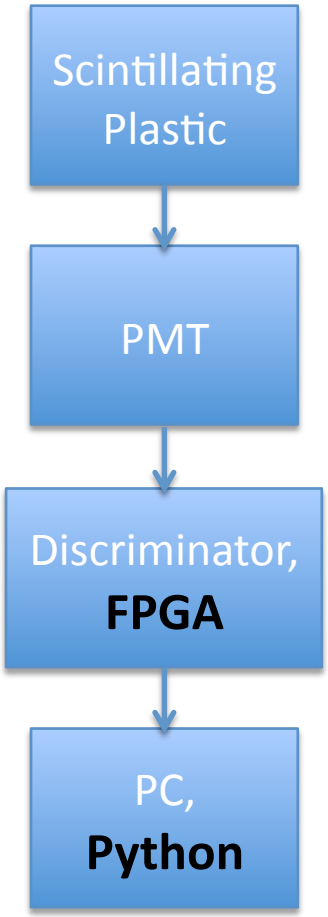

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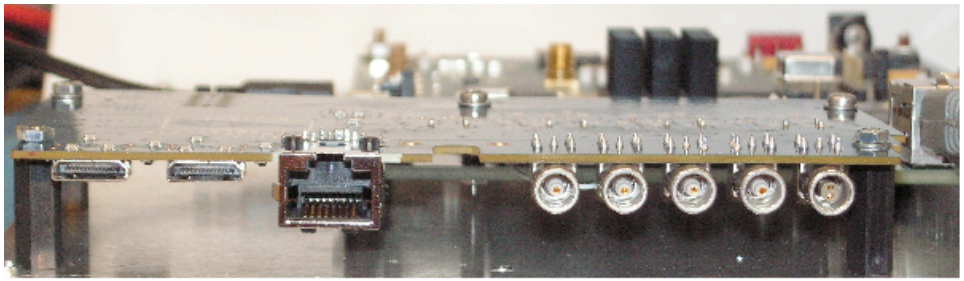
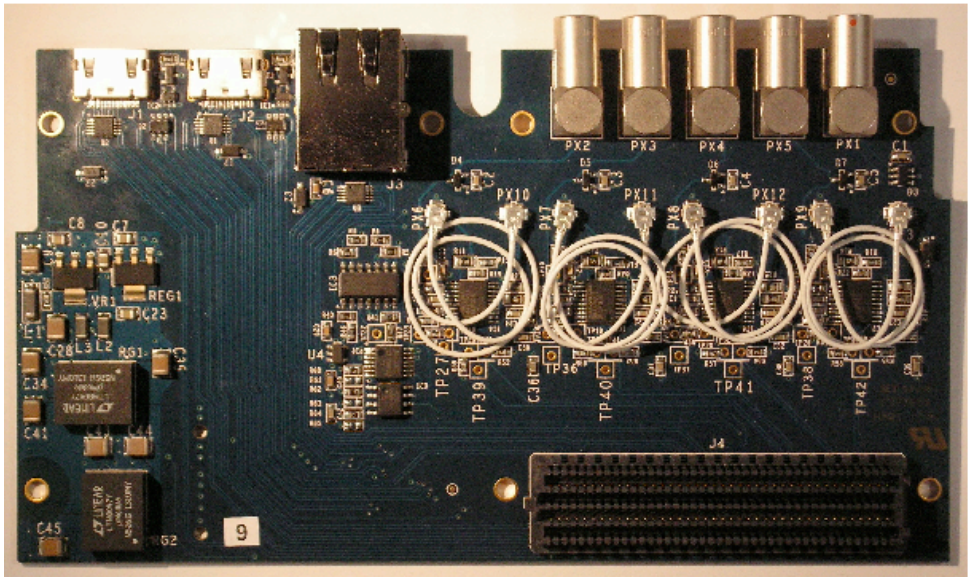
Hardware

- "Trigger Logic Unit" designed for beam test work
  - Part of EU funded AIDA-2020 programme
- "FPGA Mezzanine Card" format (VITA-57)
- Mounted on FPGA development board
  - Xilinx SP605 (Spartan-6 xc6s45)



DUT0 (HDMI) DUT1 (HDMI) DUT2 (RJ45) Trigger Inputs Clock I/O



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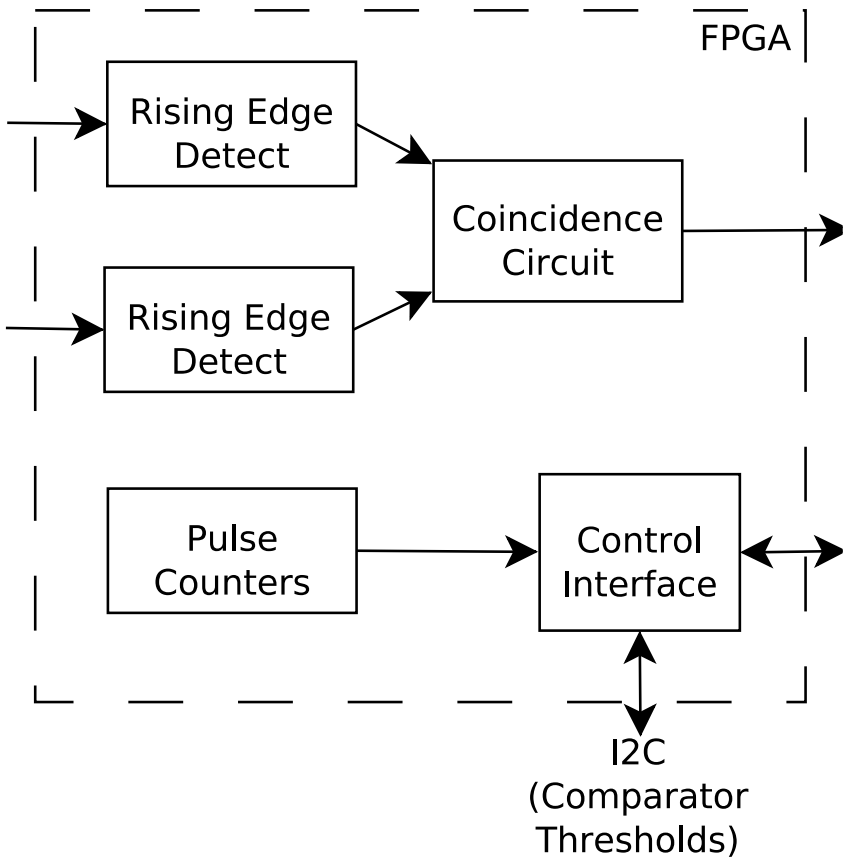
Firmware

- "Fill in the boxes" tutorial
  - Complete an existing design
- Communication with host PC using Gigabit Ethernet (IPBus fimware developed for CMS)



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Exercise

- Fill in the box (synthesis)
- Test in hardware
- Test in simulation
- Read out/control counters via Gigabit Ethernet

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Exercise

- More material than can be covered in 2-3 hours, so divided in two:
  - Lab 6 – hardware oriented
  - Lab 7 – software oriented
- Can do one or both labs.

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Acknowledgements

- Special thanks to:

Scintillation detectors and power supplies
(Ralf Diener , Hendrik Jansen)

Trigger Logic Unit hardware