Demonstrator Plans for FPGA-based L1 Track-finding with Hough Transform

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Track Trigger Concept

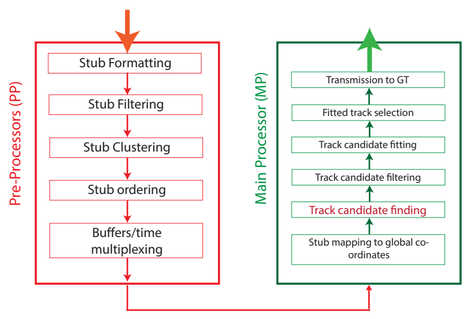
One of the major upgrades of the **Phase II CMS experiment** at CERN will be the Track Trigger. The UK groups proposed for it a **Time Multiplexed Trigger** architecture, based on **FPGA** electronics. In a TMT all data from one event are analysed by a single processor. To achieve this two processing layers are required (Pre-processors & Main-Processors). The PPs take data directly from the Front-end modules and buffer them into the MPs, where the Track Finding algorithm is implemented.

HT Basics

Straight lines considered in terms of slope-intercept parameter (m,c)

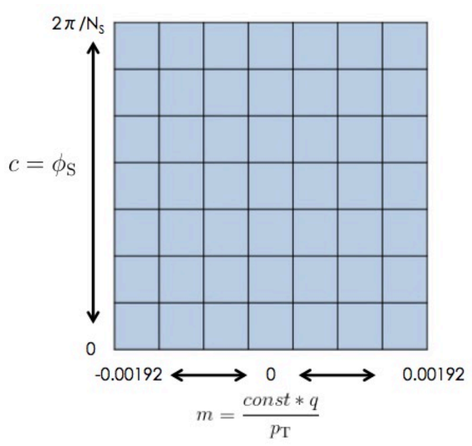
Point (x, y) —> Line (m,c)

Line (x, y) —> Point (m,c)



The L1 Track Finding algorithm is based on the **Hough Transform** method, which is applied to the *r,ϕ* coordinates, projecting them in the *m,c* plane.

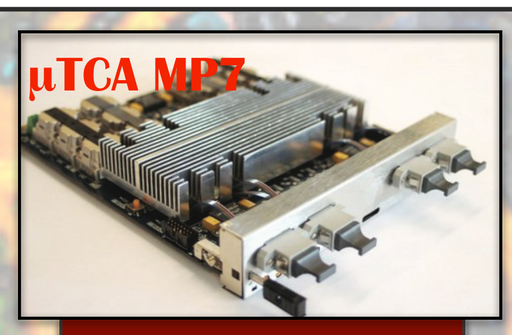
Here $c=\phi_S$ is the the predicted ϕ coordinate of the track at a chosen radial offset, with respect to the lower bound of the *ϕ* segment that the stub is allocated to; and *m* is proportional to the inverse of p_T. When a cell contains 5 or more stubs at unique radii, a track candidate is found (**r-filter**).



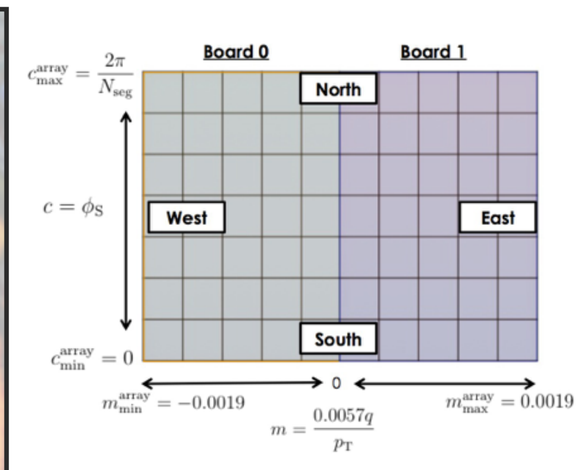
The First Demonstrator

The first demonstrator would simulate the behaviour of a Main Processor board. It will be formed by two **μTCA MP7 boards**, in which a *r-ϕ* Hough Transform array will be implemented. Future demonstrators will make use also of the *z*-coordinate information and include a track-fitting stage. The array will be **split** in the two boards **simmetrically** at *m*=0. Board 0 will reconstruct negative particles, whereas board 1 will operate with positives.

At first instance the PP tasks will be implemented in software.

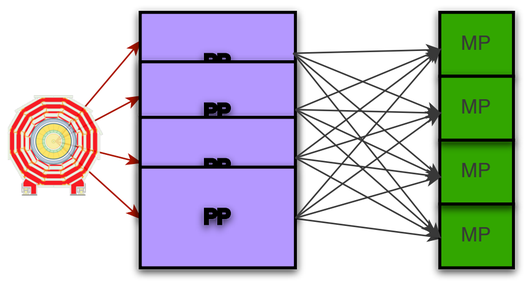


- FPGA Virtex 7
- 72 I/O Optical Links (12.5 Gbps)
- Tot. bandwitdth ~1 Tbps



The Pre-Processor

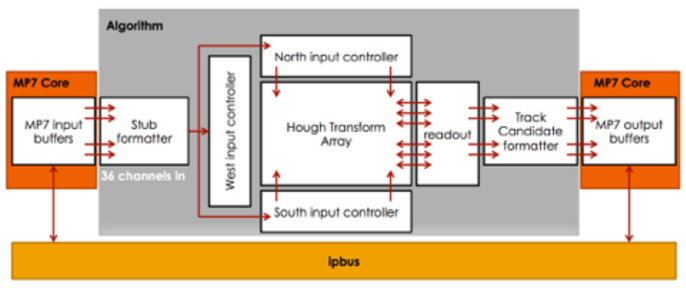
The Pre-Processor tasks will be reproduced by the **software**, which will send its output into MP7 input buffers via IPbus. The three main responsibilities of the PP are:



- Assignement of stubs to the correspondent *ϕ* segment
- Calculation of the bend resolution parameter *ρ*
- Place cut on stub p_T and *η* parameters

Additional tasks can also be implemented, like stub clustering and duplicate removal.

The Main-Processor

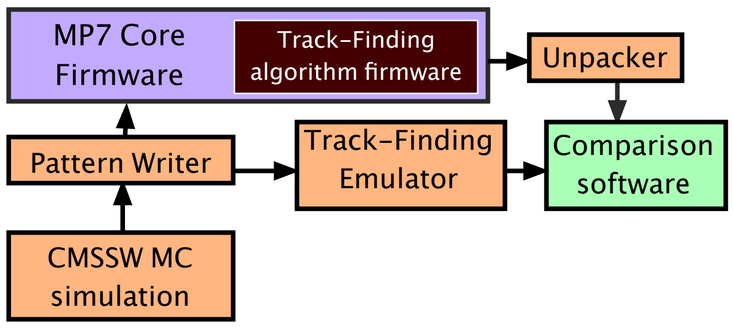


The MP firmware will be constituted by two main blocks, the **MP7 Core** and the **Algorithm**. The MP7 core provides the infrastructure for clocking, TTC signals and the handling of input/output data. The input to the board is over 72 optical links, each carrying a 32 bits word. Stub data will require 64 bits, thus each stub will be split across two input frames on the same link. The 72 input channels carry 36 stubs per tick, therefore the algorithm firmware will have 36 inputs. The algorithm represents the Hough Transform array.

Array Dataflow

- Stubs can enter in the array from West, North and South
- Input controllers determine if the stub should enter the array at the adjacent cell
- Inside the array dataflow allowed only along east, south-east and north-east directions
- Stubs stored in cell if they satisfy cell *m-c* conditions
- Cell marked for readout when it fulfils r-filter criteria
- BX end signaled using a fake stub

Software Framework



The demonstrator will require a software framework to interface with the firmware and to emulate the algorithm.

Pattern Writer	Emulator	Unpacker	Comparator
	• Based on the Calorimeter trigger upgrade emulator • Matches precisely the firmware • Used for data quality and dataflow studies, analysis and comparison with MC simulation	• Converts the output data of the MP7 firmware in EDM files for the compator. • Forms a single framework with the emulator	•Compares hardware and emulator results • Creates plots for debugging and analysis

Acknowledgment

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