3rd International Summer School on INtelligent Signal Processing for FrontlEr Research and Industry



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A Pattern Recognition Mezzanine Based on Associative Memory FPGA Technology for L1 Track Triggering at HL-LHC

Friday 25 September 2015 14:00 (5 minutes)

Presenter: FEDI, Giacomo (INFN-Pisa, Pisa, IT)

Session Classification: SPECIAL POSTER SESSION