



Contribution ID: 85

Type: **not specified**

A Pattern Recognition Mezzanine Based on Associative Memory FPGA Technology for L1 Track Triggering at HL-LHC

Friday 25 September 2015 14:00 (5 minutes)

Presenter: FEDI, Giacomo (INFN-Pisa, Pisa, IT)

Session Classification: SPECIAL POSTER SESSION