Vertical Integration in New Devices

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3rd International Summer School on
INtelligent Signal Processing for FrontIEr Research and Industry

PURDUE UNIVERSITY

Fermilab

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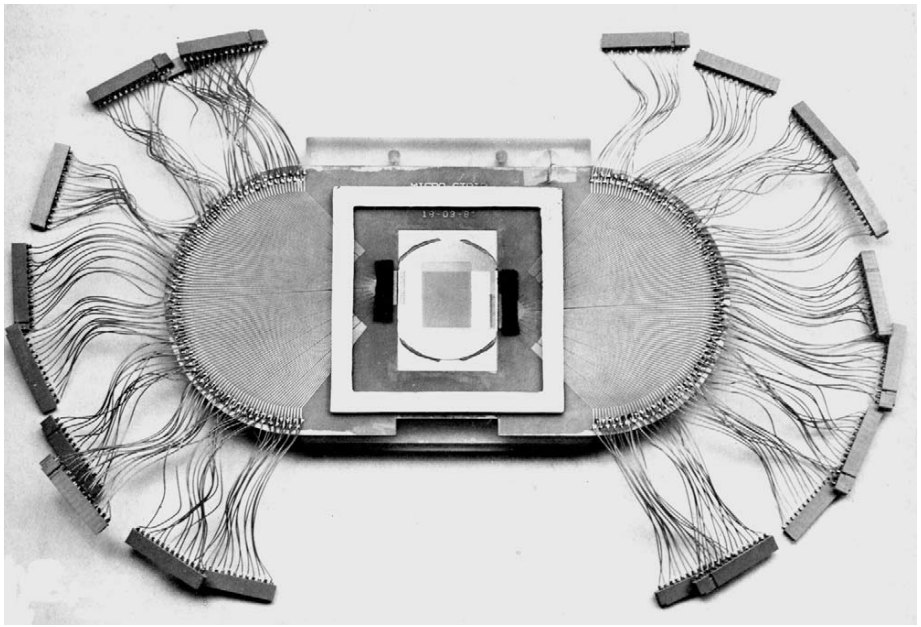
General Outline

- Motivation for Vertical Integration
- Enabling Technologies
- Bump Bonding in Pixel Sensors/Readout Chips
- Enabling Technologies for Direct Wafer Bonding
- Vertical Integration in New Pixel Sensors (VIPIC project)
- Vertical Integration in New Memory Applications (VIPRAM project)

Thanks to the experts: Alan Huffman (RTI), Nick Hinton (Purdue)

Early history: Silicon Strip Detectors



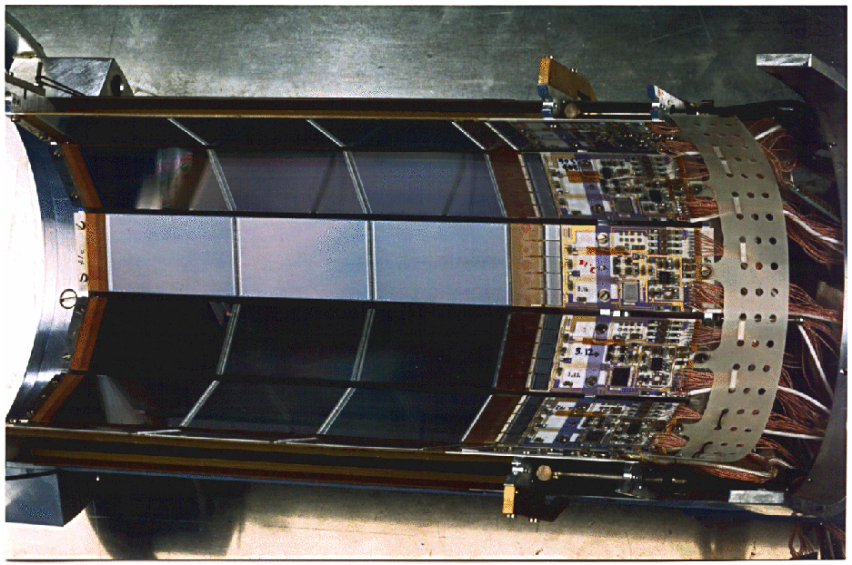
Silicon detector used in the NA11 experiment at CERN in the 1980's.

The challenge is to instrument a large number of channels while minimizing

- Mass (cables, interconnect, substrates)
- Power dissipation (requires active cooling)
- Needs to work at high rates (requires a trigger, or data buffering)

Nucl. Instrum. Meth. A324 (1993) 34-52.
Nucl. Instrum. Meth. A430 (1998) 326-350.

Readout Channel Density

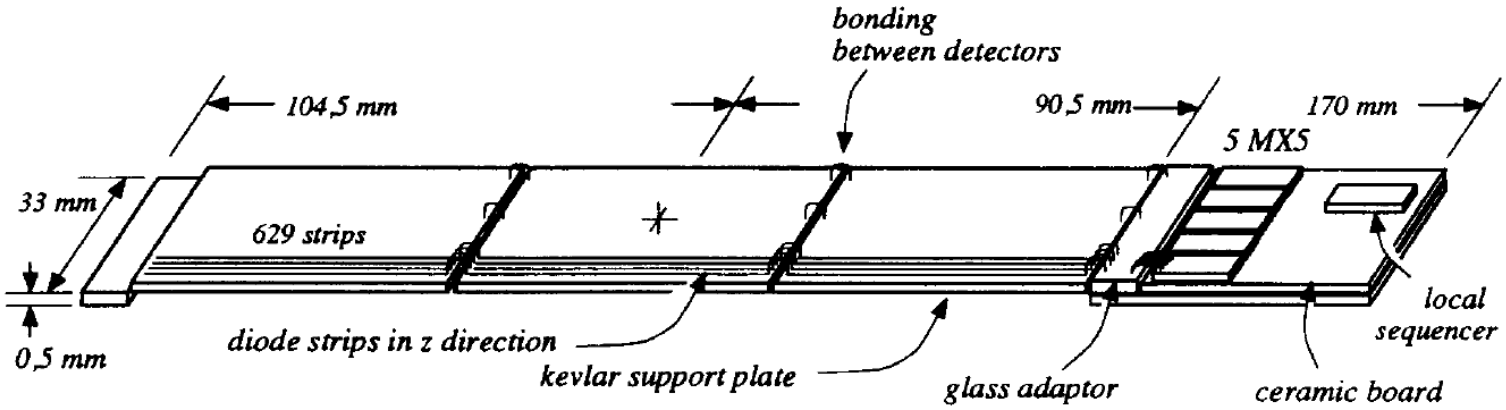


Early ASIC development:

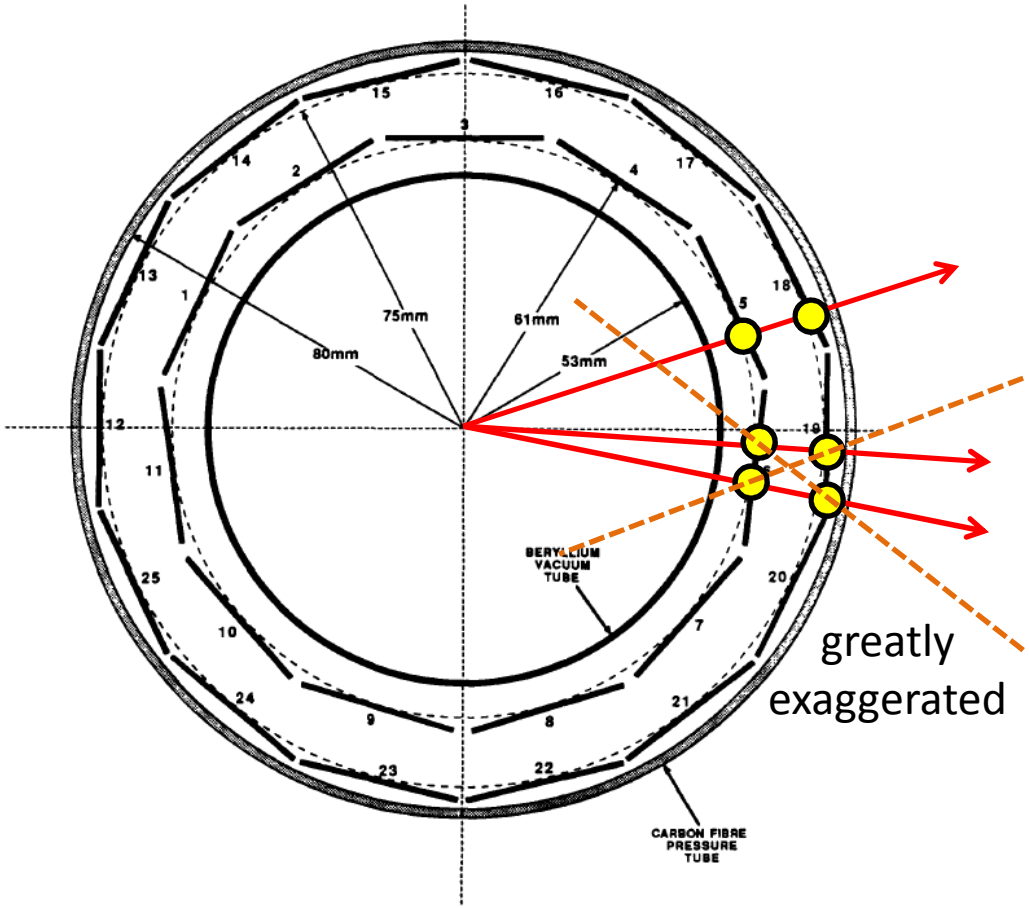
- CAMEX64 – 64 channel 3.5 µm CMOS
- MX7 – 128 channel 3 µm CMOS
- SVX – 128 channel MOSIS submission

Enabling technologies:

- Wire bonds
- Pitch adapters
- Low-mass hybrid circuits



Tracking Performance



OPAL silicon microvertex detector:
two layers of single-sided silicon strips with a 50 µm readout pitch.

Single-sided strips can work well when the occupancy is low:

- Test beams
- Outer tracker regions

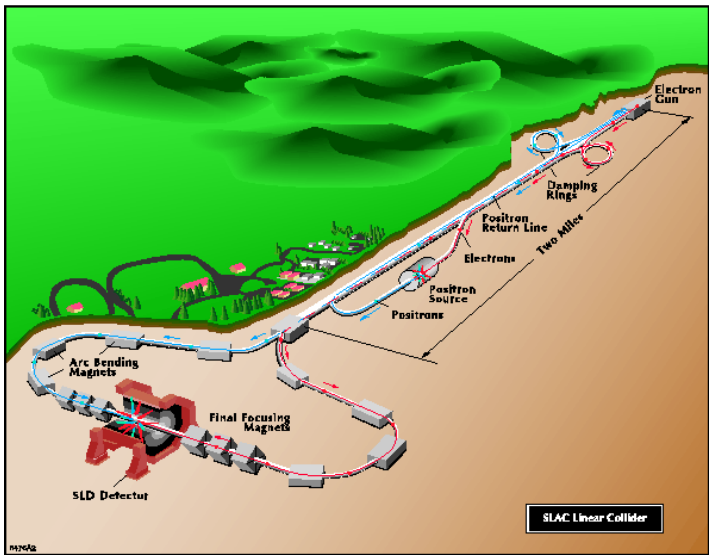
$$Z^0 \rightarrow \mu^+\mu^-$$
$$\sigma(d_0) = 15\ \mu m$$

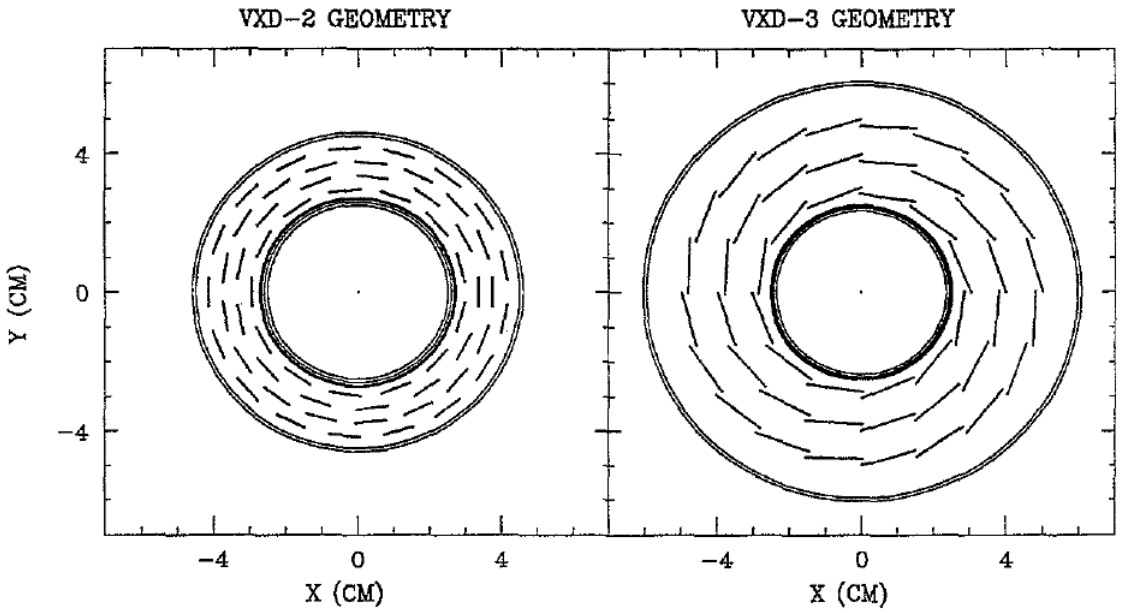
High hit occupancy leads to pattern recognition ambiguities and large fake rates.

Partially mitigated by

- Additional layers
- Orthogonal or small-angle stereo planes

CCD Sensors





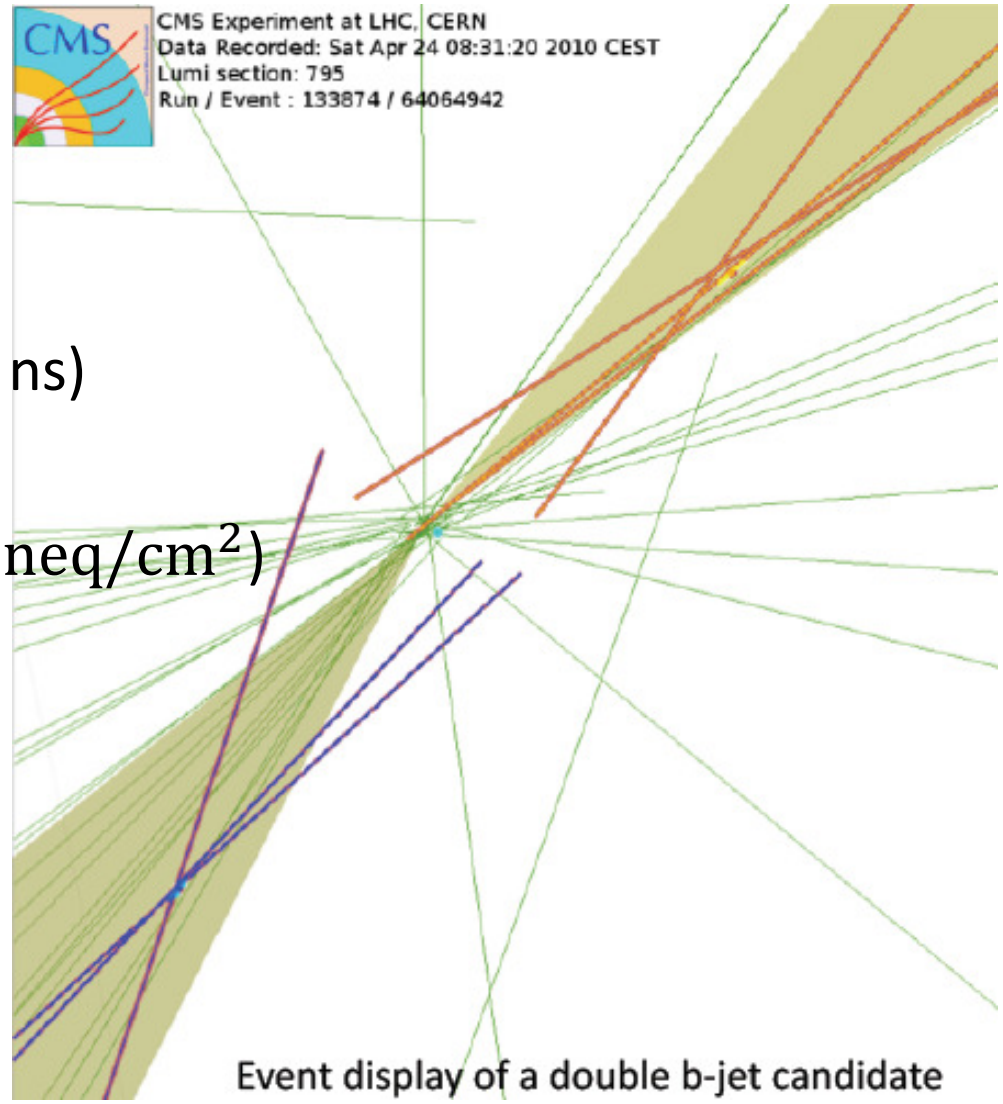
SLD experiment: $e^+e^- \rightarrow Z^0$ at SLAC

- Tiny beam spot (2 µm)
- VXD-3: 3.2×10^6 pixels ($20\ \mu m\ \times 20\ \mu m$)
- Unsparsified readout at 5 MHz
- Only possible due to low collision rate (120 Hz)

Pixel Detectors

Characteristics:

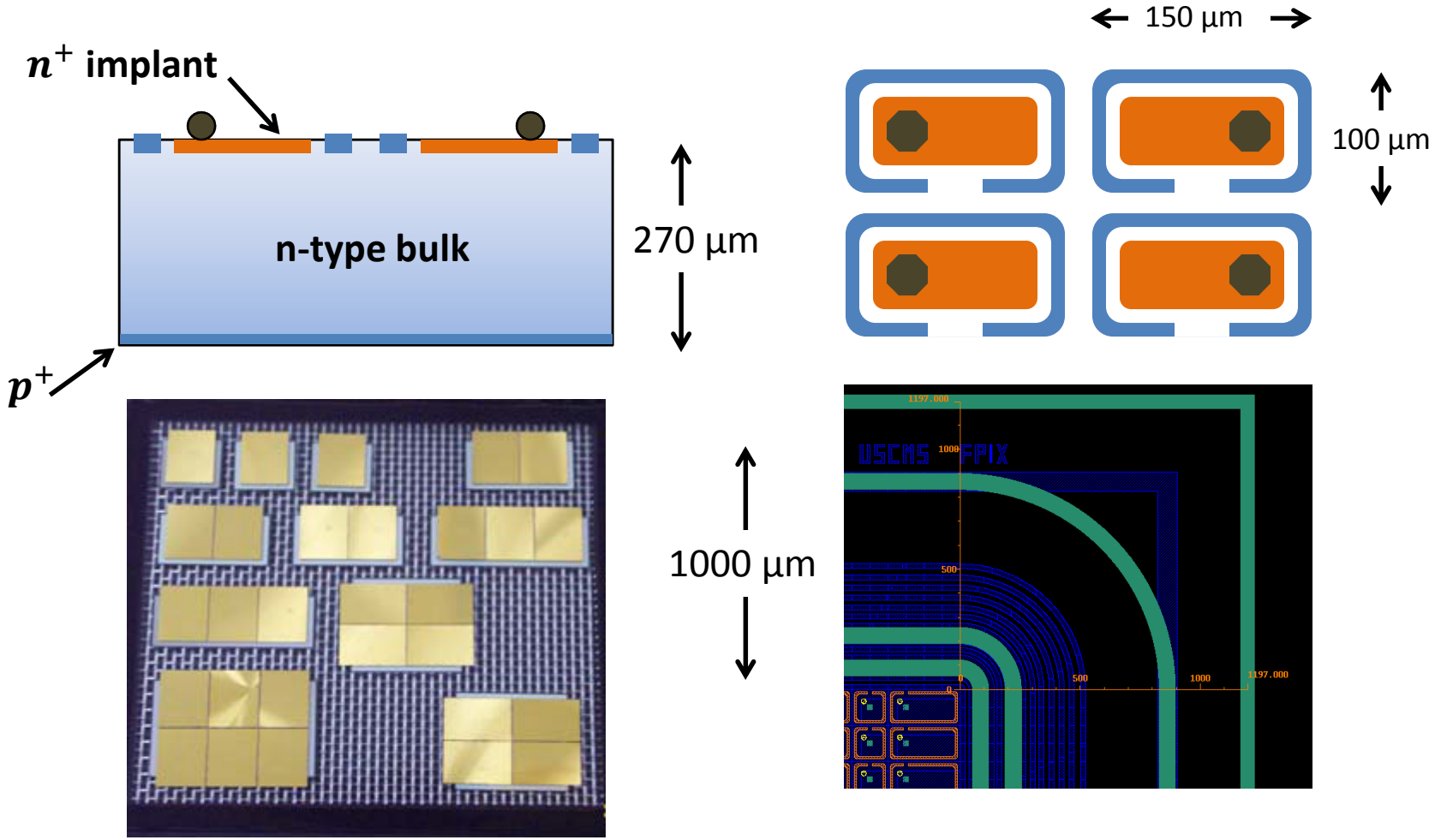
- Better pattern recognition
- Lower occupancy
- Fast signal integration («25 ns)
- Zero suppression
- Radiation hard (up to 10^{16} neq/cm^2)
- Thin
- Good signal/noise



Event display of a double b-jet candidate

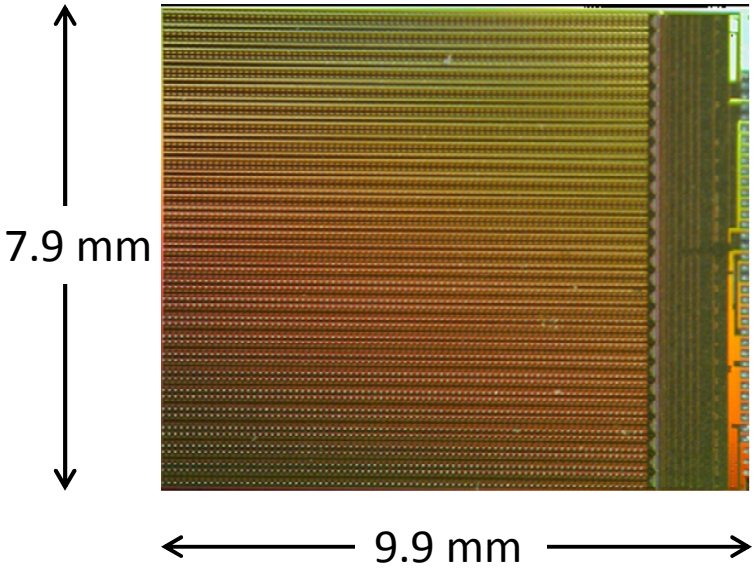
Pixel Sensor Technology

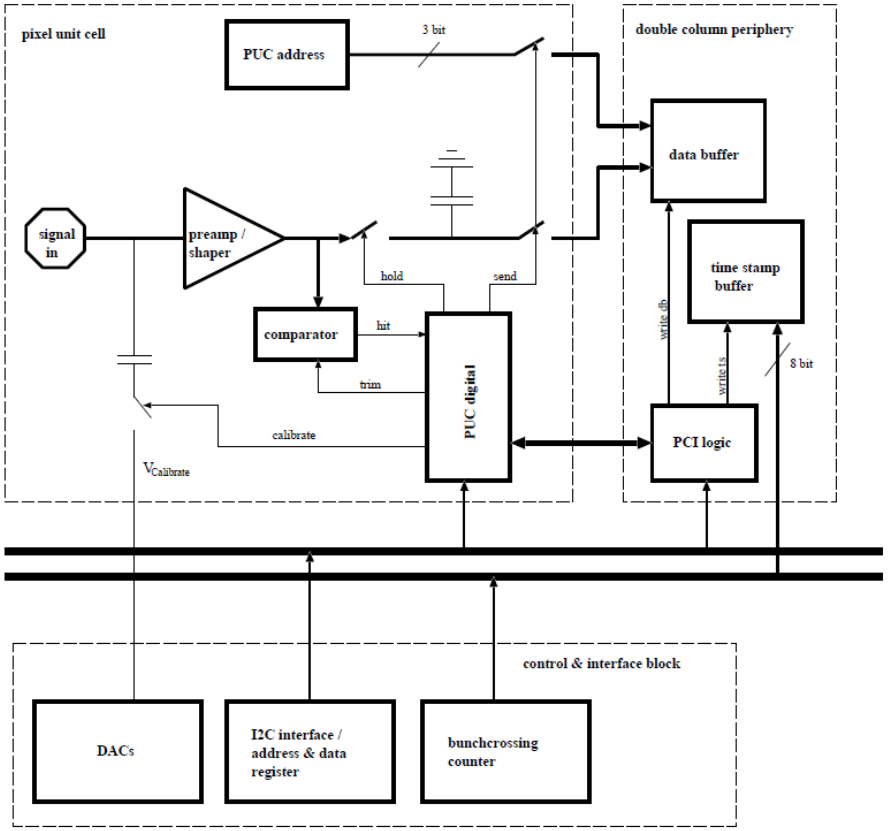
Example: CMS Forward Pixels



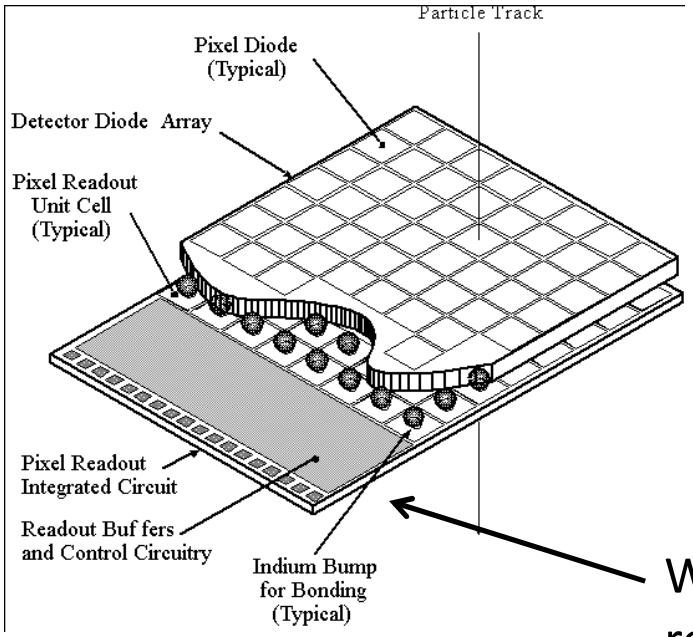
PSI46v2 Pixel Readout

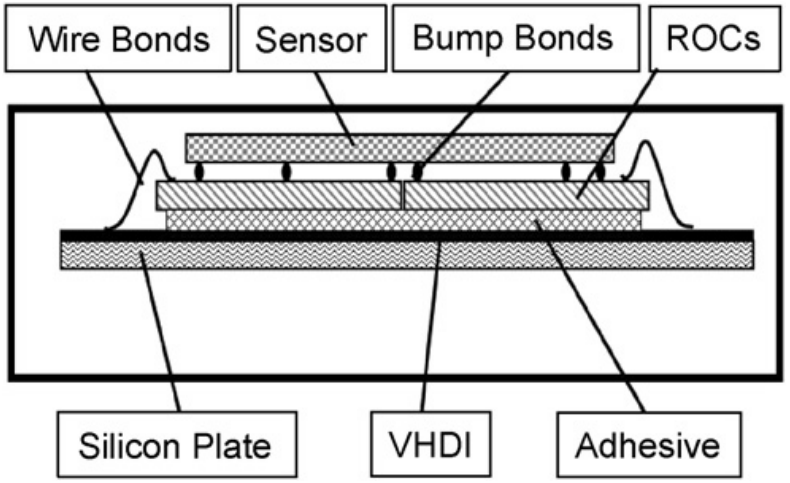
- 250 µm CMOS process with 5 metal layers.
- 52x80 array of 100 µm x 150 µm pixels.
- Data from double-columns transferred to data buffers in periphery logic.
- Input signals, clock, data, trigger.
- Output digital data at 160 MHz.





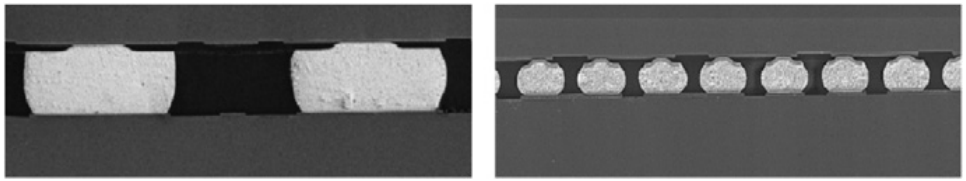
Hybrid Pixel Detectors





Wire bonds to external circuits still required at the periphery.

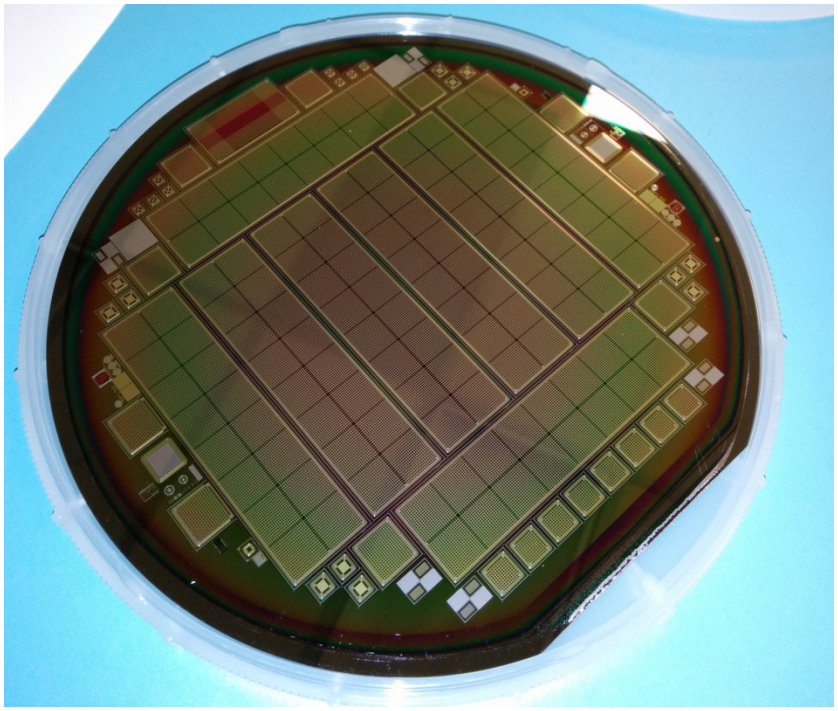
Small pitch requirements are not preferred by typical industrial applications…



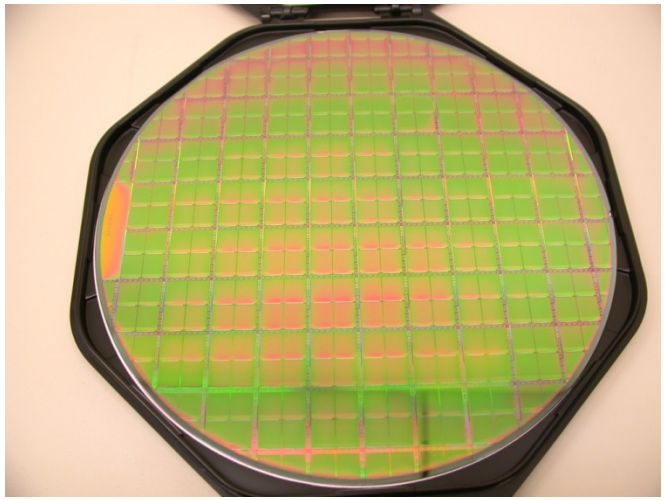
Hybrid Pixel Detectors

- Several enabling technologies are needed:
  - Dielectric materials for passivation
  - Under-Bump Metallization (UBM)
  - Bump formation
  - Dicing
  - Thinning
  - Flip-chip assembly
- *Wafer-level processing wherever possible*
- Still making use of previous enabling technologies:
  - Low mass hybrids
  - Wire bonding
  - Low mass power distribution and cables

Typical Flip-Chip Assembly Flow



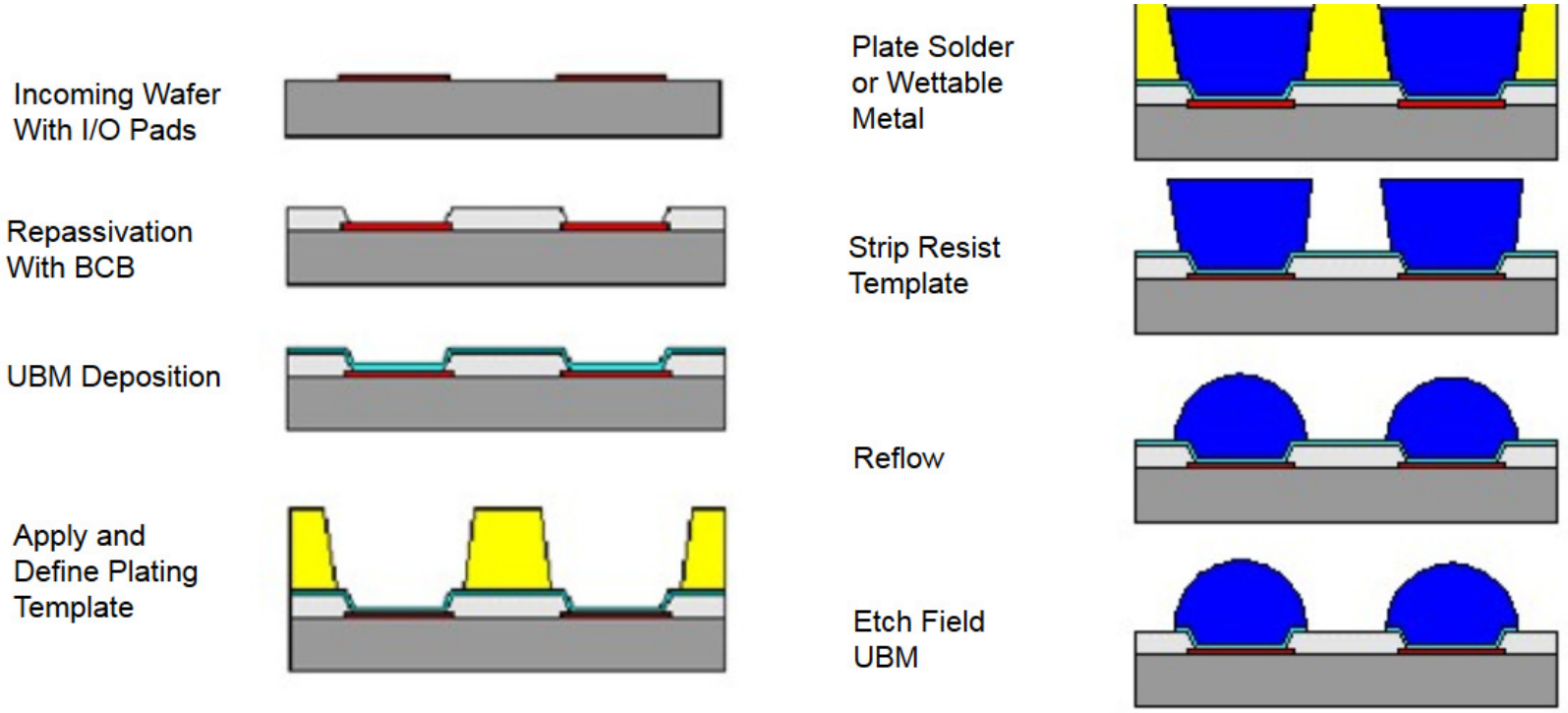
Sensor wafer containing 8 2x8 sensors for CMS Forward Pixel detector upgrade



Sensor wafer containing PSI46v2 readout chips – 66 2x2 reticles.

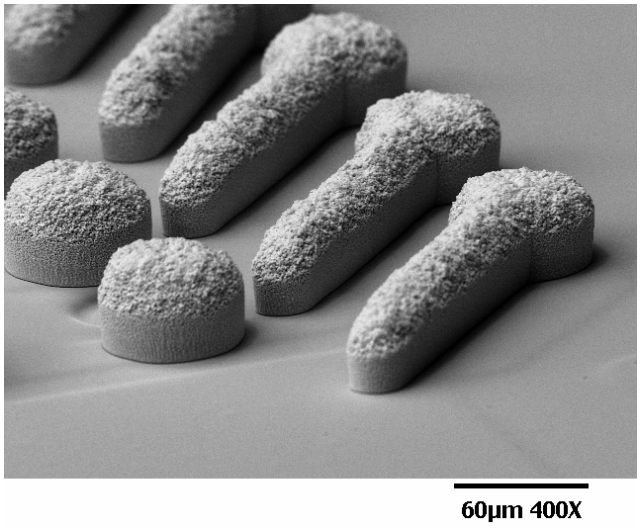
A reliable process available for over a decade.

Fine Pitched Bump Formation

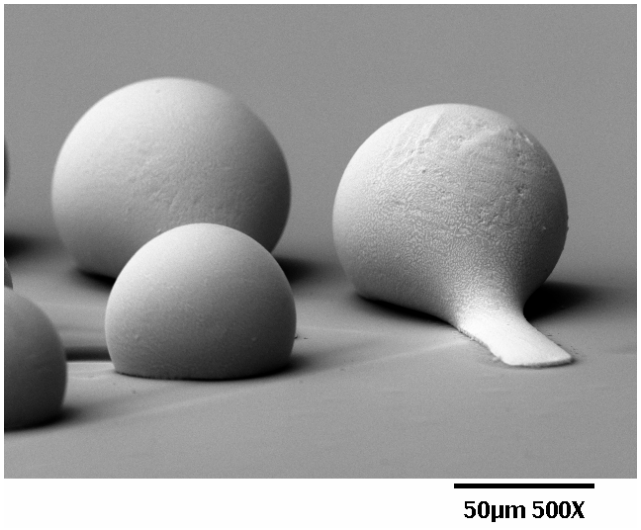


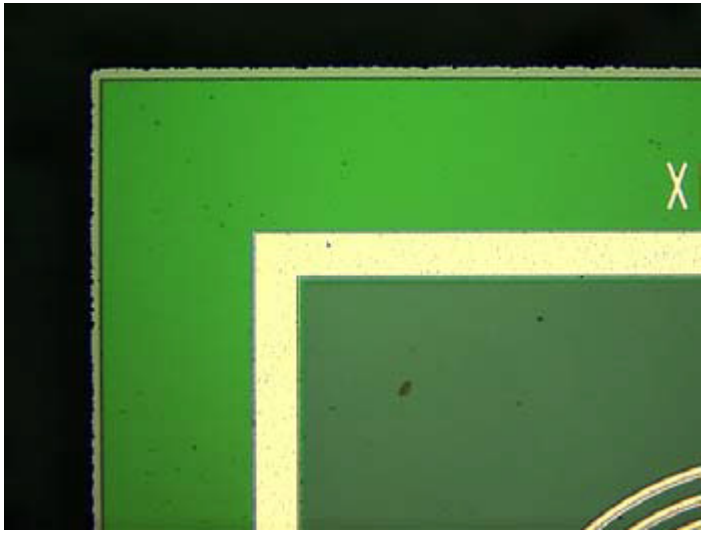
- BCB polymer applied to entire surface with openings for bump pads.
- Ti-Cu under-bump metallization.
- Solder bumps electroplated to readout chip only.
- Ni-Au deposited on sensor for solder bond.

Reflow and Dicing

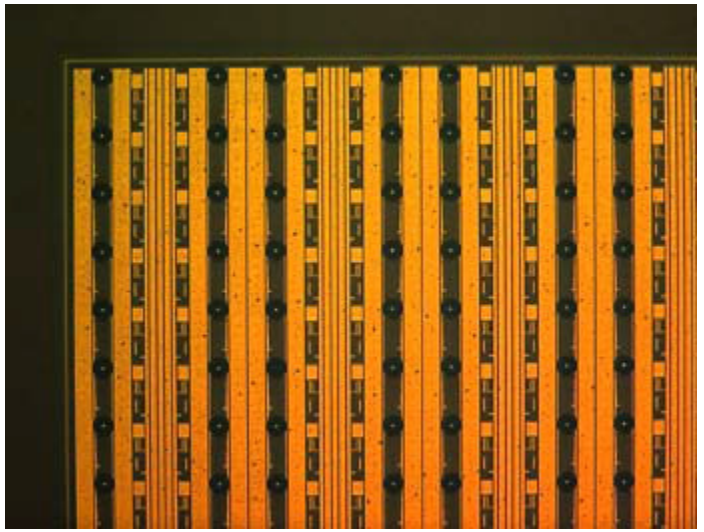


reflow

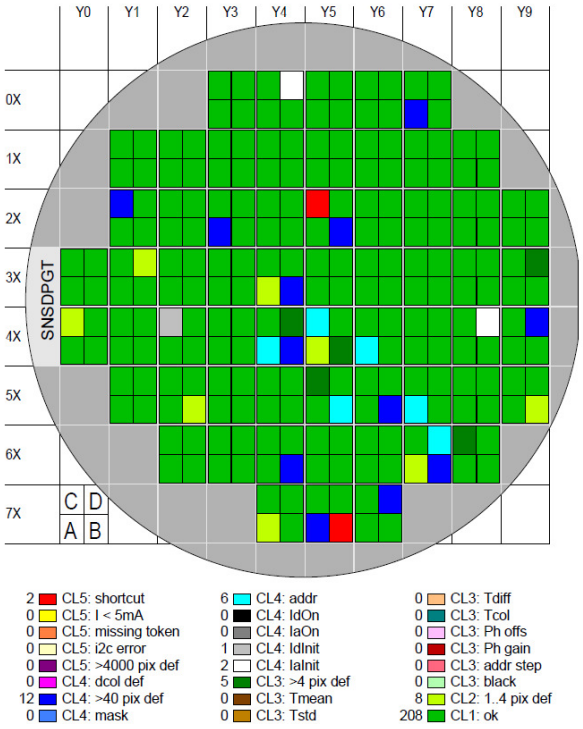




dicing
ROC and
sensor



Flip Chip Assembly and Reflow



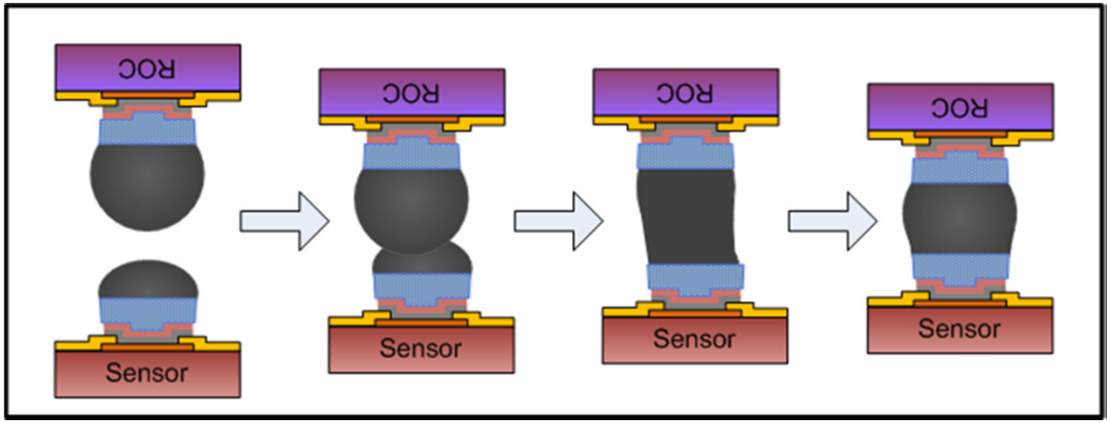
Good ROC wafer map from testing with probe card.

Solder flux – also acts as tacking compound during placement but must be cleaned.

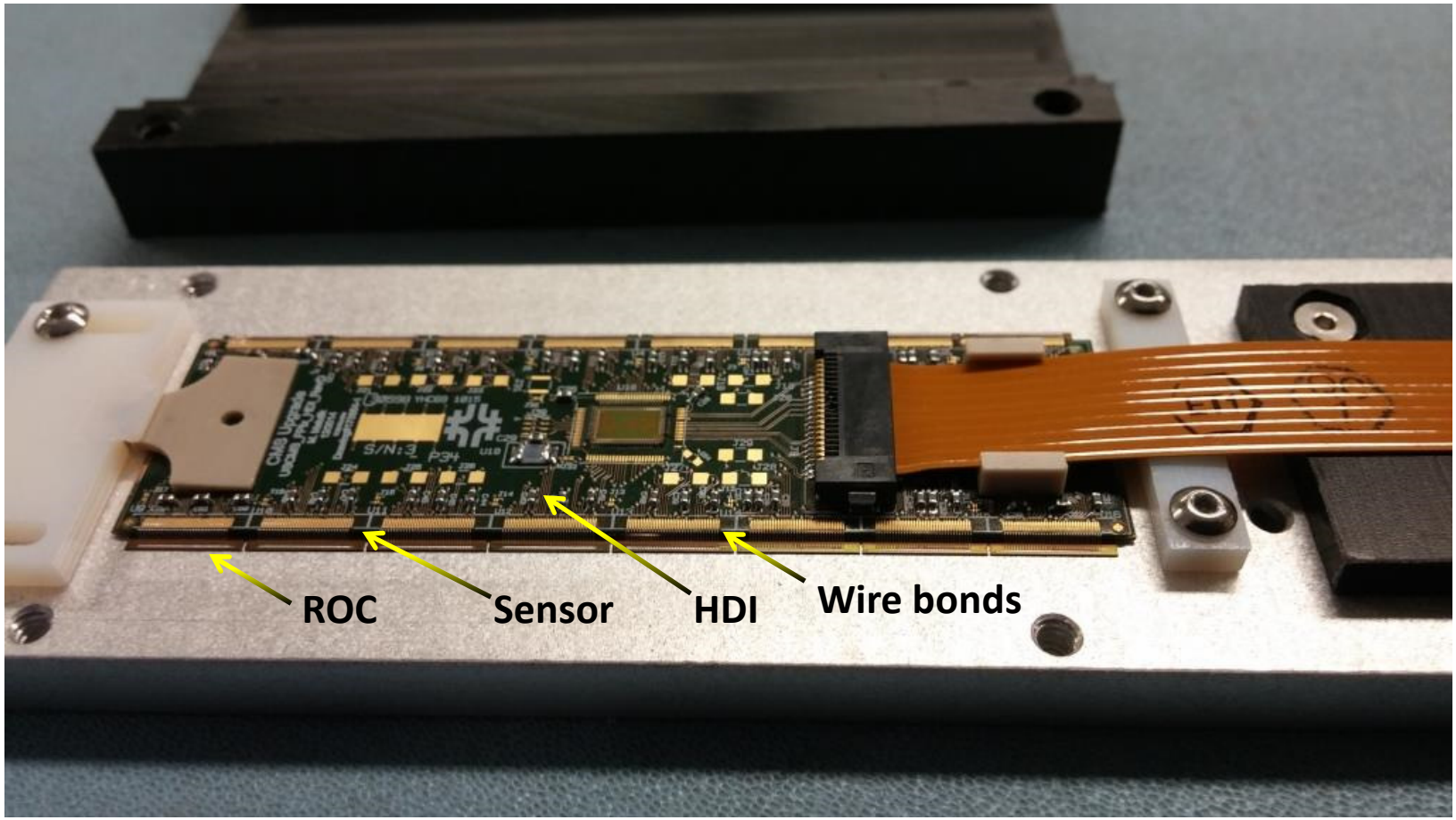
Plasma-assisted dry soldering – activation of Sn-Pb surface before reflow.

Placement of good die on sensors.

Nitrogen atmosphere reflow – self-alignment.
Placement accuracy demands at least 60% overlap.

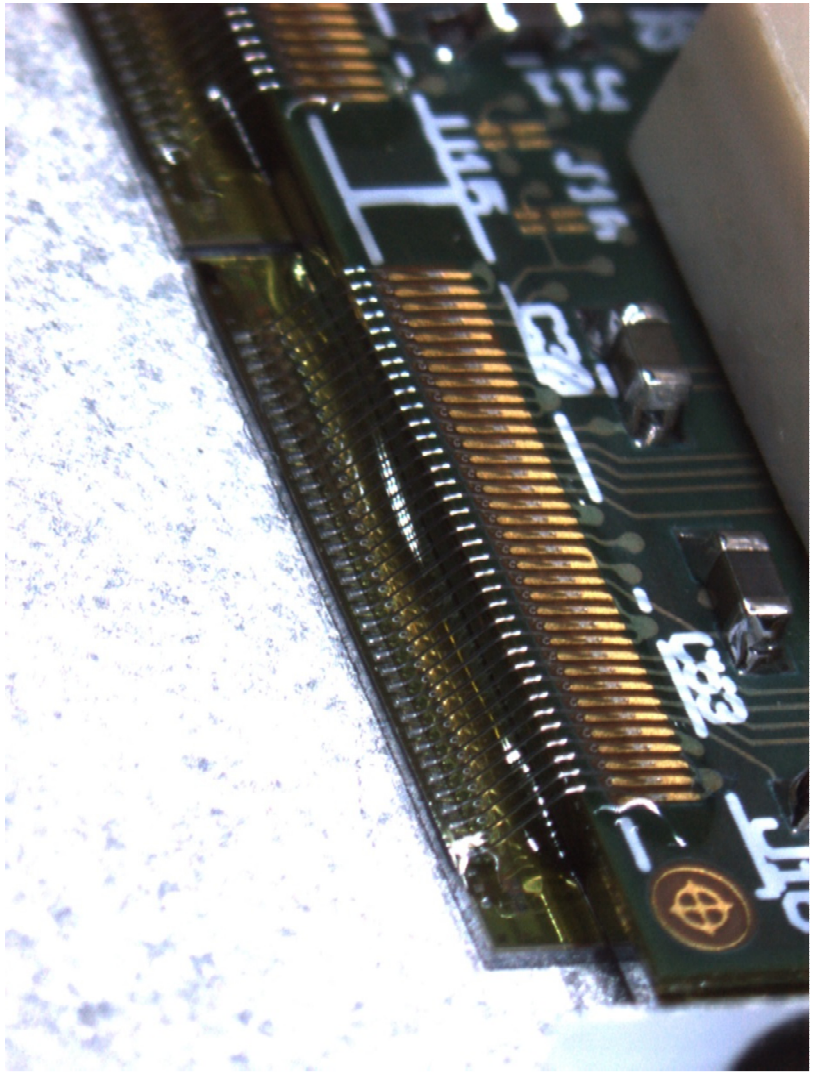


Phase 1 Upgrade FPix Modules

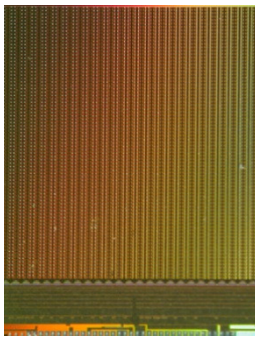


Wire Bonding and Encapsulation

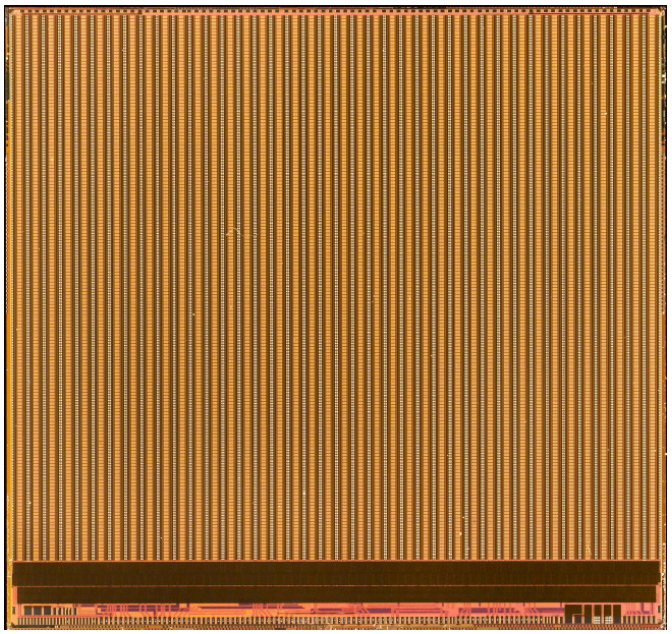
- Lots of technologies used:
  - Wire bonding
  - Encapsulation of wire bonds
  - Rad-hard adhesives
  - Thin circuits with small feature sizes
- Vertical integration has not replaced these older technologies
  - Choose appropriate technology wisely!



Large Devices



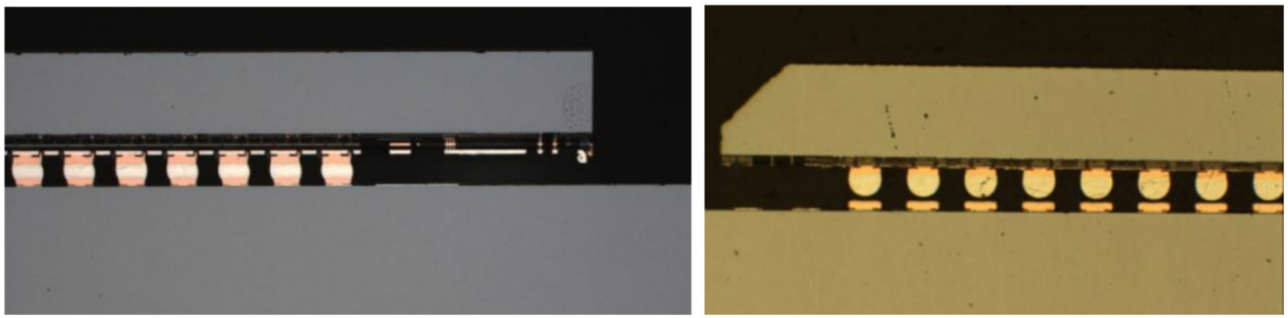
PSI46
78 mm^2
250 nm CMOS (2005)
100 µm x 150 µm pixel size
52x80 pixel array (4160)
Active area: 81%



ATLAS FE-I4B
380 mm^2
130 nm CMOS (2011)
50 µm x 250 µm pixel size
80x336 pixel array (26880)
Active area: 89%

Challenges of Large, Thin Die

- Thinning by backside mechanical grinding
- Stress relief
  - Mechanical polishing
  - Chemical mechanical polishing
  - Wet or dry silicon etch
- Front/back CTE mismatch between warps wafer during reflow



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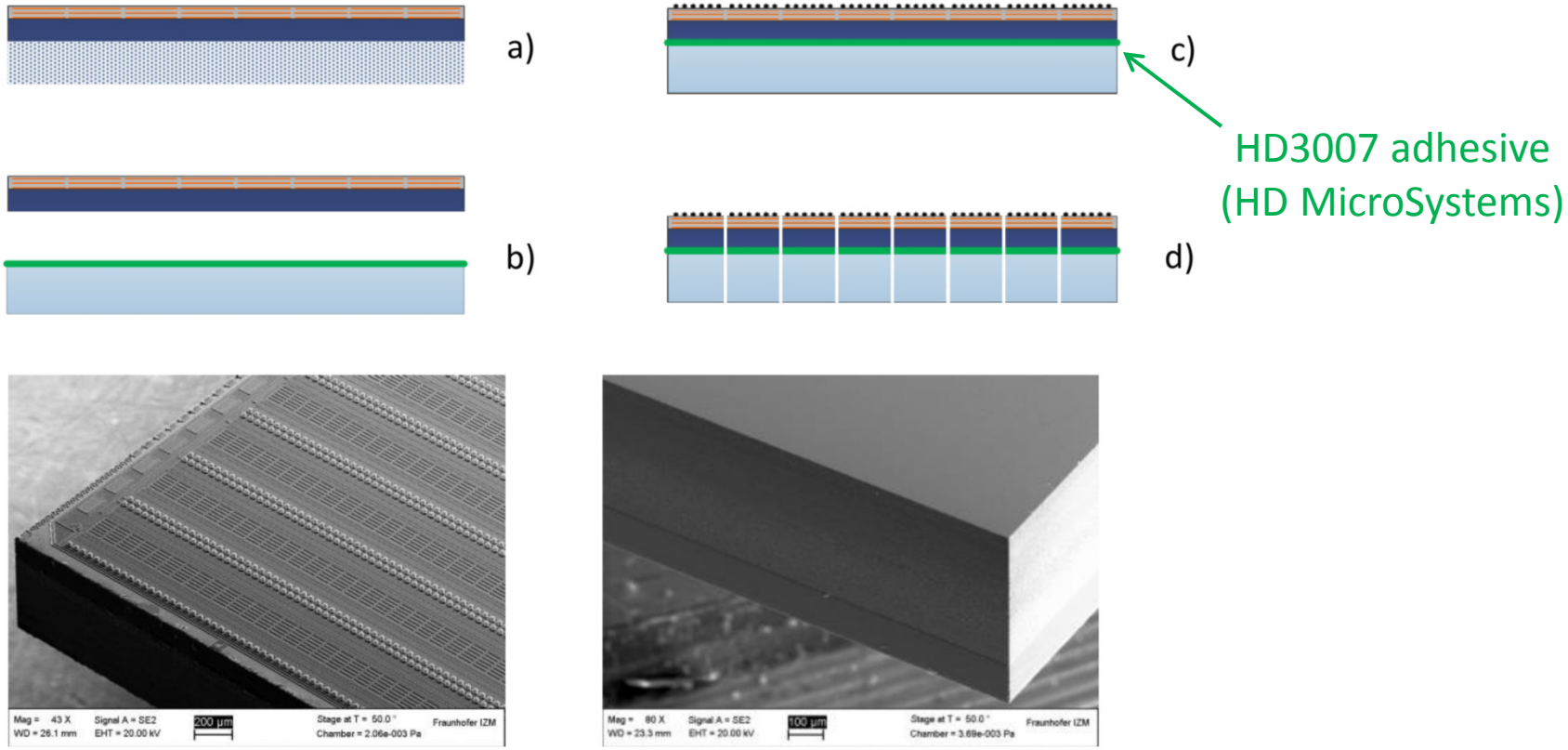
Bonding with a Carrier Wafer



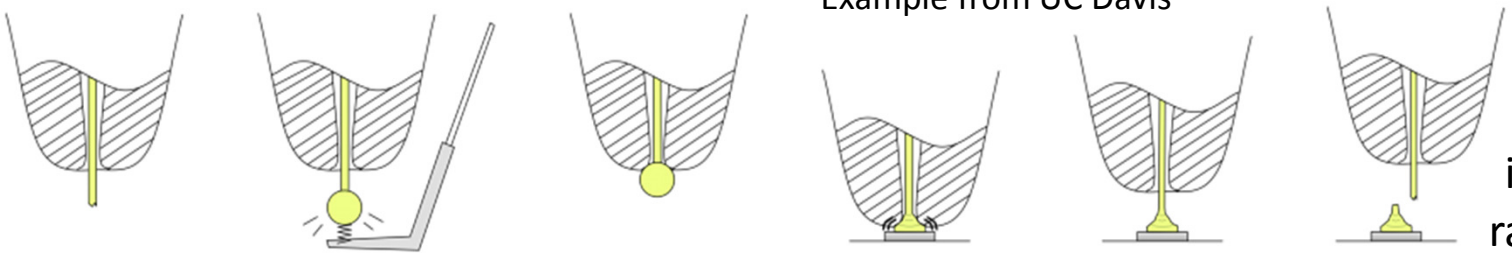
- Example material: Schott Borofloat 33
- Un-bonded using UV laser light

Low Volume Applications

- Current R&D effort: rad-hard pixel sensors
  - 3D implants, p-in-n epitaxial, (diamonds)
  - Continue to operate at $10^{16}\ \mathrm{neq/cm^2}$
  - Currently available readout chips die at 10^{15}
- Desirable to attach un-irradiated readout chips to irradiated sensors
- Avoid high temperatures associated with solder reflow to prevent annealing of damage to crystal lattice
  - Indium bumps forced together without reflow
  - Low volume alternatives

Alternatives: Gold stud bonding

Example from UC Davis



1) Capillary with wire threaded. This is the waiting state after a successful bond.

2) A pneumatic arm torches the wire with high voltage (electric flame off) to form the gold ball.

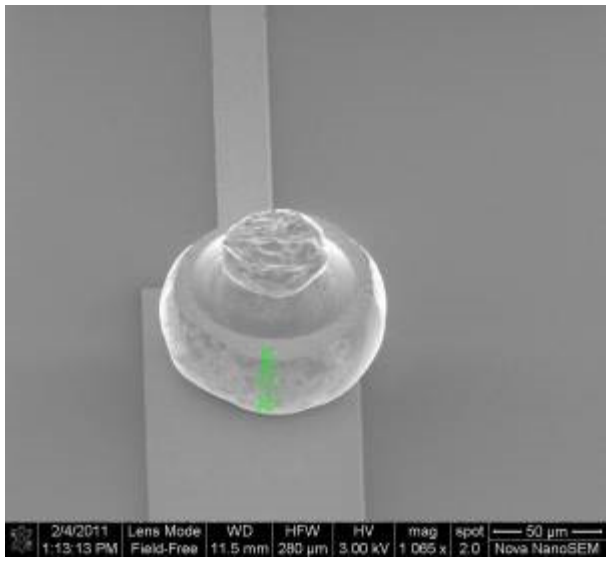
3) The ball is retracted to the tip of the capillary.

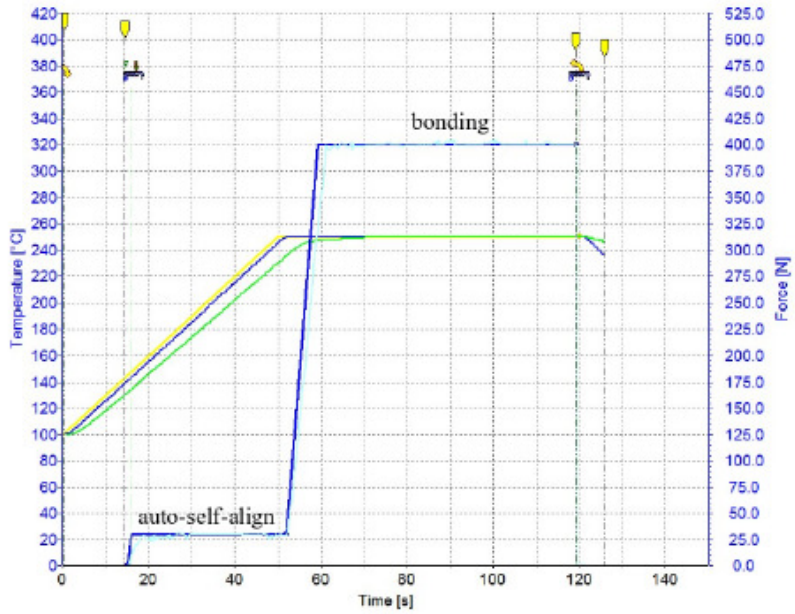
4) The capillary is lowered and bond formed using ultrasonic energy.

5) The capillary is raised.

6) Wire breaks at top of gold stud. Repeat from Step 1.

Placed individually at rate of a few Hz





Profile from Karlsruhe

Fully 3D Integration

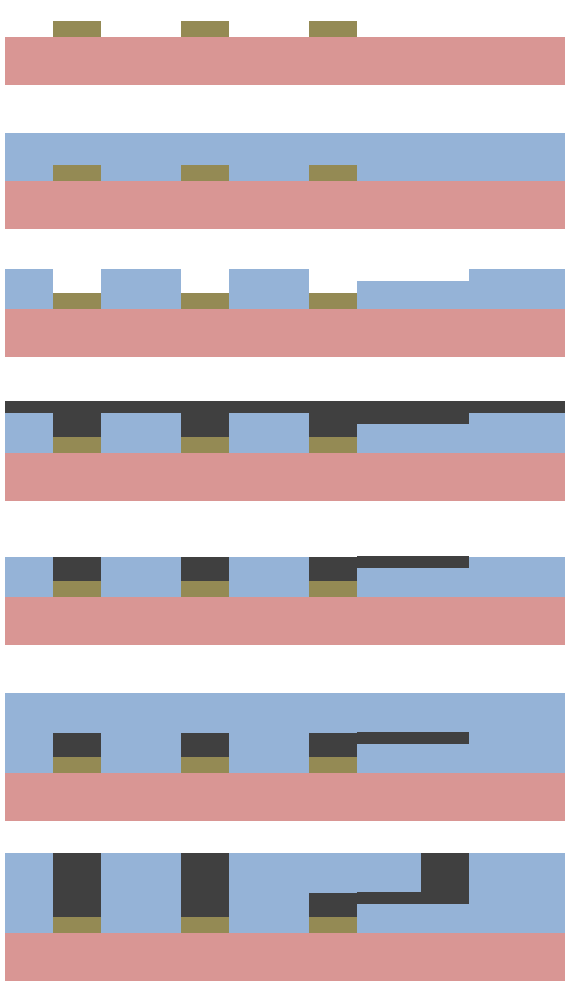
- Motivation:
  1. Reduction in system volume, mass, footprint
  2. Higher bandwidth, reduced power consumption
  3. Reduced manufacturing cost
  4. New applications
- Generally all are of interest for HEP instrumentation

  But the appropriate technology must be chosen wisely.
- Vertical Integration Technology:
  - Overview of the enabling technologies
  - Recent examples from High Energy Physics

Direct Wafer Bonding

- Bump bonding is performed at the die level
- Desirable to process entire wafers (if possible)
- An alternative is direct bonding of
  - Wafer to wafer
  - Die to wafer
  - Die to die (possibly)
- Requires several new “enabling technologies”:
  - Vertical interconnect (may include thru-silicon vias)
  - Wafer alignment and bonding

DBI Process Flow (Damascene Method)



Contact metal

Back end-of-line silicon surface

SiO_2

Etch inter-layer dielectric

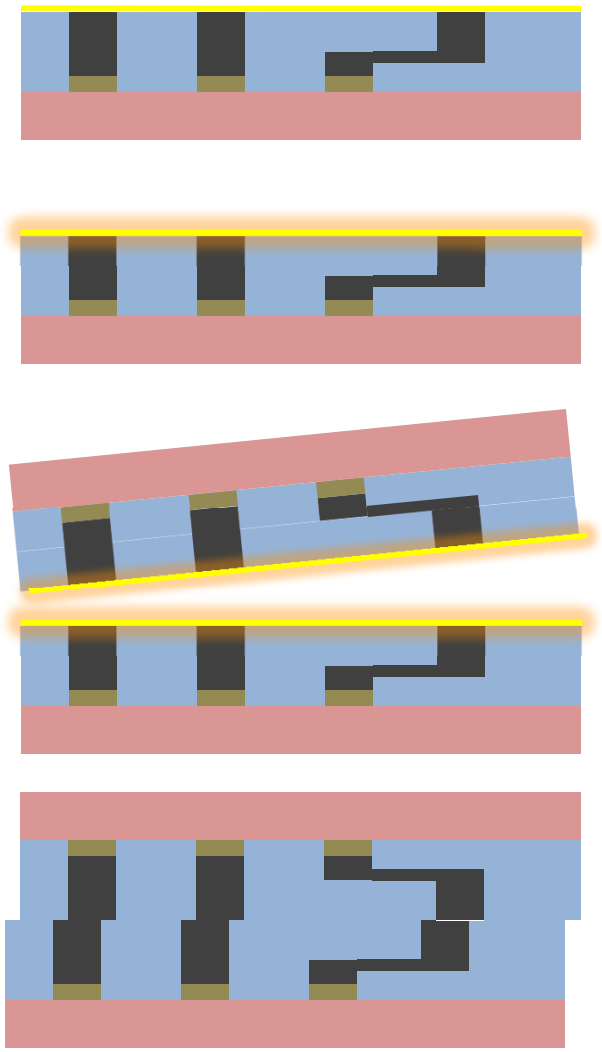
Deposit metal contact (eg. Cu)

Chemical/Mechanical Polishing

Repeat…

The result is a highly planar SiO_2 / metal surface

DBI Process Flow (Ziptronix)



Cleaning – removes a few monolayers of SiO_2 / breaking surface bonds

Activation – terminates Si bonds $Si\text{-}NH_2$ or Si-HF

Alignment and placement

Low temperature bonding

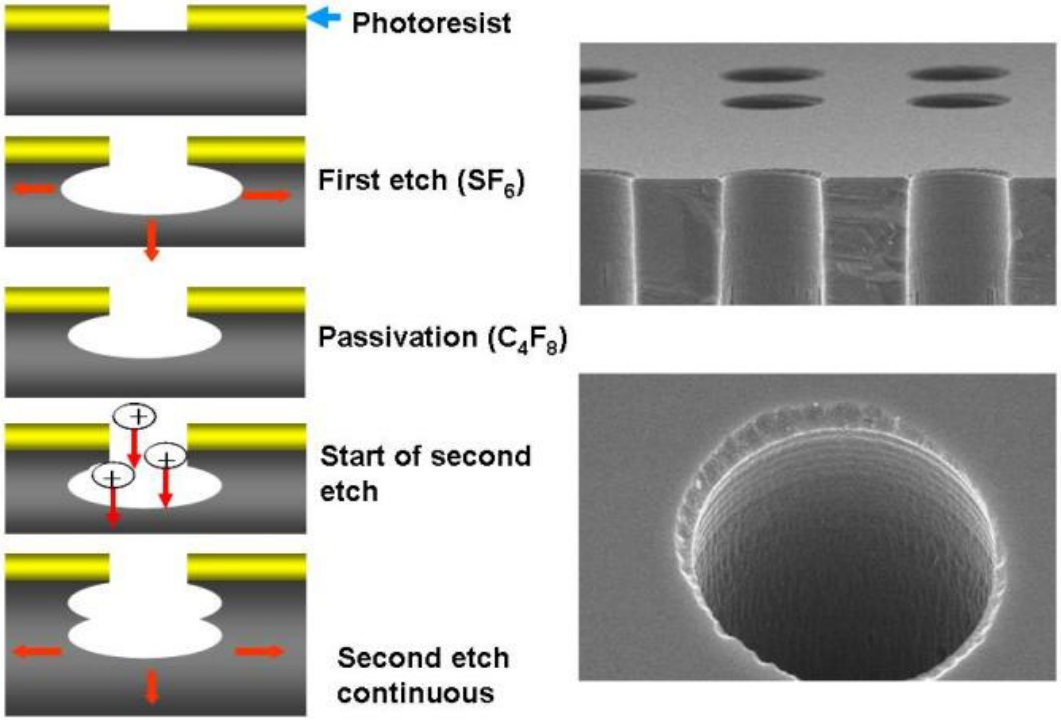
$Si\text{-}NH_2 + Si\text{-}NH_2 \rightarrow Si\text{-}N\text{-}N\text{-}Si + 2H_2$

$Si\text{-}HF + Si\text{-}HF \rightarrow Si\text{-}F\text{-}F\text{-}Si + H_2$

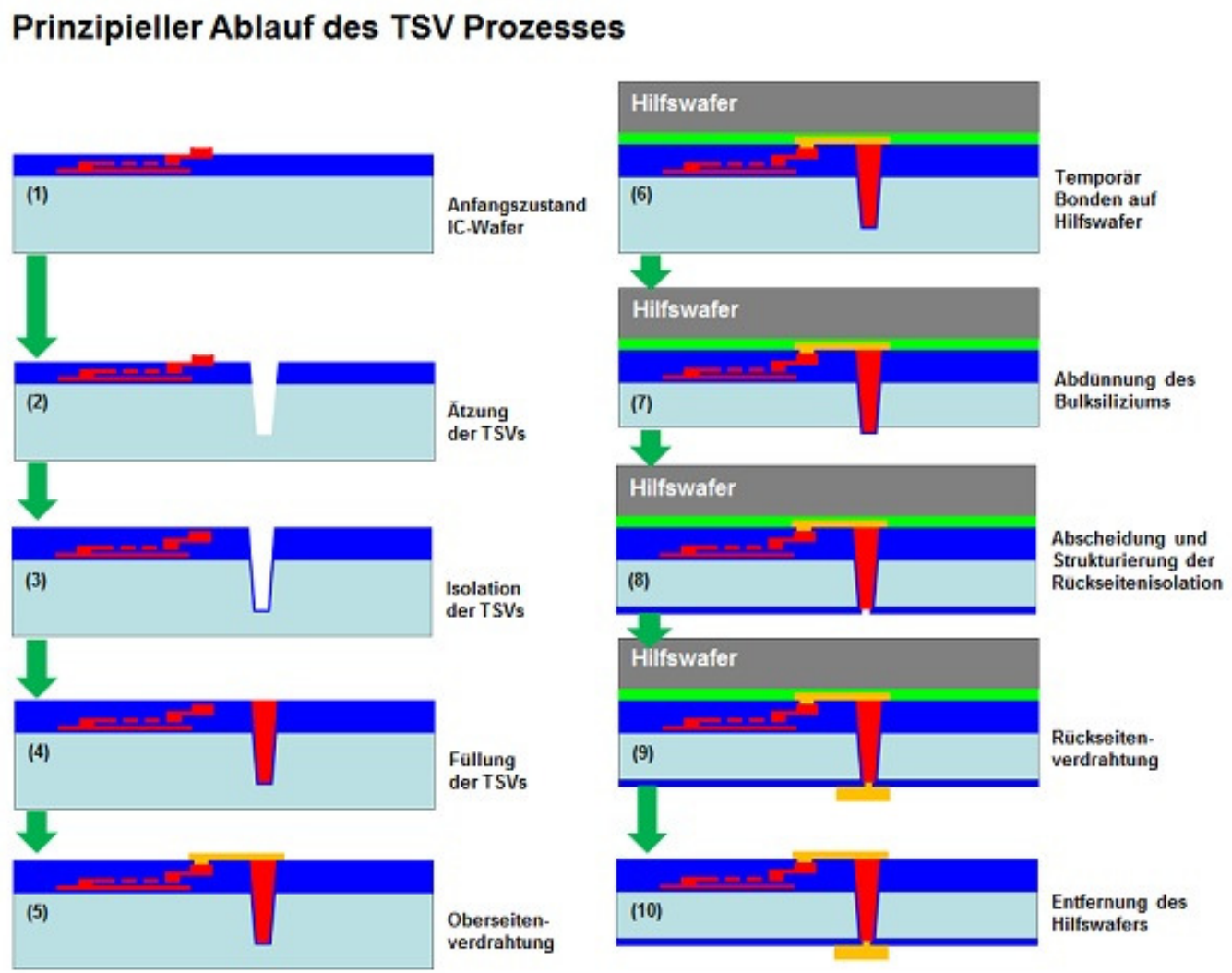
Placement accuracy < 1 µm

Thru-Silicon Vias

- The DBI Process can join wafers front-to-front.
- Stacking more than two wafers requires front-to-back connections.
- Thru-silicon vias: DRIE, passivation, seed layer, metal deposition
- Wafer thinning



Thru-Silicon Via Formation



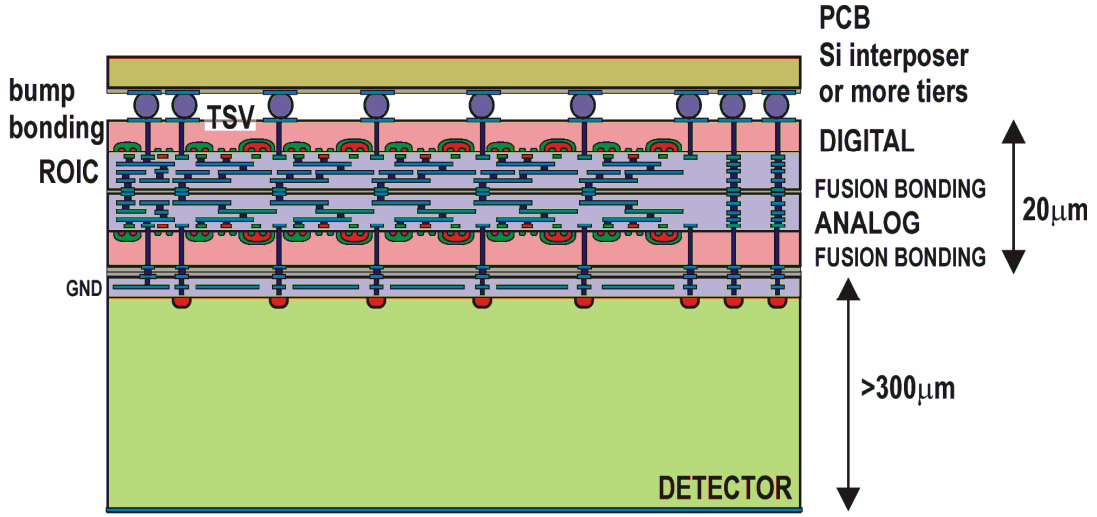
Vertical Integration in HEP: VIPIC Project

Vertically **I**ntegrated **P**hoton **I**maging **C**hip

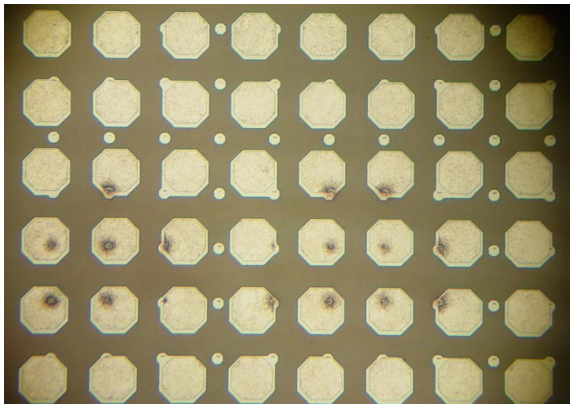
- Targeting X-ray photon correlation spectroscopy:
  - Current generation of cameras has 1 kHz frame rate
  - Next generation would like
    - Large detector area
    - Dead-time-less readout
    - Time resolution of 10 ns
    - Frame rates approaching 100 kHz
- Collaborating Institutes:
  - BNL, FNAL (US) and AGH-UST (Krakow Poland)
- Disclaimer:
  - Grzegorz Deptuch and others are the real experts

VIPIC Project

- Demonstrates a 64x64 array of 80 µm x 80 µm pixels
- Analog and digital circuits fabricated in 130 nm CMOS on different layers, interconnected using copper fusion bonding
- TSVs provide connections to sensor and pads for bump bonds.
  - Thinned to 6 µm, 1.2 µm ø, 3.8 µm minimum spacing
- No dead areas at the edges – multiple devices can be butted together



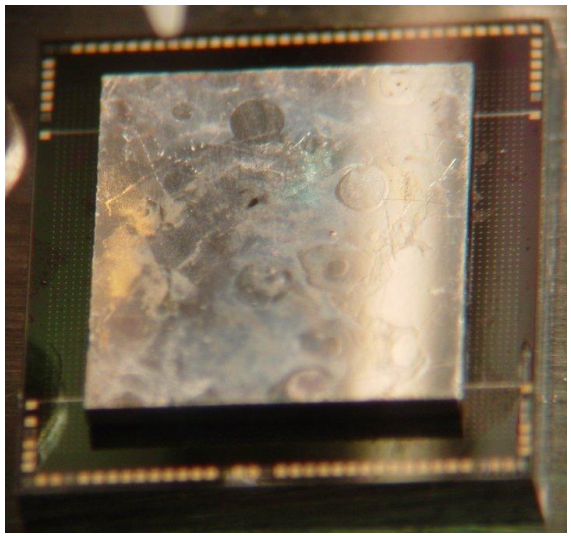
VIPIC1 Project

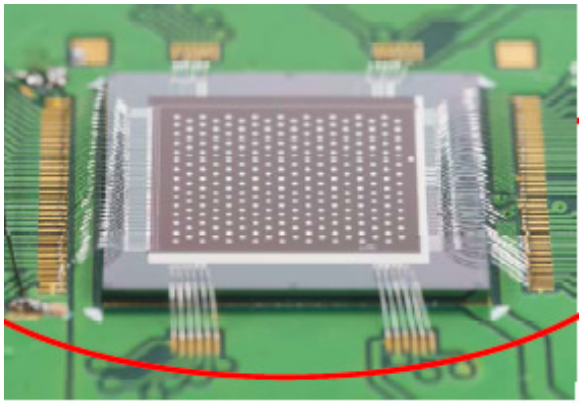


First tests interfaced the 80 µm x 80 µm pixel array with a 100 µm x 100 µm sensor.

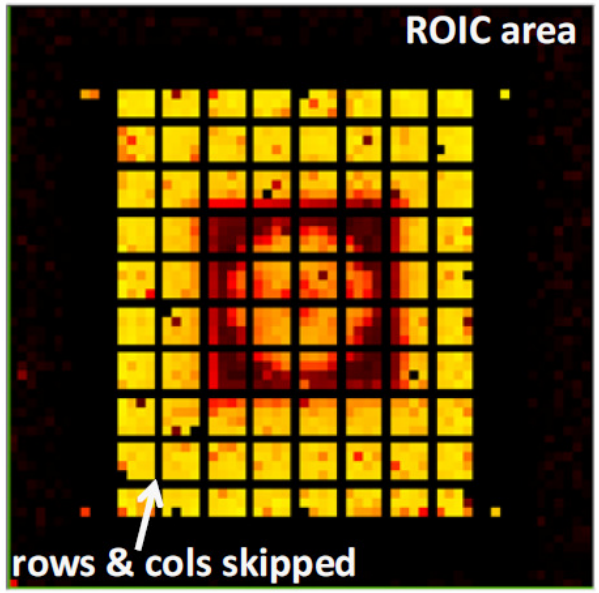
Pads for bump bonding skip every 5th pixel.

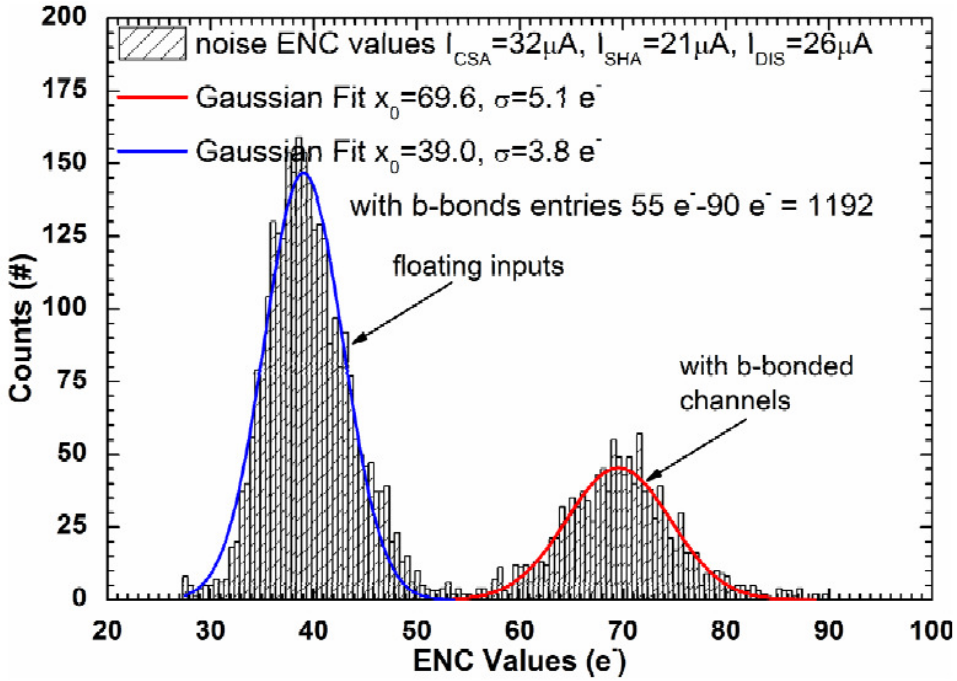
Bump bonded to interposer, wire bonded to PCB.





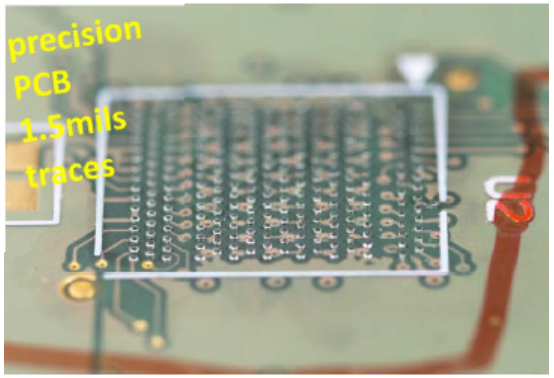
VIPIC1 Performance

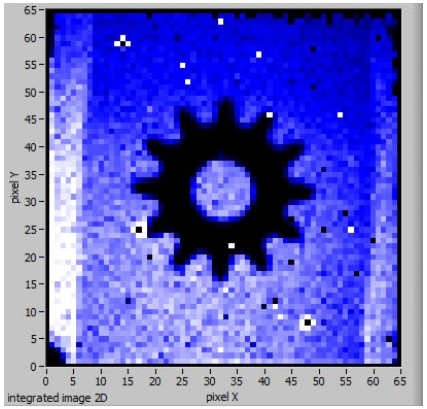


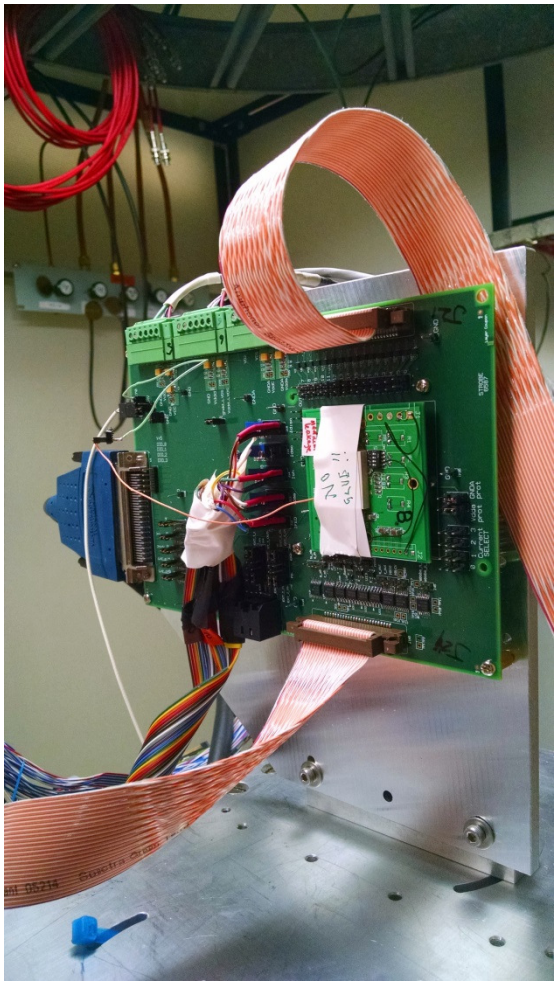


- Calibration charge injection corresponding to 4.5 keV x-ray
- Connected pixels see larger input capacitance and more noise.

VIPIC Performance







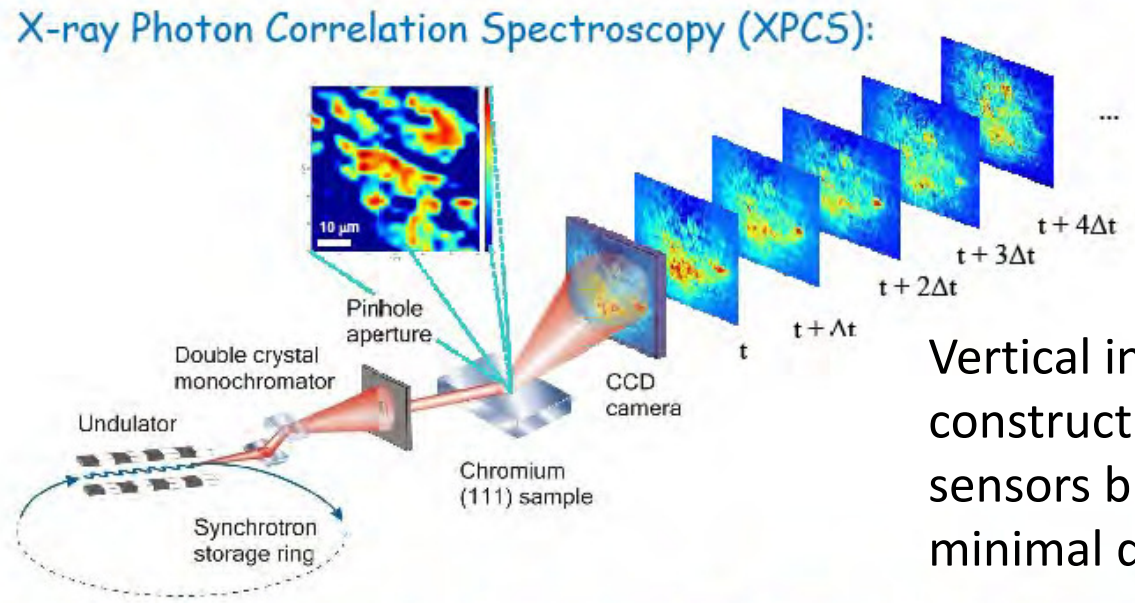
Equivalent noise is about 40 electrons.

Compare with noise on bump-bonded PSI46v2 (160 e^-).

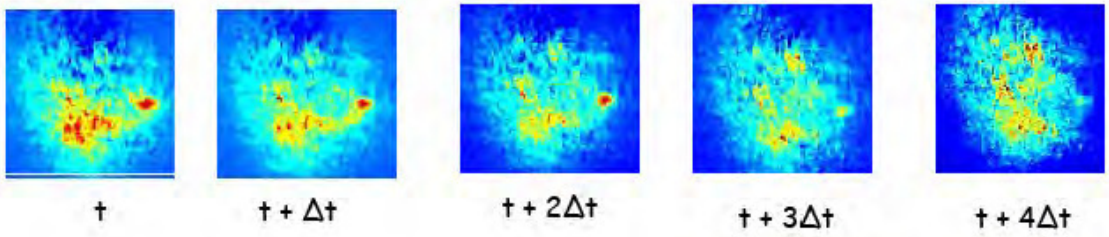
Read out in Fermilab test beam – hits correlated with reconstructed tracks.

No wire bond pads = no dead space at edges of device.

Scaling Up to Larger Arrays



Vertical integration allows the construction of a large array of sensors butted together with minimal dead space.



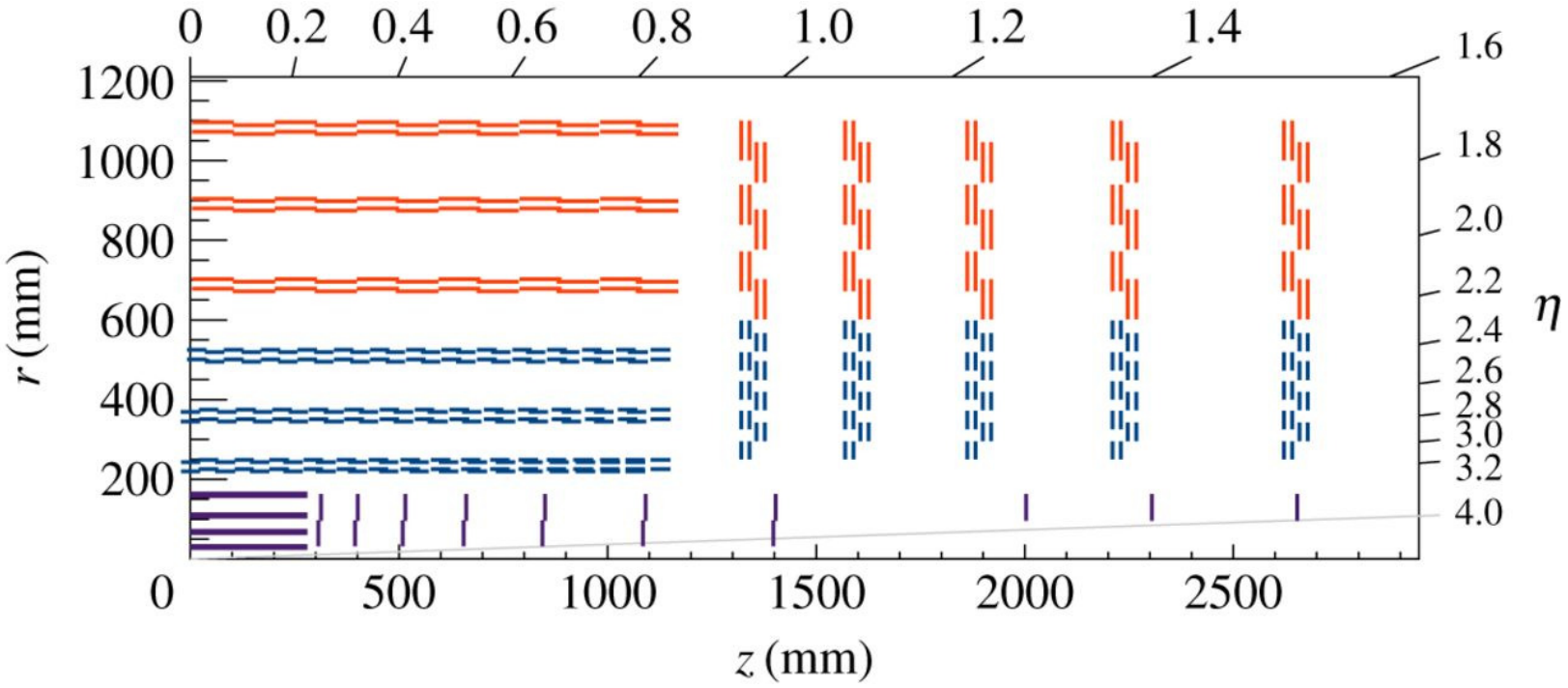
O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

Memory Applications

- Yield considerations:
  - One bad readout chip leaves a large hole in a larger sensor
  - Only assemble with known good die
  - Allow single-chip sensors to be closely spaced on all sides
- Different considerations for memory applications
  - When designed to tolerate defects, bad regions of memory reduce capacity but don't yield the entire device
  - Multiple identical tiers of logic
  - Design with space required for TSVs

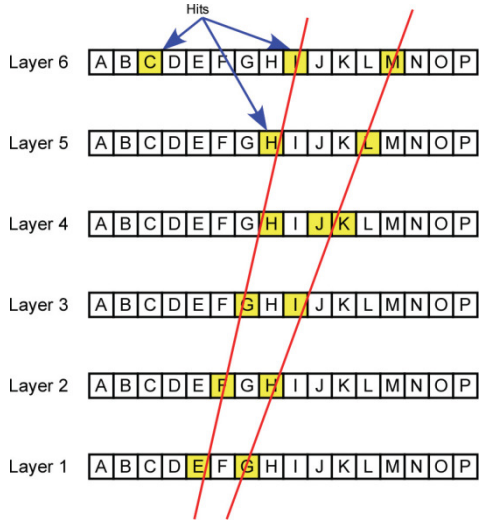
VIPRAM Motivation

- Pattern Recognition Associative Memory for fast pattern recognition in fast track trigger applications
- Tracking information in the CMS Level 1 trigger requires finding and fitting patterns of hits in the outer tracker.



Fast Track Finding

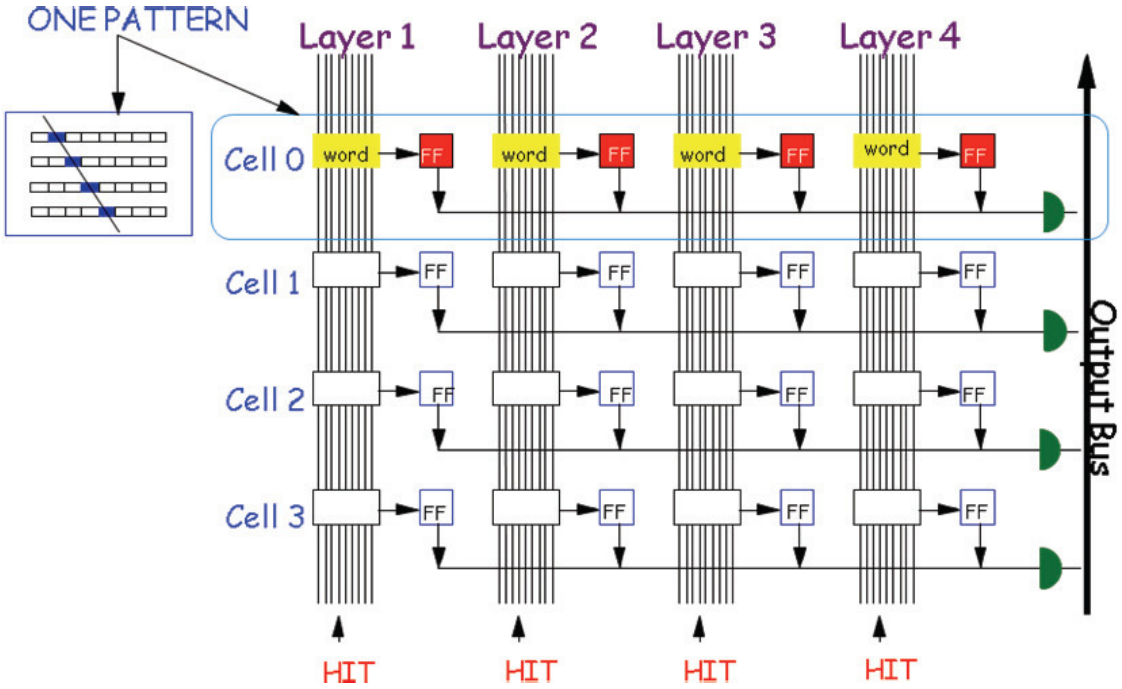
- Track reconstruction
  - N layers, n hits per layer
  - Pattern recognition, worst case $\mathcal{O}(n^N)$
  - Track fit, $\mathcal{O}(N)$
- Pattern Recognition Associative Memory
  - Stores which patterns correspond to possible tracks



Identify all acceptable patterns in parallel.

Tracking at the LHC may require 10^9 patterns!

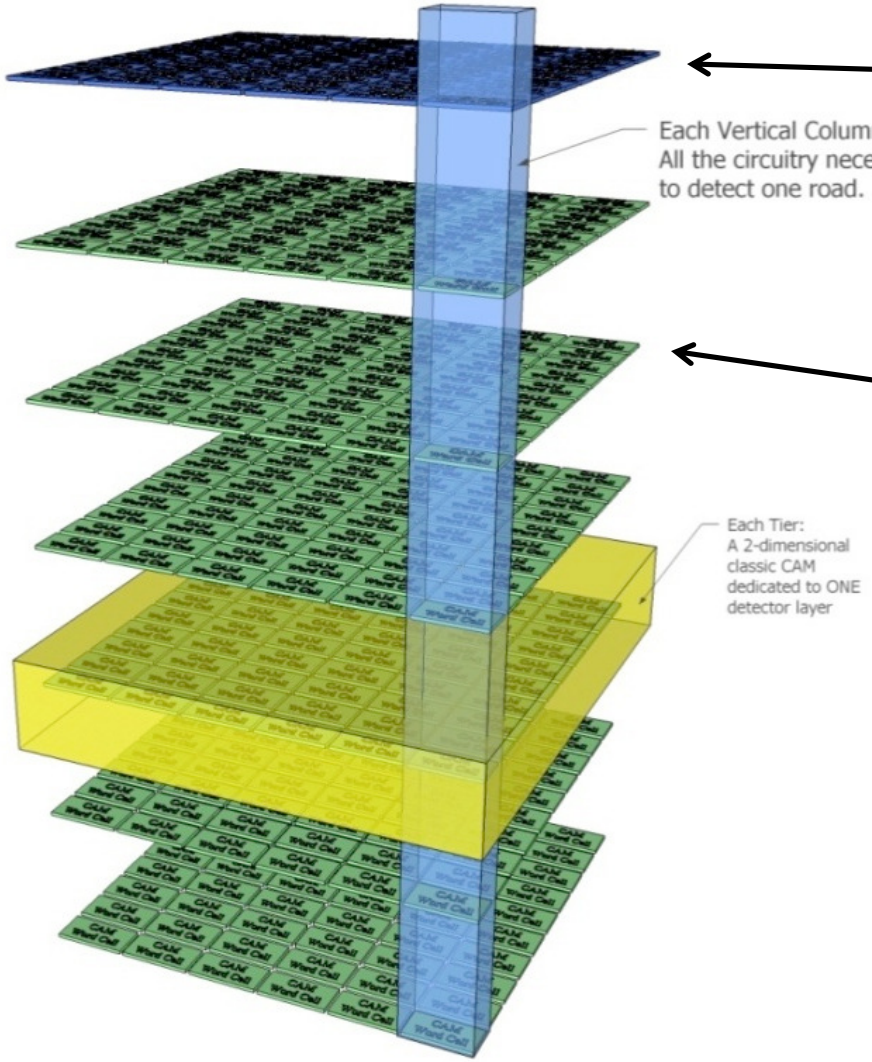
2D Implementation (AMchip03)



INFN design: 5120 patterns per chip

- Majority logic selects patterns with hits in a sufficient number of layers
- Output is the pattern address
- Routing contention in 2D: matching bits must be routed to edge of chip
- Natural solution: route matching bits vertically in 3D

3D Implementation: VIPRAM



Majority logic

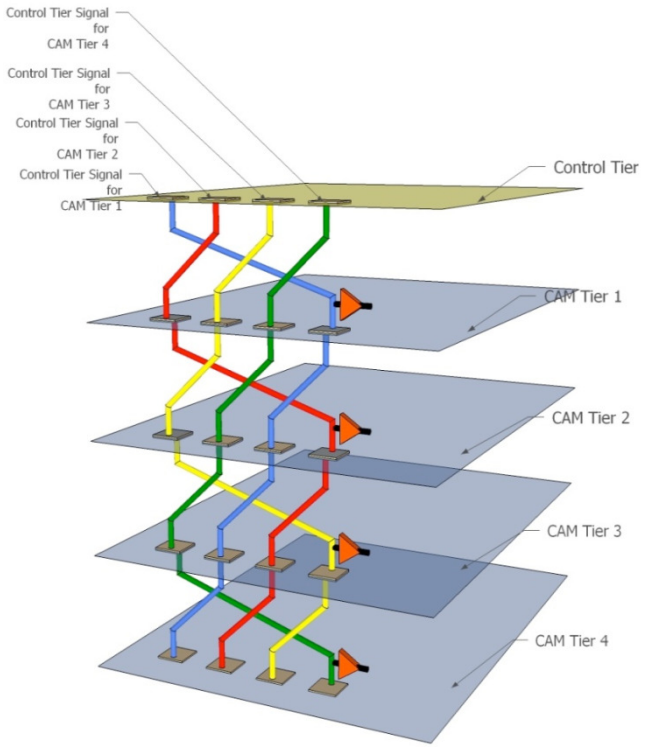
Each tier contains patterns on one layer

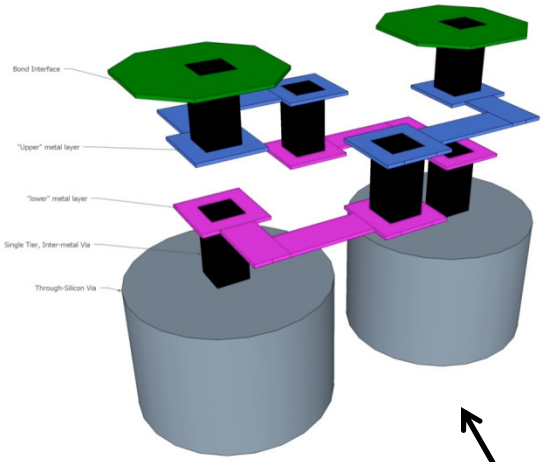
First implement in 130 nm technology with 204,800 patterns per device.

Ultimately, fabricate in 65 nm.

Vertical Integration

- Economical because each layer is identical.
- Signals routed from individual tiers to top layer using structures called “diagonal vias”:





Conventional routing with TSVs to lower tiers

Summary

- Many “enabling technologies” are needed
- Technology discussed here is no longer on the “bleeding edge”
- Modern particle physics experiments need technology that can be relied on
  - Deliver required components on schedule
  - Budget constraints
- New technologies enable new ideas
- Older technologies remain indispensable