AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of new dedicated readout electronics for LumiCal detector

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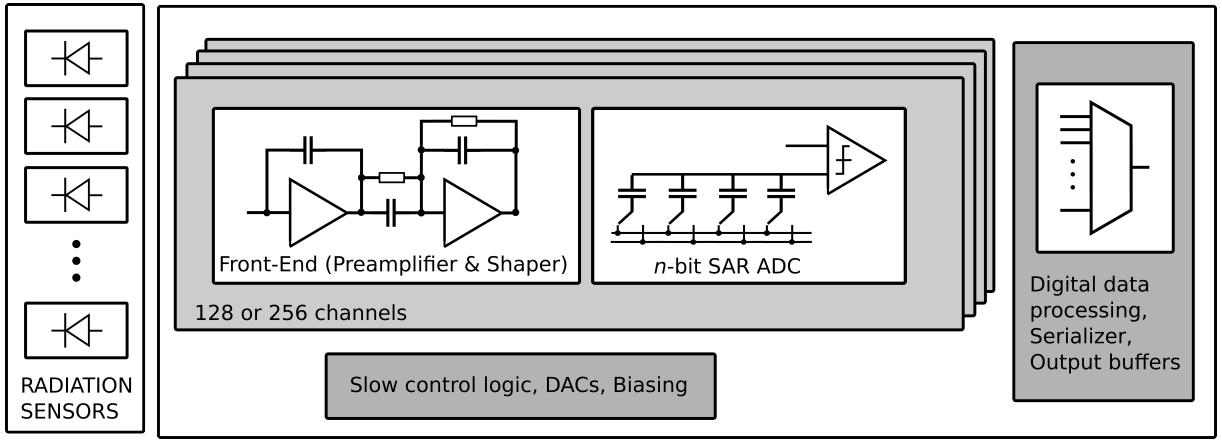
Outline

- Motivation
- Development of readout ASIC in CMOS 130 nm
- Status and Plans

Motivation
What kind of readout ASIC do we need ?

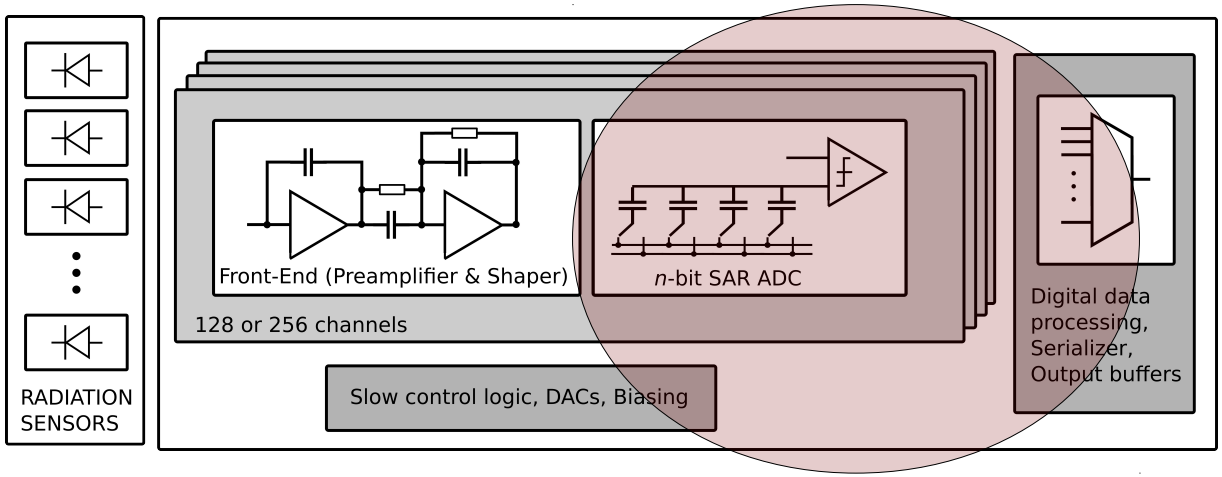


We are developing ultra-low power readout ASIC with good amplitude and time measurement for LumiCal detector

We have chosen a multi-channel readout ASIC with:

- Advanced funtionality: front-end and ADC in each channel, followed by serialization and fast data transmission
- Main features: fast and frequency scalable (f_{sample} ~DC-40 MS/s), ultra-low power, power pulsing, asynchronous ADC sampling (no clock needed)
- Main components: front-end, ADC, PLL, fast I/O, slow control, test modes, DACs, etc... – complex System-on-Chip (SoC) readout ASIC

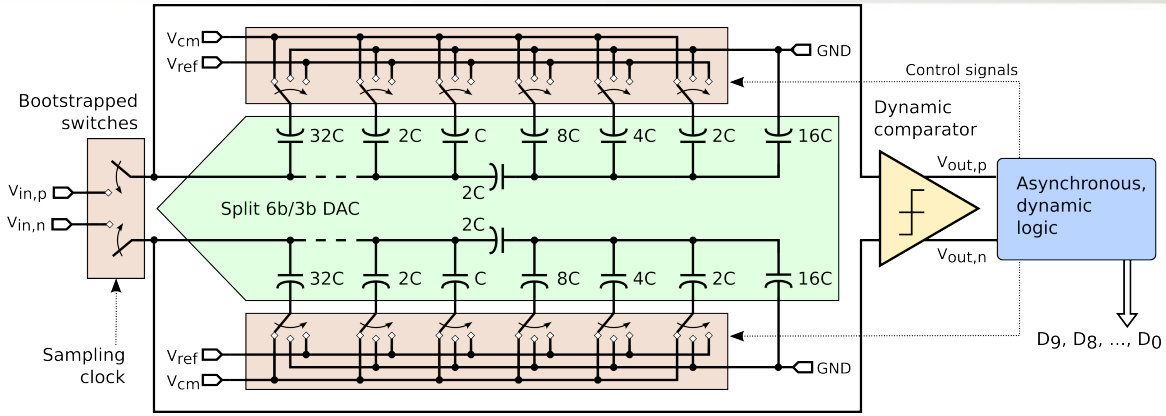
Multichannel readout ASIC
What has been already done ?



Over the past years we have made a big progress in data conversion (ADC) and serialization parts:

- Fast ultra-low power ADC has been developed
- Multichannel ADC was designed and fabricated
- Fast PLL-based serialization is under development with very promising results

Multichannel readout ASIC
Fast ultra-low power 10-bit SAR ADC

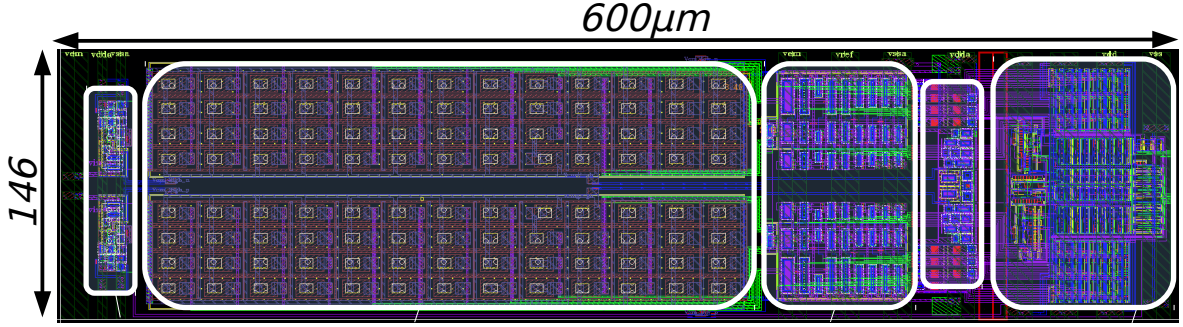


Design consideration:

- Power scalable with sampling frequency (up to >40 MS/s)
- Power cons. <1mW@40MS/s
- Power pulsing (no clk=no power)
- 146 µm pitch, ready for multichannel integration

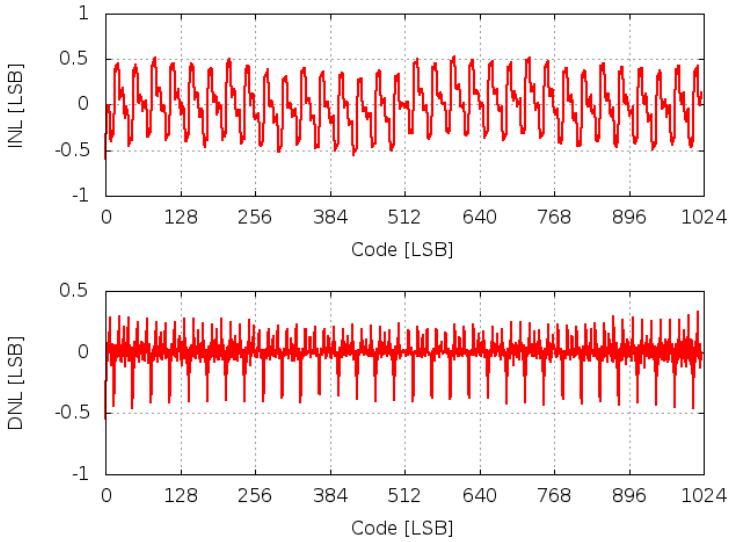
Architecture of 10-bit SAR ADC

- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing (no clk=no power)***
- Asynchronous logic – ***no clock tree, power saving, fast***

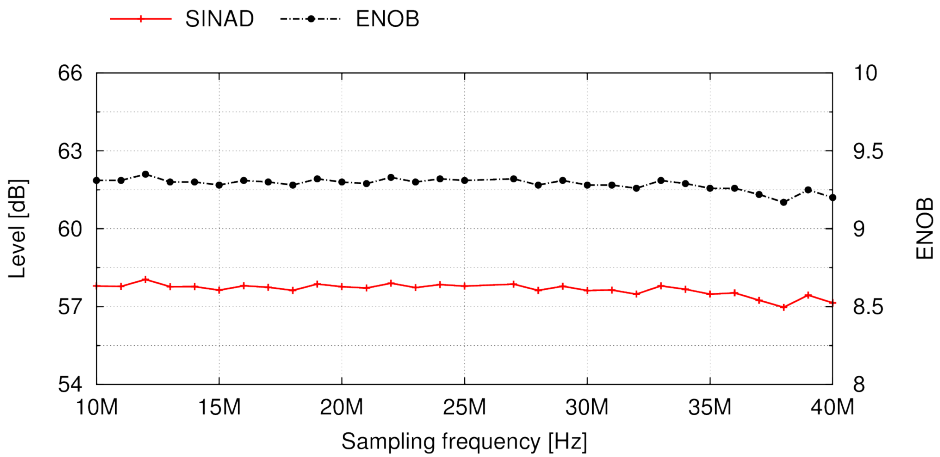


Multichannel readout ASIC
Measurements of single 10-bit SAR ADC

Static performance
example at 10MS/s



Dynamic performance
scan over f_{sample} for f_{in} at 0.1 Nyquist



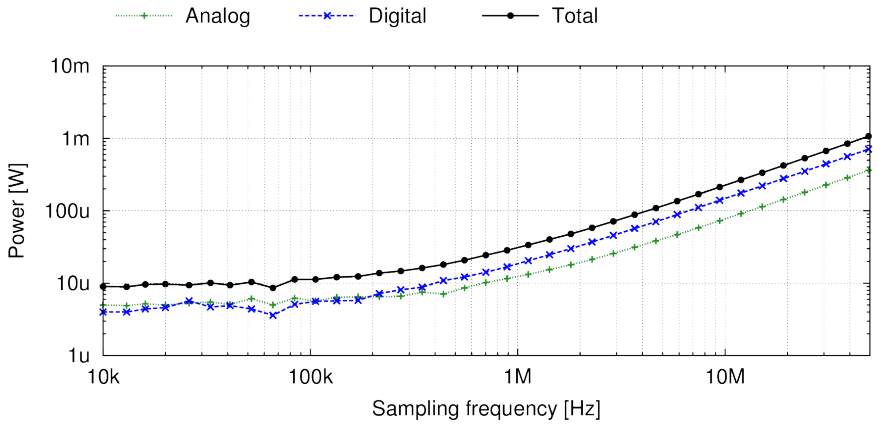
Very good ADC performance: INL,DNL > 0.5LSB and ENOB ~ 9.3

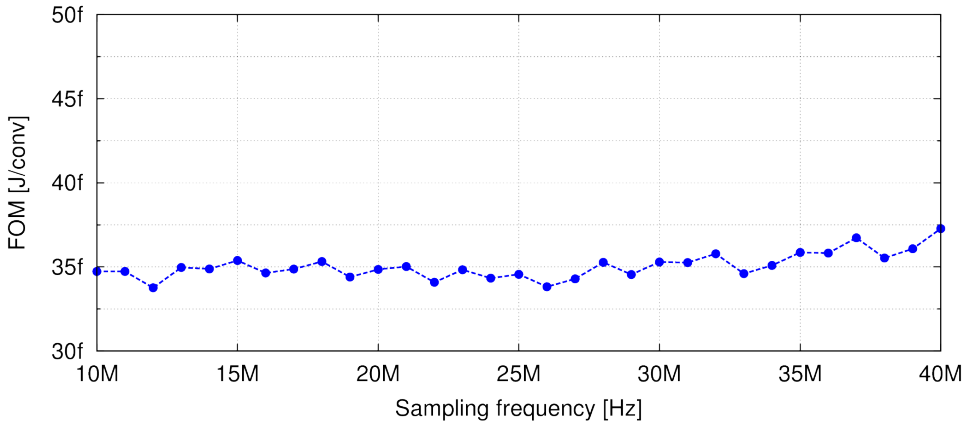
M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, J. Moron, K. Swientek. "A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors", submitted to JINST...

Multichannel readout ASIC
Measurements of single 10-bit SAR ADC

Power consumption

$$FOM = \frac{Power}{f_{sample} * 2^{ENOB}} [J/conv.]$$





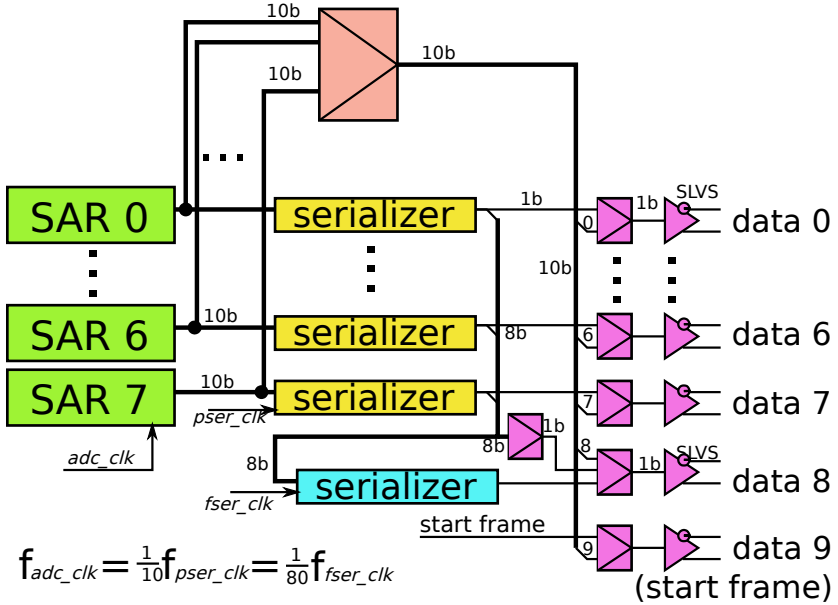
Ultra-low power consumption and excellent Figure-of-Merit

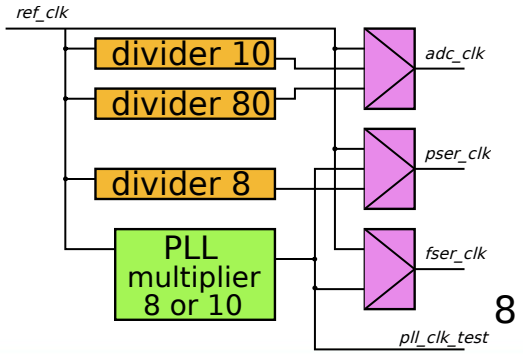
ADC performance among the best State-of-Art designs

Multichannel readout ASIC
Architecture of 8-channel 10-bit digitizer

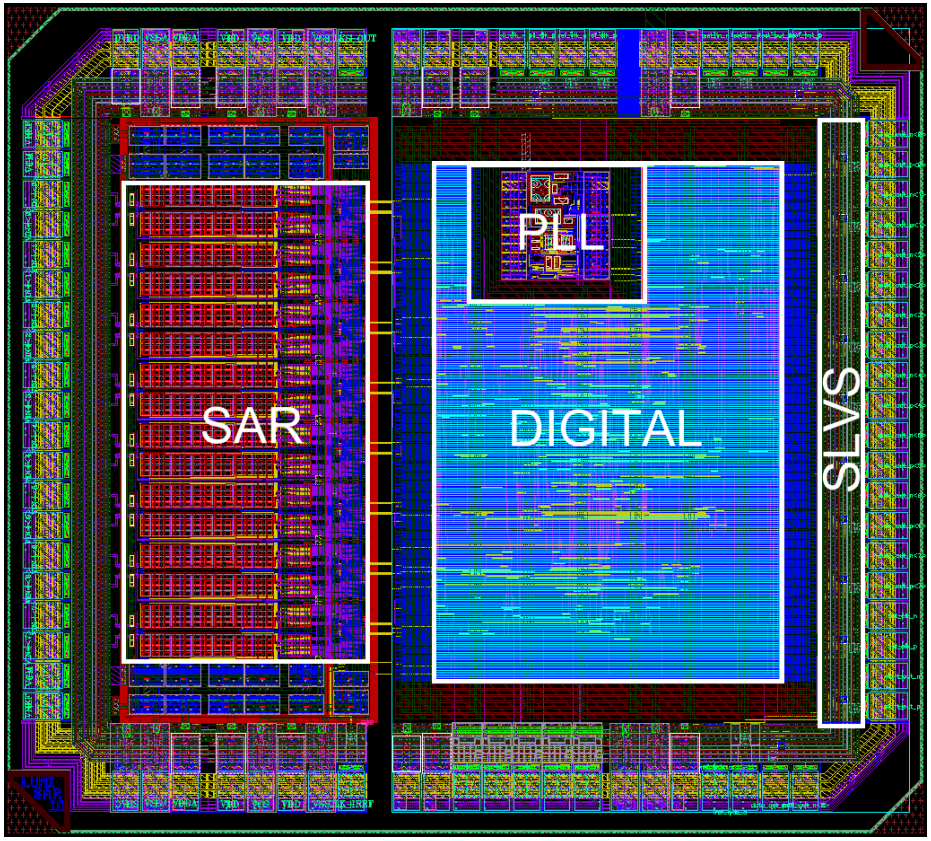
Specifications & main features:

- Technology CMOS 130 nm
- 8 channels of 10-bit SAR ADC
- Multimode multiplexer/serializer:
  - Single ADC mode: single channnel output
  - Parallel mode: one output per channel (10-bit serialization with faster clock)
  - Serial mode: one output per all channels (double serialization: 10-bit x 8 channels)
- Additional test modes, with counters/pseudo-random data instead of ADC output, to verify serialization/transmission
- PLL for data serialization
- High speed SLVS interface (>1GHz)
- Power pulsing

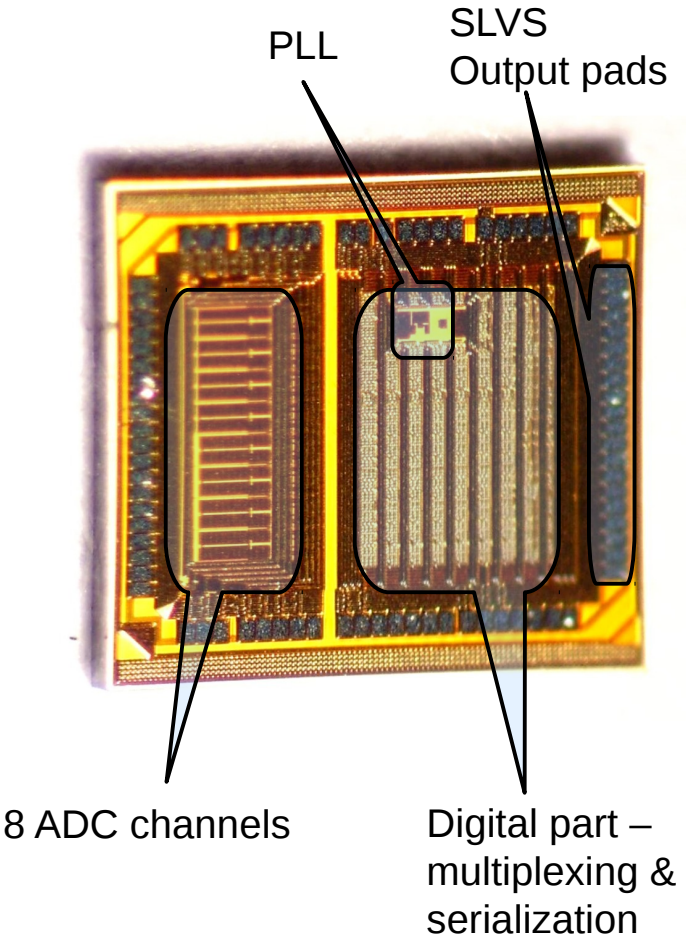




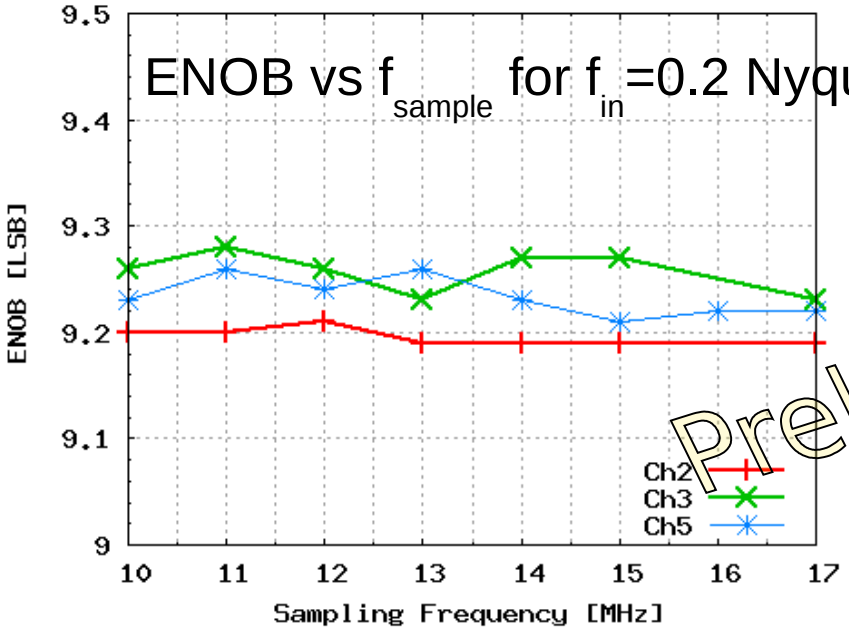
Multichannel readout ASIC
8 channel 10-bit digitizer - layout&prototype

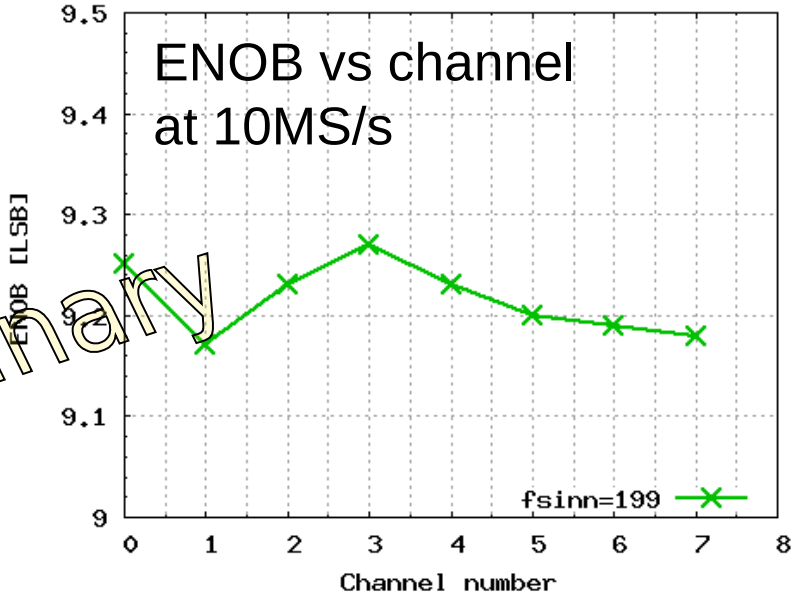


2200um x 2000um



Multichannel readout ASIC
First measurements of 8-channel 10-bit digitizer



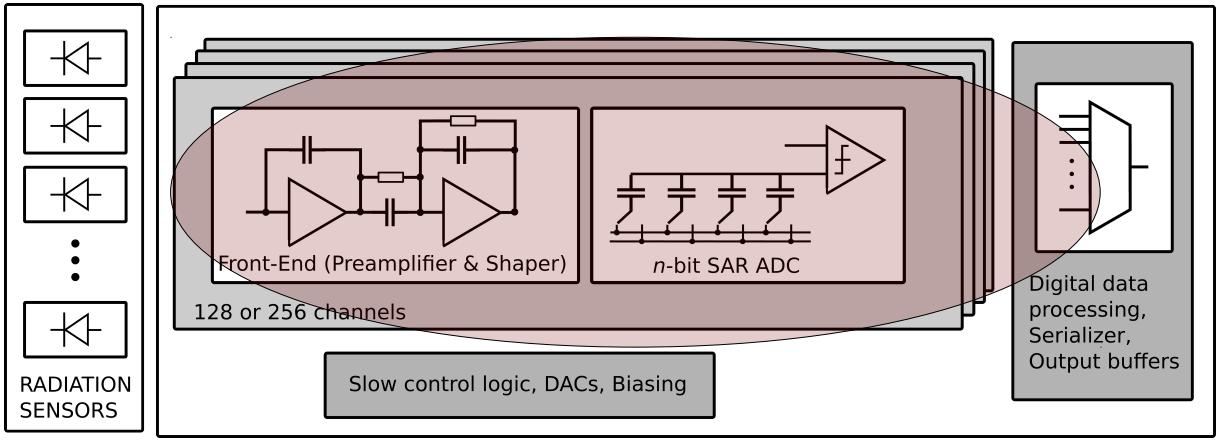


Preliminary

All 8 channels work well !

It is probably the first working very low power multichannel 10-bit ADC for particle physics detectors

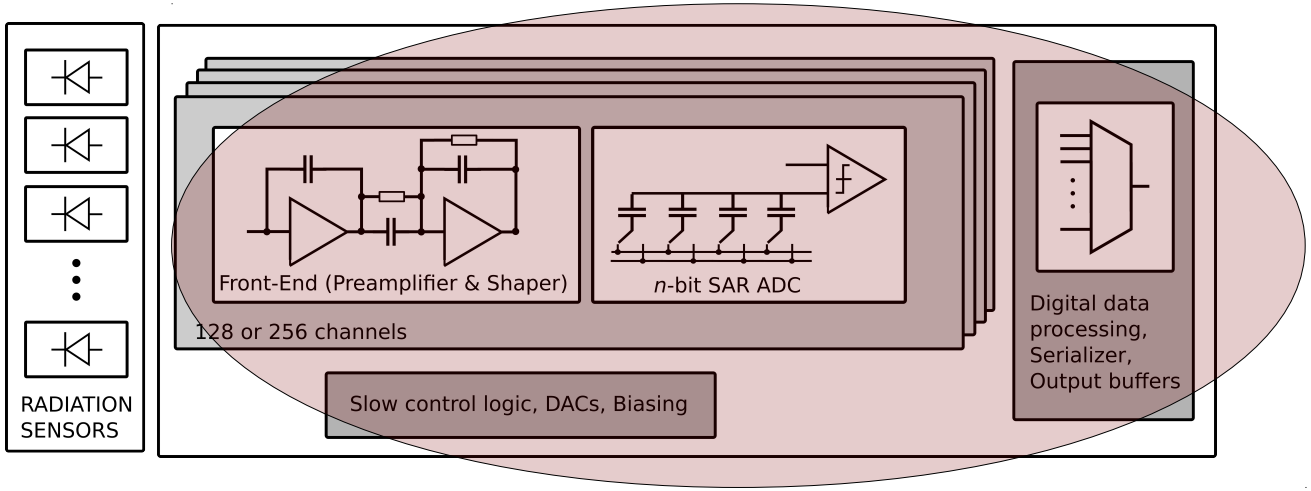
Status
Where we are now ?



In November 2015 we would like to submit the ASIC:

- 8-channels
- front-end and ADC in each channel,
- Serialization not yet complete
- Some DACs for automatic setting still missing

Plans – short term



In 2016 we would like to submit a prototype ASIC ready for compact LumiCal:

- 16-channels ???
- front-end and ADC in each channel,
- Serialization completed (1 data output per chip – few Gb/s)
- Everything (all DACs) for automatic settings comprised in the chip

Thank you for attention