Contents

1 Control Unit *(SLAC)*

The control unit makes the configuration and calibration of the CHESS2 ASIC possible. It also provides a convenient way to talk to the ASIC through a serial interface with hand-shake protocol called SACI (SLAC ASIC Control Interface).

The main circuital blocks that compose the control unit are:

- Command Logic: decodes and executes SACI system commands;
- SACI System: serial interface with hand-shake protocol;
- Global Register: rad-hard registers used to configure the ASIC;
- Row and Column Selection Register: used for single pixel, single row or single column selection.
- Data Bus Drivers: used for digital signals integrity.

In Figure 1 the control unit layout is shown and the block highlight is shown in Figure 2. A block diagram of the control unit is provided in the next section in Figure 4.

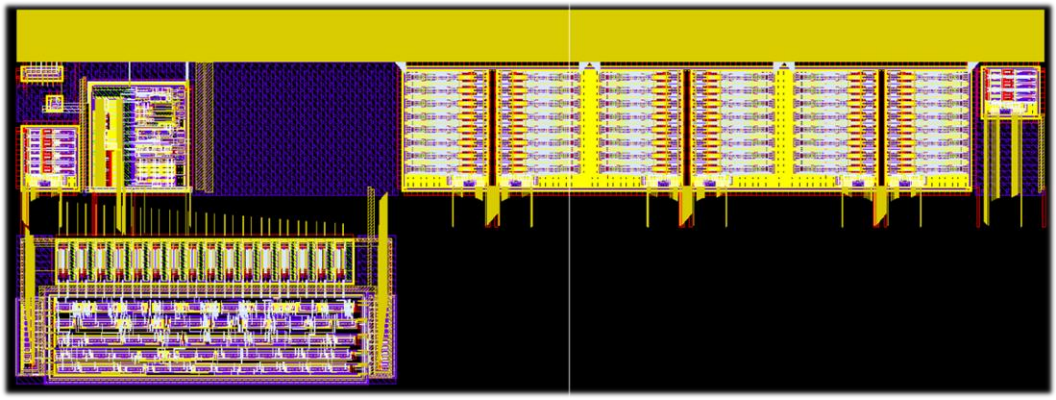


Figure 1. Control Unit Layout.

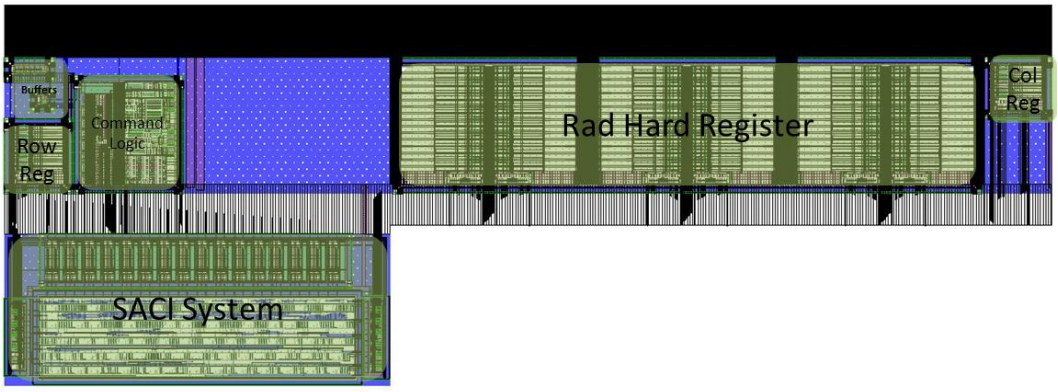


Figure 2. Control unit block highlight.

1.1 SACI System *(SLAC)*

The SACI system provides configurability to the entire ASIC. It directly interacts with all the configuration and calibration blocks providing a serial interface to the ASIC with hand-shake protocol. The two main parts that compose SACI are called SACI Core and SACI Buffer. The overall system layout is shown in Figure 3.

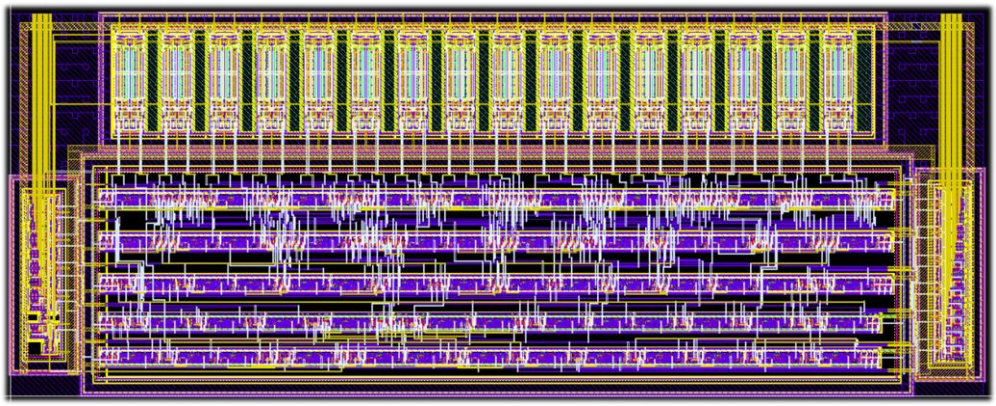


Figure 3. SACI System layout.

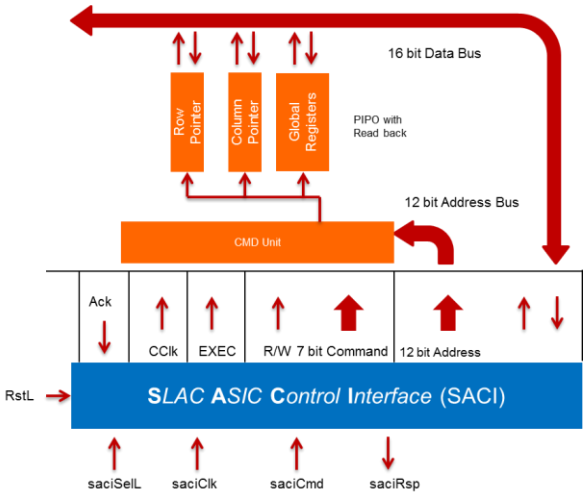


Figure 4. Control unit block diagram.

1.1.1 SACI Core *(SLAC)*

The SACI core has 6 digital input signals called **SACIclk**, **SACIcmd**, **SACIsel**, **SACIrsp**, **ack** and **reset**. The reset signal can be shared with the ASIC reset signal and SACIclk, SACIcmd and SACIrsp can be shared among several SACI in a system containing several ASICs (see Figure 5). Using this arrangement SACI requires only 4 I/O pads + 1 shared reset line.

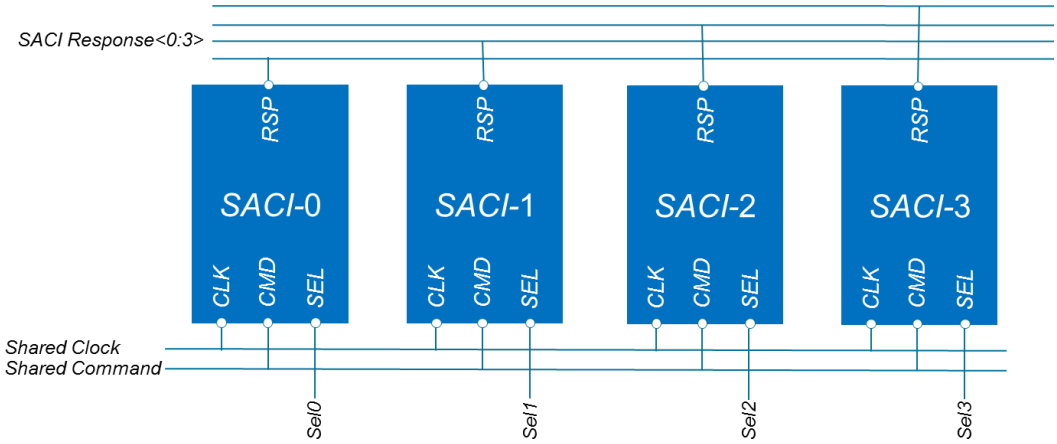


Figure 5. Multiple SACI connection

The acknowledgment signal (**ack**) is provided as input to SACI core from the control logic.

The SACI core output signals are:

- 52 bits word as shown in Figure 6 (set bit, notRead/Write bit, 7bits command, 12 bits address, 32bits data bus);
- 1 execute signal (**EXEC**);
- 1 clock signal (**CClk**);

Figure 6. SACI parallel output word bit definition.

When **EXEC** is HIGH the 52 bits word is ready at the output of SACI and the command logic starts to execute the command; when the command is executed the command logic sends the **ACK** signal to the SACI system that echos a replica of **SACIcmd** (rw + command + address) on the **SACIrsp** line.

1.1.2 SACI Buffer *(SLAC)*

The SACI system contains data bus, address and command re-buffering and conditioning. A brief description of these blocks is provided in the sections 1.1.2.1 and 1.1.2.2.

1.1.2.1 Data bus Buffer (SLAC)

SACI contains circuits that re-buffer and provide conditioning of the data bus. In particular these circuits guarantee that SACI is writing the data bus only in WRITE mode and it is reading the data bus in READ mode. Writing and reading of the data bus are permitted only when the **EXEC** signal is HIGH in order to save power. SACI is reading the data bus only when the **ACK** signal is HIGH in order to avoid buffer high current consumption when the bus is floating.

1.1.2.2 Address and Command Buffer (SLAC)

The address and command digital signals buffer chain provides a strong driven output signal and they are conditioned with the **EXEC** signal. In particular the address and command lines are written only when exec is on HIGH state in order to avoid charging and discharging of the address lines and save power.

1.2 Command Logic *(SLAC)*

The command logic shown in Figure 8 receives and executes the commands sent by SACI system in order to perform read/write operations on global registers (see section 1.3), row and column registers and the entire matrix. Decoding of the SACI system commands is done in the command decoder (see 1.2.1).

The principle of operation is the following: SACI system sends the command word and the command decoder decodes it and executes it when **EXEC** is high. An internal clock generation circuit allows the alignment of the command to the first **CCKclk** after **EXEC** by defining an internal **BUSY** signal. On the falling edge of **BUSY**, an **ACK** signal is sent to the SACI system.

The command logic generates a **CCKreg** clock signal for the global register configuration and read-back and the **CCKpix** clock signal for the matrix configuration.
The control unit provides all the signals required in order to address properly the matrix. It is possible to address single pixel, single row, single column or full Matrix (Figure 7).

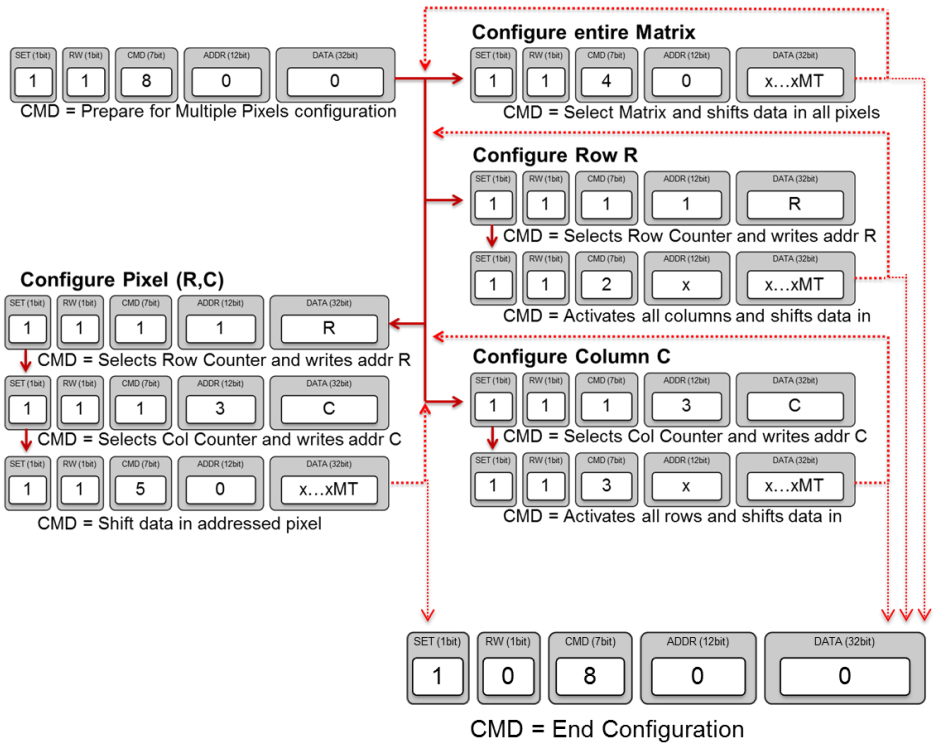


Figure 7. Matrix Configuration commands.

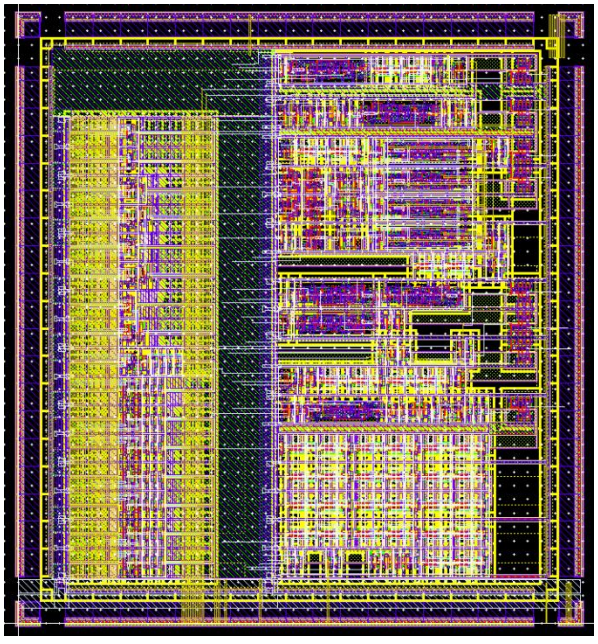


Figure 8. Command Logic layout.

1.2.1 Command Decoder *(SLAC)*

The command list is defined in Table 1 :

RW	CMD	ADDR	DATA	Function
0/1	1	Register Address	Data	Read/Write Global Register
1	4	0	Data	Write Matrix
0/1	5	0	Data	Read/Write Pixel
1	8	0	0	START Matrix Configuration
0	0	0	0	END Matrix Configuration
1	2	0	0	Write all Columns (used to configure a single row)
1	3	0	0	Write all Row (used to configure a single column)

Table 1. Control Unit list of commands.

Command decoder layout is shown in Figure 9.

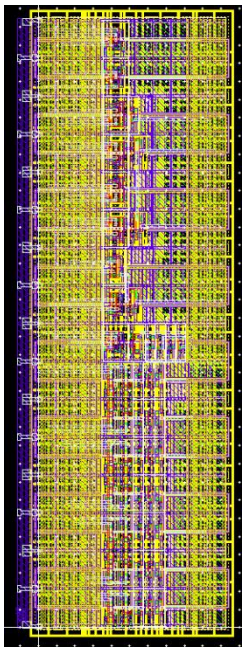


Figure 9. Command Decoder layout.

1.3 Registry (Rad Hard) *(SLAC)*

The registry store the ASIC configuration settings needed for the DACs (in order to bias pixel circuitry) and the control unit (to activate delays on the matrix configuration control signals in order to compensate for large matrix lines load). The configuration settings must be preserved to ensure the correct ASIC behavior in case of radiation exposure. For these reasons rad-hard registers are available in CHESS2 and in this document we will refer to them using the term *global registers*. These registers have a read-back feature. They share an external digital global reset signal (**GR**) with the SACI system, command logic, row and column pointers and set the initial condition to guarantee correct DACs and control unit settings. Radiation hardness design is achieved using nMOS with a gate-enclosed layout in the memory cells.

Registry is composed of six 16 bits rad-hard registers univocally identified by a 12 bits address with value from 5 to 10 and the registry map is shown in Table 2. It shares global reset, address and data bus lines with SACI. Each register contains a logic section to handle read/write phases and a bit section that stores the digital word. The command logic provides the digital signals required to operate the registers are (**CCKreg**) , the global reset (**GR**) and the read/write (**rw**).

		Address									
		1	2	3	4	5	6	7	8	9	10
BIT	0	Row Pointer	Not assigned	Column Pointer	Not assigned	DAC0 0	DAC2 0	DAC4 0	DAC6 0	Future Full Chip DACs configuration settings	DelEXEC 0
	1					DAC0 1	DAC2 1	DAC4 1	DAC6 1		DelCCKreg 1
	2					DAC0 2	DAC2 2	DAC4 2	DAC6 2		Future ControlUnit configuration settings
	3					DAC0 3	DAC2 3	DAC4 3	DAC6 3		
	4					DAC0 4	DAC2 4	DAC4 4	DAC6 4		
	5					DAC0 5	DAC2 5	DAC4 5	DAC6 5		
	6					DAC1 0	DAC3 0	DAC5 0	DAC7 0		
	7					DAC1 1	DAC3 1	DAC5 1	DAC7 1		
	8					DAC1 2	DAC3 2	DAC5 2	DAC7 2		
	9					DAC1 3	DAC3 3	DAC5 3	DAC7 3		
	10					DAC1 4	DAC3 4	DAC5 4	DAC7 4		
	11					DAC1 5	DAC3 5	DAC5 5	DAC7 5		
	12					Spare bits	Spare bits	Spare bits	Spare bits		
	13										
	14										
	15										

Table 2. Rad Hard Registry addresses.

The entire registry layout is shown in Figure 10.

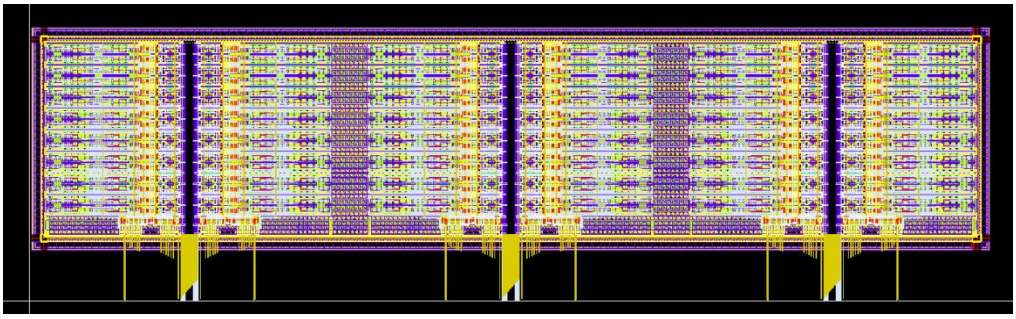


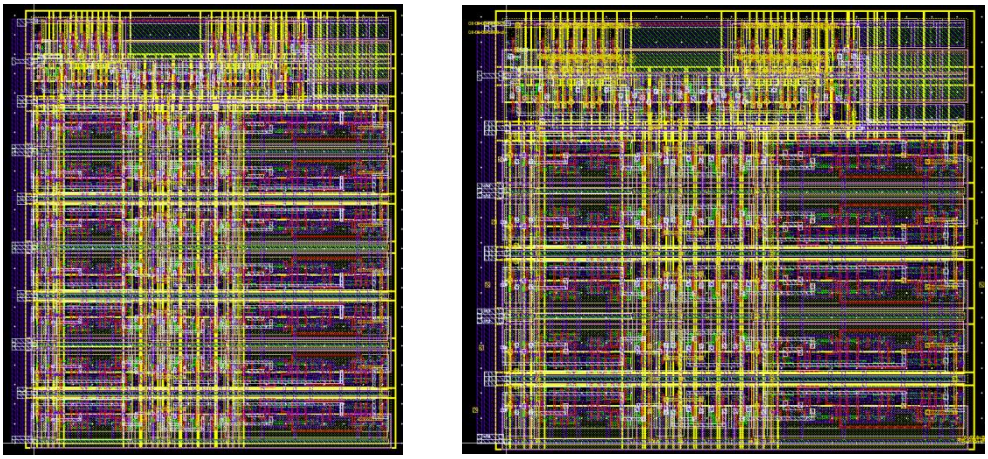
Figure 10. Rad Hard Registry layout.

1.4 Column and Row Selection Register *(SLAC)*

Read/write operations can be operated on a single pixel defined by a row and column. The selection is done by the row and column Registers which layout is shown in Figure 11.

The Matrix is composed of 128 rows and 32 columns, so it is necessary to use a 7-bit register to select the rows and a 5-bit register for the columns. Row and Columns Register outputs are sent to decoders (see section 2) to select the proper pixel.

The row and column registers are written and read-back using the same global register commands set.



(a) (b)

Figure 11. Selection registers: (a) Row; (b) Column.

2 Decoders *(SLAC)*

Configuration of single pixels, single rows or columns and the entire matrix is available in CHESS2. The selection is made converting the digital words coming from row and column selection registers using two decoders. Each pixel is univocally identified by row and column position and when it is selected it can be configured.

Single matrix rows /columns can be enabled by **allcol**/**allrow** signals coming from the control unit. If both the signals are set, both the decoders outputs are enabled and the entire matrix can be configured.

2.1 Rows *(SLAC)*

A synchronous 7-to-128 decoder allows matrix row selection according to the 7 bits word coming from the row selection register. Decoder output is latched on **CCKpix** clock signal sent by the control unit.

2.2 Columns *(SLAC)*

An asynchronous 5-to-32 decoder is used to convert the word coming from the column selection register and select the matrix columns. The outputs are used to mask the buffered data configuring the pixels.

3 LVDS-like Transmitter and Receiver *(SLAC)*

CHESS2 output data transmission consists of 13 LVDS-like transmitters that operate at a frequency of 320MHz. The number of LVDS transmitters has been chosen in order to match the word length and the transmitter operational speed is 40MHz x 8 where 8 is the number of hit that can be detected for each 25ns cycle. The 320MHz clock is fed in the ASIC through an LVDS receiver. A description of the transmitter and receiver blocks is provided in this section.

3.1 LVDS Transmitter *(SLAC)*

The LVDS transmitter is a circuit that provides a LVDS-like output given a CMOS level input. The LVDS outputs meet the standard LVDS signal level but the common mode and the output swing can be also configured (see Table 3).

Specs	Typical	Min	Max
Differential Output Voltage (@ R_{LOAD}=100Ω)	600mV		
Output Common Mode	1.2V	0.5	2.8
Current	3mA	0.2mA	3.5mA*
Speed	320MHz		500MHz
Supply	3.3V		

Table 3. LVDS Transmitter simulated characteristics.

3.2 LVDS Receiver

The LVDS receiver is a circuit that provides a CMOS level output given a LVDS-like input. The input signals can either match the standard LVDS or any of the adjustable level set from the CHESS2 LVDS transmitter.

4 Data bus distribution chain

The SACI data bus is buffered in order to preserve signal integrity and to provide a strong driven signal for the entire ASIC. As seen in 1.1.2 the data bus is buffered using a circuit able to handle the bi - directionality of the data bus avoiding multiple write at the same time. An additional buffer chain has been inserted to provide a strong driven signal to the matrix and to match the delay of the write pixel signal. The data bus distribution chain creates a tree of signal in which each end node drives a column.