CMOS Strip Project
1st year Status Report

V. Fadeyev, R. Nickerson, M. Stanitzki

For the CMOS Strip Collaboration:

A. Affolder[0], K.Arndt[1], R. Bates[2], A. Blue[2], D. Bortoletto[1], C. Buttar[2], P. Caragiulo[3], D. Das[4], J. Dopke[4], A. Dragone[3], F. Ehrler[5], V. Fadeyev[6], Z Galloway[6], H. Grabas[6], I. M. Gregor[7], P. Grenier[3], A. Grillo[6], L. B. A. Hommels[8], T. Huffman[1], J. John[1], K. Kanisauskas[1,2], C. Kenney[3], J. Kramberger[9], Z. Liang[6], I. Mandic[9], D. Maneuski[2], S. McMahon[1,4], M. Mikuz[9,10], D. Muenstermann[11], R. Nickerson[1], I. Peric[5], P. Phillips[1,4], R. Plackett[1], F. Rubbo[3], J. Segal[3], A. Seiden[6], I. Shipsey[1], M. Stanitzki[7], D. Su[3], C. Tamma[3], R. Turchetta[4], L. Vigani[1], J. Volk[6], R. Wang[12], M. Warren[13], F. Wilson[4], S. Worm[4], J. Zhang[12]

[12]Argonne National Laboratory, [8]Cambridge University, [7]Deutsches Elektronen-Synchrotron, [9]Jožef Stefan Institute, Ljubljana, [5]Karlsruhe Institute of Technology,[1]University of Oxford, [4]Rutherford Appleton Laboratory, [3]SLAC National Accelerator Laboratory, [2]SUPA - School of Physics and Astronomy, University of Glasgow, [11]Universite de Genève, [6]University of California Santa Cruz, Santa Cruz Institute for Particle Physics (SCIPP), [13]University College, London, [0]University of Liverpool, [10]University of Ljubljana.

1 Table of Contents

1 The CMOS Strip project within ATLAS

1.1 Introduction

This document describes the progress made since June 2014 in establishing a CMOS-based strip sensor as an alternative sensor for the ATLAS Phase-II Strip Tracker Upgrade. It gives an overview of the project and its rationale and then addresses the impact of such a sensor on the overall detector mechanics and electronics. The current understanding of the technology is given together with the upcoming plans for the next year. It concludes with an outlook about the future of this technology for the strip region of the Inner Tracker (ITk) in ATLAS.

1.1.1 The Phase-II Upgrade strip tracker layout

For the Phase-II Upgrade of the ATLAS detector scheduled to be completed in 2022, it is planned to replace the current tracker with an all-silicon detector using both pixels and strip sensors. The current layout as described in the Letter-of-Intent (LoI) (1) consists of a barrel with four hybrid-pixel layers and five strip layers (including a stub) and two endcaps consisting of six hybrid-pixel disk and seven strip disks each. Each layer uses small-angle stereo sensors with a pitch of 75 µm on each side. The total area of this tracker is estimated to be 201 m^2, of which over 95% belongs to the strip tracker. The current layout is shown in Figure 1 and has been adopted as the baseline design for the upcoming studies.

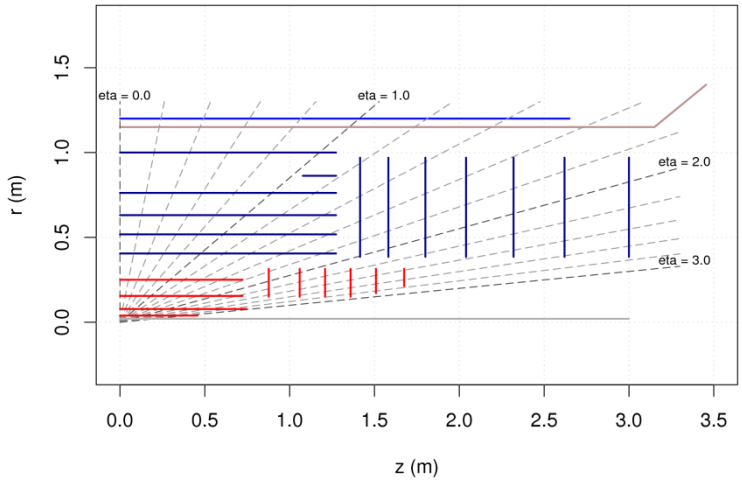

Figure 1: The current baseline Tracker layout for the ATLAS Phase-II Upgrade

The strip tracker uses staves and petals (see Figure 2) as central building blocks compared to the present module-based ATLAS SCT. A stave consists of a carbon-fibre core with thirteen identical modules mounted on each side. A barrel module has a silicon sensor with 10x10 cm dimensions and a strip length of 2.5 cm with a strip pitch of 75 µm. Each module has two hybrids with ten ABC130 readout ASICS each. Altogether a module has 5120 channels. All the data, commands and the power are centrally routed through the End-of-Substructure (EoS) card. For the endcaps, a similar scheme has been proposed, however the wedge-shaped petals have nine differently shaped modules on each side. The data/commands are routed to the DAQ using High-Speed radiation-hard optical links and high-speed multiplexers – the so-called GBTs – which are envisaged to provide bandwidth up to 9.6 GBit/s. Low-Voltage is distributed using DC-DC converters for each module, while for the sensor high-voltage a HV-

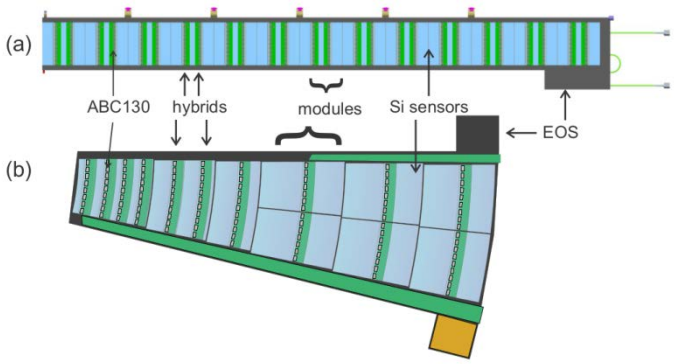

Figure 2: Staves (a) and Petals (b) as building blocks of the baseline design.

Multiplexing scheme is foreseen.

ATLAS is currently re-vising its baseline design for the upcoming Technical Design Report (TDR) which is scheduled to be finalized in September 2016. It is expected that some parameters may get adjusted. However, the key features and the overall design are very likely to stay.

1.1.2 Monolithic active pixel sensors

Monolithic active pixel sensors (MAPS) have been developed since the early '90s as imaging sensors and have currently replaced CCD sensors in most applications. Very early on, their potential as a particle detector was realised and the first MAPS for particle physics appeared shortly thereafter. The last two decades have seen tremendous progress in the development of MAPS both for particle physics as well as adjacent fields such as heavy-ion physics and synchrotron-light applications. The basic MAPS cell was based on a 3-Transistor (3T) structure diode using NMOS transistors only, the charge being collected with a readout diode using charge diffusion. There were two basic limitations to this approach. The n-well of the PMOS acted as a parasitic charge collection unit, which prevented the full use of CMOS functionality and the devices were inherently slow due to the charge collection mechanism being diffusion. The introduction of deep implants allowed the use of full CMOS functionality, while the use of high-resistivity epitaxial layers (HR-CMOS) or the use of a special HV-CMOS process allowed collecting the charge much faster thanks to presence of a drift field. Both of these processes are potentially very radiation-hard, making them suitable to be used for the HL-LHC (10^{15}-10^{16} neq/cm^2).

1.2 Advantages compared to the baseline solution

A CMOS-based sensor offers several attractive benefits compared to the baseline solution, which is based on a planar strip sensor. These benefits can be split in three categories: reduction of material, improved resolution and reduced cost. For the following discussion, the model is a StripCMOS sensor with a pitch of 40 µm and a 2.3 cm strip length, which is composed of 720 µm length individual pixels chained together to form a strip with digital z-encoding (see 1.3.1).

In the baseline solution, there is a need to have silicon sensors on both sides of the stave/petal, to provide the necessary z resolution using a small-angle-stereo configuration. The CMOS solution eliminates the need for the small-angle stereo configuration as the pixels already provide full 3D-Hits. Coupled with thinning, this leads to a reduction of the material from 1.8% to 1%. The finer strip pitch and the use of pixels internal to the strip improve the resolution by a factor of two in r-ϕ and provide a precise point in z as well. Finally the reduction in cost and associated assembly time is significant. The total silicon area is reduced by a factor of two, which is estimated to save on the order of 30 MCHF in core cost.

Parameter	Planar Sensor	StripCMOS Sensor
r-ϕ resolution	20 µm – 23 µm	11 µm
z-resolution	850 µm	280 µm
Two hit resolution in r-ϕ	160 µm-240 µm	80 µm
z-element length	2.5 cm	720 µm (2.4 cm / strip)
Fraction of two hit clusters	15% - 20%	2%-3%
Geometry inefficiency on stave	~0.7%	~1%
Radiation Lengths per stave	1.8%	1%
Insensitive crossings after a hit	1 BC	0.3 BC (1/32 of strip is dead for 10 bunch crossings)
Number of Signal Wire bonds	O(5100)	O(1100)

Table 1 Comparison between the baseline and StripCMOS solution for the ITk Phase-II Strip Tracker Upgrade

There is a potential additional cost-saving benefit by switching from a highly specialised process for the planar sensors to a mainstream high-volume CMOS process, which has not been fully quantified yet. Having a factor of five less wire bonds has a significant impact on the assembly time and the associated on-costs. A summary of the potential benefits is given in Table 1.

1.3 The StripCMOS programme

At the ATLAS Upgrade Week in 2014, it was decided that ATLAS will investigate the use of CMOS sensors for the Phase-II Strip Tracker Upgrade and a three-year programme with well-defined break points after each year will start in June 2014 to lead this investigation. It is an aggressive time-driven development programme, which given the time-constraints is not optimised to fully exploit the possibilities of CMOS, but rather to attempt to secure the benefits mentioned above for the Phase-II Tracker Upgrade. A part of the charge was that this programme will not distract resources from the baseline solution so that the TDR can be delivered on time. Part of the mandate was to have an annual review to review the progress of the programme and to decide on its continuation. It should be noted that the collaboration which has formed to undertake this task is not a purely ATLAS group, since it includes many participants from outside the Collaboration.

1.3.1 Basic StripCMOS architecture

Given the time-constraints dictated by the completion date of the ATLAS TDR and the available resources, it was decided very early on to investigate a solution which would replace the sensor itself and would require some modifications of the readout ASIC, but would keep everything else beyond almost exactly the same as in the baseline solution, therefore minimising the impact on the overall effort. It is obvious that this solution is not taking full advantage of all the benefits that a CMOS solution could offer, but it is the only viable solution given the time-scales and the available resources. Therefore solutions which eliminate the need for a readout ASIC by embedding all the digital logic in the sensor were not pursued. This decision was taken after a careful examination of the possibilities.

The architecture adopted employs a digital z-encoded design with a basic pixel width of 40 µm and a length of 720 µm. The choice for the digital variant was made as it was considered to be easier to implement and less of a risk than an analogue form of z-encoding. The pixels forming a virtual strip are then connected to the Encoder block at the end of the sensor with individual traces. Each pixel has its own comparator and the z information – effectively the pixel ID – is encoded into the digital data stream in the Encoder block (See Figure 3).

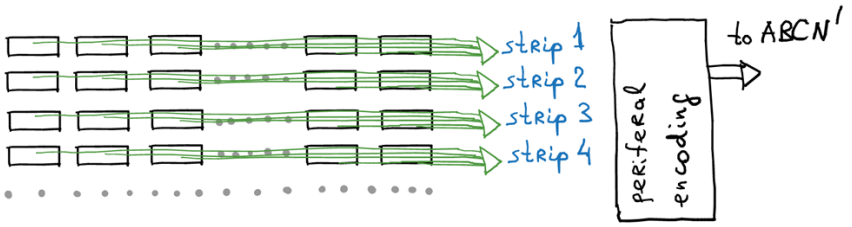

Figure 3 Sketch of the digital z-encoded design

The Encoder block at the periphery of the chip is then connected to a modified version of the ABC130 readout ASIC, which is called ABCN'. This chip has effectively the analogue front-end removed and replaced with a digital block which communicates with the sensor. The digital back-end is slightly modified (to handle the z-encoded data coming from the Encoder block) and interfaced to the HCC (Hybrid Control Chip) chip. The total size of the CMOS sensor chip is planned to take advantage of the maximum available reticule size, which is in the order of 2 cm x 2.5 cm. For reasons of effort and potential yield, there is no stitching solution being pursued at the moment, which would allow overcoming the size limitations of any CMOS process.

1.3.2 Selection of the investigated CMOS processes

The CMOS Strip programme decided early on to minimise the number of processes to be studied to two. The following processes were considered the leading candidates:

- AMS HV-350
- GlobalFoundries 130 HV
- LFoundry 180 HR
- TowerJazz 180 HR-CMOS
- Espros Photonics AG (EPC) 150 HR.

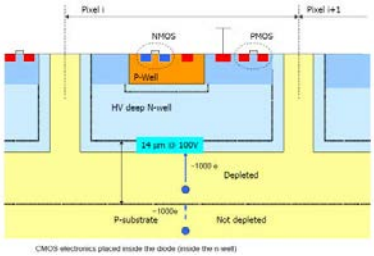

Figure 4 AMS 350 HV CMOS

It was decided to select one HV and one HR CMOS process in order to have two distinct approaches. This allows exploration of the major process options whilst restricted by the time-scales and the effort available.

For the HV-CMOS, the AMS HV-350 process was selected because of the large amount of positive experience with this process already within the community and because of ease of access. The AMS HV350 technology is a variation of a standard CMOS process that is frequently used for power devices. It allows for higher-resistivity substrates and design rules for either 60V or 120 V bias voltages. A pixel in AMS HV-350 technology is shown in Figure 4.

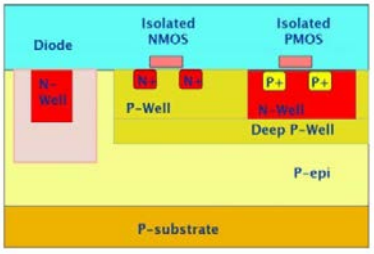

Figure 5 TowerJazz 180 HR-CMOS

For the HR-CMOS the TowerJazz 180 HR-CMOS process was selected because of good connections with the company and past experience. ALICE is using this process for their MAPS. This process offers thin epitaxial layers (< 25 µm) consisting of high resistivity material. It also allows using the full CMOS capabilities due the availability of deep p-implants. A pixel in TowerJazz 180 HR-CMOS is shown in Figure 5.

1.3.3 The three year programme

As already mentioned above, the StripCMOS programme has been given three years to investigate the use of CMOS. It formally started in June of 2014, co-lead by V. Fadeyev (UCSC), R. Nickerson (Oxford) and M. Stanitzki (DESY). Below the goals and milestones for each year are summarised.

1.3.3.1 Year 1: Characterization of basic sensor/electronics properties and Architecture

The goal of the first year is to establish the feasibility of using CMOS for the Phase-II Strip Tracker Upgrade. Two decisions were made in advance, the selection of AMS and TowerJazz as the target foundries and the decision to pursue a digital z-encoded design. In terms of the Pixel development, the primary goal was to characterize the pixel itself, especially its radiation hardness. The peripheral electronics need to be specified and a common readout system for testing needs to be selected.

Furthermore, the impact on the physics is to be evaluated and the integration in the baseline design needs to be studied. Together with the foundries, the viability of stitching, cut lines, stitching and multi-reticule possibilities need to be evaluated.

1.3.3.2 Year 2: Fabricating and evaluating a large-scale device.

The main goal of year two is to manufacture a large scale sensor with close to full functionality, to evaluate its radiation hardness and to characterize the pixels in terms of hit efficiency, charge collection speed and to measure to signal-to-noise ratio. The peripheral electronics architecture needs to be tested and its performance must meet the goals.

For the mechanics, all potential substantive changes required need to be evaluated and test parts will be fabricated for any essential new elements. Potential changes to the services need to be studied and bus tapes to be redesigned to accommodate new module configurations. The last item is the ABCN', which needs to be designed, fabricated and tested and a first hybrid design needs to be available at the end of year two.

1.3.3.3 Year 3: Full prototypes of sensors and ABCN'.

The ABCN' needs to be available in significant quantities and tested with sensor prototypes from year two. A full scale sensors needs to be designed, fabricated and characterised and both sensor and ABCN' need to be operated in a module-like configuration. As a second step, have more than one of these modules operating on a bus tape. Changes to accommodate new layout and stave/petal need to be designed and assembly protocols and series production planning have been considered.

1.3.4 The StripCMOS collaboration

While the programme started from within ATLAS, there are a significant number of key people, who are not members of the ATLAS collaboration, but nevertheless still have a strong interest in the success of this project and who are contributing a lot to the effort. Therefore the StripCMOS "collaboration" has formed to ensure credit is appropriately assigned and to avoid the obvious complications of any other arrangement. Currently there are 49 authors from thirteen institutes participating in the StripCMOS collaboration.

2 Resources

For the three-year programme the Collaboration will make use of existing infrastructure and effort in the participating groups as well as having limited additional resources, which are coming partially from existing grants or additional funding from labs. The major fraction of the funding to date has gone into the fabrication costs of the chips (Details see Section 2.1) and a significantly smaller fraction in production of the associated testing PCB's.

2.1 Submission Costs

Currently we have submitted HVstrip1 and the two CHESS1 Chips with an overall investment of ≈90 kEUR. For the submission of the CHESS2-AMS Chip we have already secured the necessary funding of 100 kEUR. Overall the total investment for submissions was 190 kEUR.

3 Impact on detector mechanics and electronics

It is recognized that the schedule does not permit a complete redesign of the mechanics to optimise for the use of CMOS sensors. Considerable compromise is envisioned in order to facilitate re-use of the bulk of the work already done for the mechanical systems. The layout does not change from that proposed for conventional strips in the sense that the planes remain in the same place: the principle alteration is from two planes of stereo to one of pixelated strips. It is argued that by design the geometry is so similar, that to a significant degree the barrel region can use the same mechanics as the LoI layout, the same services concept, with only moderate changes required. In the forward region the situation is more complex as wedged sensors are not envisioned for the CMOS option. Whilst an outline early concept for an implementation for the forward region is sketched here, it remains a major task for the second year of the programme to understand in detail how the forward region can work with rectangular detectors. One possibility is to construct the endcap disks out of "blades" (similar to staves) instead of petals. For the forward region there are significant mechanical simplifications as well as complications, so this is anticipated as being a tractable problem, but it is

acknowledged that this is a significant change and that the effort required to fully understand the ramifications is not negligible.

The goal for the first year of the programme on the mechanical side was ' basic study of mechanical implications'. This is reported here.

3.1 Barrel Region

3.1.1 Barrel StripCMOS module

The barrel StripCMOS module is shown in the figure below, it consists of four silicon sensor elements, bonded to a single hybrid, which has the ABCN' read-out chips, an HCC and a DC-DC convertor. The hybrid is a flex-rigid and acts both as the electrical hybrid and the mechanical stiffener for the module. Each of the four sensor modules consists of five independent reticules each with an independent CMOS sensor. Each ABCN' services two such reticules, a total of ten ABCN' per hybrid. The number of wire bonds is vastly reduced compared with the planar detectors as (synchronous) data sparsification happens in the periphery of the sensor reticules. The sensors are directly mounted on the staves, so the good heat transfer properties with the planar design are retained.

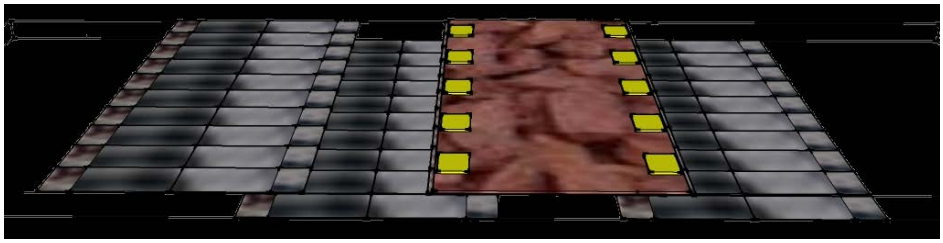

Figure 6 Four modules on a stave, three showing reticule layout above and below the stave (which is invisible) and one showing the hybrid with ABCN' read-out ASICs

Each strip is 2.3[1]cm long and the strips are on a 40 μm pitch. A strip is divided into 32 elements, providing z information for a hit.

The performance of the LoI layout using CMOS sensors has not been simulated, but some estimates of the likely performance can be made from scaling arguments and earlier work on CMOS sensor response to tracks. Some simulation work has been done to understand occupancies. Table 1 gives estimates of the comparison between CMOS and planar for the barrel region. Several assumptions are made regarding geometric efficiency, not enumerated here. An example is that it is easier to eliminate the gap at z = 0 for CMOS sensors in the barrel region, but there are more z gaps between sensors for the CMOS case. With a different geometry of CMOS module these could be reduced to zero, but the number of modules would double and this seems a high price.

3.1.2 StripCMOS Barrel Stave

The modules are alternately tiled on opposite sides of the stave (see Figure 6), with the module at z=0 protruding beyond the end of the stave. This arrangement is similar to the planar detector, but considerably simplified and allows actual overlap of sensitive regions at z=0. This also allows the contraction of the stave to be allowed for in the centre of the stave which could be exploited to simplify the end of stave region (but doesn't need to be). Mechanically the stave core is almost identical to the planar design, with the major change being to the service tape on the surface. These would be no more complex than the existing design, but would be different. The bulk of the effort on the existing tapes has been to understand radiation hardness, manufacturing methodology, size stability etc. Changing the actual layout is a significant but not a long task. It would also mandate reprogramming the tape testing robot.

[1] This number will depend on the final sensor design and will affect the number of modules per stave and the dead space fraction. It will not affect the concepts.

Twenty-eight modules are attached to a stave. The total power consumption is comparable to the baseline planar stave; the total data rate is reduced as the z information does not require two separate hits to be encoded, but only a few extra bits on a single hit. The DC-DC convertor in this model would be redesigned to provide power for just one module. The ongoing HCC design is being done with possible use with a CMOS data structure in mind. It is anticipated that the module mounting robot could be reprogramed and with a new set of jigs used to mount CMOS modules just as easily as planar.

Whilst the heat dissipation remains relatively symmetric on either side of the stave it is not identical to the planar design, so some simulation and measurement work will be needed to verify that the stave does not change behaviour with the alternate module layout. Some additional work on redesign of the end of stave services may be needed as it is not yet certain all the services will remain identical. They should however be extremely similar so this should not be a major task. In fact the total data rates should be reduced (two binary hits are replaced with one with z address), so if anything the services might simplify.

3.1.3 Geometric Inefficiency and Pattern Recognition

This issue applies equally to barrel and forward strip regions and is not repeated in the sections relating to the forward region.

The number of planes required to ensure a high efficiency tracking and low ghosting is complex to evaluate as, in part, it depends strongly on the algorithmic methods employed. The CMOS option described replaces ten planes of single sided detector with five of pixelated layers, which could adversely affect many algorithms. However the required number of planes depends not only on the number and efficiency of individual planes, but also on the quality of information the planes are providing. The strip CMOS option improves the r-ϕ resolution by almost a factor of two, the z-resolution by a factor of five, and the two hit resolution by a factor of two to three in r-ϕ . This is close to being a pixel detector in terms of segmentation with a strip-like read-out: it is possible that with appropriate algorithms and including the pixel layers, that the five planes of strip CMOS would provide better pattern recognition than ten of planar silicon strip sensors. This contention is supported by the recent layout study which showed a 25% reduction in the fake rate with the addition of a fifth pixel layer as a replacement for two planar. The planar area ambiguity in (r-ϕ) -z associated with a hit is reduced by a factor of six and there is also a smaller but also large improvement in the two hit resolution. Whilst not currently planned, it would be possible with StripCMOS to provide two hit resolution in z of 1.4 mm, i.e. multiple hits from within a single strip.

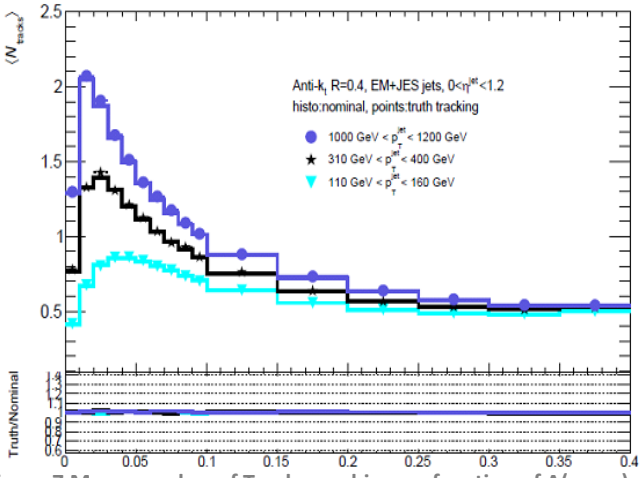

Figure 7 Mean number of Tracks per bin as a function of $\Delta(_{RTrk,Jet})$, the distance between the track and the Jet for bins in P_T^{Jet} of NT and TT tracking. Jets are reconstructed with the anti-k_t(R=0.4) algorithm and calibrated using the EM+JES calibration scheme.

Figure 7 (from (2)) shows the mean number of tracks as a function of angular displacement from the centre of a hadronic jet. At the radius of the strip tracker the first bin in this plot represents a physical separation of about 3 mm between tracks. This is a 75 CMOS strips wide distance, about 35 resolvable separate (r-ϕ) regions with a mean number of hits of 1.3 for a 1 TeV jet. Magnetic bend will improve things

further. With 20 k background hits from the uninteresting events in a beam crossing this gives 0.4 background hits in the same 75 strip region. It is reasonable to anticipate that a detailed study will prove favourable in terms of pattern recognition even with a reduced number of planes when the two track resolution and improved resolution is fully exploited.

In the forward region the basic layout is unaltered from the planar design; as with the barrel region the support mechanics and services concept is also essentially unaltered. The sensors are tiled onto similar petals as would be used for planar sensors.

There is one major change in the forward region compared with planar. Because it is not practical to design wedge shaped sensors in CMOS, a non-pointing geometry is adopted. The basic sensor is identical to that for the barrel region, but the wafers are cut into different sizes of reticule blocks. Effectively modules of different shapes are built based on 2.3 cm x 1 cm tiles. The use of non-pointing geometry is being considered even in the case of planar sensors, the pattern recognition uses space points, which are provided with better precision by CMOS sensors, so there is no fundamental problem with this approach.

3.1.4 Forward StripCMOS module

The forward modules are built from two strips of 2.3 cm tall reticule blocks. The size of these is determined by their position on the petal. The barrel module is a particular case of the forward module design, unifying the forward and barrel efforts with concomitant efficiency gains expected. The figure shows an example of a module construction, which is described in the barrel section. Also shown is how these modules build up a wedge shaped coverage. The stepped edges result in extra silicon being required compared with a wedge shaped tiling, but this is ameliorated to an extent because the overlaps between rear and front planar sensors are eliminated.

3.1.5 StripCMOS Petal

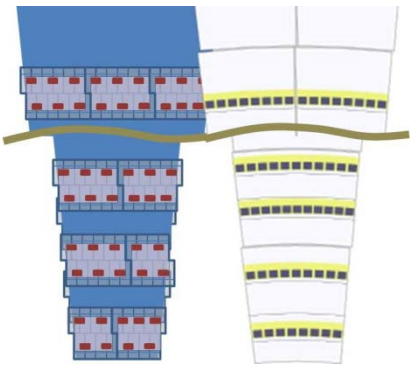

Figure 8 A CMOS Petal (left) and the baseline Petal (right)

There are eighteen rows of modules on each petal, which are alternately tiled on opposite sides of the stave to reduce geometric inefficiencies. Within each row there are up to three different module types, the difference between them being the number of sensor reticules and correspondingly the number of ABCN' ASICs.

This arrangement is similar to the planar detector, but considerably simplified as there are large gaps between sensors on each side. These gaps can be used to mount the HV switches and possibly the DC-DC convertors, though it is proposed to put those on the modules. It would also be possible to simplify the EoS region by exploiting available space between the last two rows of modules.

Whilst the gaps between modules can simplify mechanical aspects of the design; there is increased overlap between adjacent petals due to the edges of sensors being non-radial. This increase has not been precisely quantified, but it is expected to be small, at the level of few percent of the total area.

3.2 Feast II and HCC, electrical systems

The DC-DC convertor will need to be redesigned for the CMOS application, however the FEAST2 chip is designed to provide voltages above 1.2 V and currents up to 4 A. This matches the CMOS

configuration. The opinion of the design engineers is that the redesign is a question of physical layout, not a major redesign of the system.

The HCC will need to be different for the CMOS solution because the data streams include z information in the hits. However the current redesign of the HCC is being done with this in mind, so that the HCC will either be already compatible with the CMOS solution, or will need well controlled modification.

The HV multiplexing system will be relatively unaffected, except that a wider range of switches will be available at the lower voltages. This could be exploited, but does not need to be. Some change will be necessary to accommodate different numbers of modules, but again this is not felt to be a major issue by the engineers.

The service tapes redesign is regarded as a matter of weeks, also straight forward, the bulk of the effort in developing these are to do with understanding process, not the detailed layout.

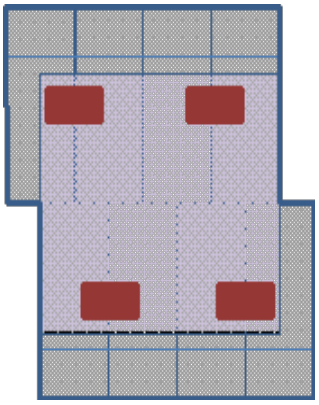

Figure 9 Example of a CMOS Forward Module in the 4-4 configuration. Two rows of four un-separated reticules offset by half a reticule; each Hybrid has four ABCN' chips.

Overall the largest time needed for the change of services and electronics will be in the re-testing time of modules, full electrical staves and petals. This cannot be accomplished in the same manner as the current generation because of time limitations; however with the full weight of the ATLAS collaboration behind this effort, it should be feasible to do the necessary testing on the requisite time scale.

4 Programme status

Using the first three chip submissions, we have obtained a diverse set of results regarding the technology performance. Key components of monolithic pixels have been assessed after different kinds of radiation. We have learned several aspects of charge collection, amplifier, and transistor performance. So far we have not seen any significant show stoppers. But the new knowledge is essential for choosing working options for the large scale device submission.

4.1 Requirements for a final StripCMOS Chip

One of the first year tasks was to compile a table of requirements for a final StripCMOS chip, which could be candidate for the ATLAS Phase-II Strip Tracker Upgrade. A compilation of these requirements is given below:

4.1.1 Strip Pitch

The goal was to provide a comparable r-ϕ resolution to the baseline solution. When charge sharing is accounted for the baseline detector achieves 20-23 μm depending on the angle of incidence. 20 μm is taken as the requirement. Given the technical possibilities, a strip pitch of 40 μm was chosen, with a projected r-ϕ resolution of 11μm assuming no charge sharing.

4.1.2 Power Consumption

The system power consumption must be <0.7 W/cm^2 which is translated into <0.5mW/cm^2 for the sensor and 0.2W/cm^2 for the ASICs. This limit comes from assuming a maximum cooling power of 1kW/stave in the barrel region and a similar power density in the forward. This is consistent with the current stave design, though the highest test was performed at 600W in a 1.2m stave. For note there is no issue with thermal runaway so the existing stave design is well suited to the use of thermal sensors with no modifications.

4.1.3 Z resolution

The goal was to provide a comparable r-z resolution to the baseline solution, which uses small angle stereo to achieve 850mm in z (or R in the forward region). The current design utilised a pixel length of 720μm providing a z resolution of 280 μm.

4.1.4 Radiation hardness

The location of the innermost barrel layer and endcap disk ring drives the requirements for the radiation hardness. For the HL-LHC we expect an integrated luminosity of 3000 fb^{-1} at the end of running in 2035.. From simulations performed using the FLUKA package (taken from (1)) it has been shown that is $2x10^{15}$ neq/cm^2 is a conservative upper limit (Figure 10). Most sections of the strip tracker receive significantly less dose. The dose requirement of photons is to withstand 60 Mrad.

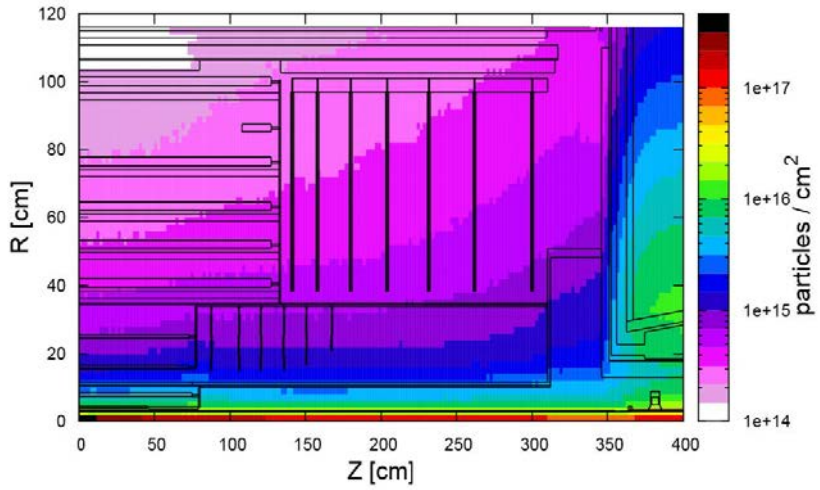

Figure 10 Particle Flux in the ATLAS ITk baseline design at the end of the HL-LHC 3000 fb^{-1}

4.1.5 Sensor Thickness

The requirement is that the sensor be no thicker than in the baseline solution, which is 300 μm. The technologically possible thickness for the AMS-HV-CMOS can be of the order of 100 μm driven by the depletion depth, and for the HR-CMOS much smaller as the epi layer is thin, and more of the order of 30 μm. a goal, but not a requirement is to provide a sensor thinned to <100 μm.

4.1.6 Signal-to-noise in a pixel & Noise Occupancy

Within a single pixel the required signal-to-noise ratio is at least eight to one after irradiation of the sensor. In addition the noise hit rate, after irradiation, in a strip must be less than 10^{-3} per bunch crossing. The former ensures high efficiency and low noise the latter is a restriction on coherent effects. The figure of 10^{-3} is chosen as significantly less than the pile up background real hit rate at the inner radius of the strip tracker.

4.1.7 Detection Efficiency

The efficiency of hit detection in the active area of the sensor must be >99%. This requirement will evolve as the pattern recognition with CMOS strip sensors is understood better.

4.1.8 Data format

As it is planned to re-use the digital back-end of the ABN130 in the ABCN', the data packet format from the modules must be unchanged, however the binary hit payload must include an extra six bits to encode the additional z information.

4.1.9 Sensor Size

The goal is to construct physical modules of comparable size than the planar design so that only the module construction phase of the project need be significantly different. To accomplish this the sensor element must be large and this is taken to mean that a sensor should be a full reticule in the process selected. This should be 4 cm^2 or larger.

4.1.10 Dicing Streets

To further help with production of large modules, it is planned that reticules may not be separated on the wafer, so the dicing street should be <100 µm to ensure small dead regions.

4.1.11 Active Area

The distance from the active area to the edge of the sensor should be <250 µm. This ensures that the geometrical efficiency of the StripCMOS sensor layout is comparable to that for the planar.

4.1.12 Dead time

Individual pixels must be able to detect two hits separated by 10 buckets (250ns). In addition when one pixel is dead, it must not prevent other pixels in the strip being read-out in subsequent buckets. A hit results therefore in 1/32 of a strip being insensitive for 10 bunch crossings. The dead time from this at strip occupancy of 1% is 0.3% compared with 1% for the planar design.

4.1.13 Permissible hit density

The number of hits which can be read-out in a 32 contiguous strip region must be ≥.8 Based on simulations done at SCIPP and work reported by Jansky (2) this ensures the efficiency of reading out hits in a high energy jet core to be very close to 100 %.

4.1.14 Time resolution

It is necessary to uniquely identify the bunch crossing that a hit belongs to. This requirement will evolve to more detailed requirements on amplifier and other element jitter.

Further more detailed requirements will be developed as this project advances, for example the required planarity of sensors will depend on a more detailed understanding of module construction.

4.2 The HVStrip1 Chip

This chip was designed by I. Peric (KIT) to start investigations relevant for strip CMOS project (Figure 11). It was implemented in AMS-HV350 0.35 µm technology. The chip contains a 22x2 array of pixels with size of 40x400 μm^2. They are active pixels with amplifiers, shapers, discriminators and a digital readout scheme. Some of the pixels have amplifiers made with standard linear transistors in the feedback, and others use circular layout. There are also pixel test structures with analogue readout. Three MOSFET structures (NMOS-linear, NMOS-enclosed and PMOS-linear) with drain connections are included as well.

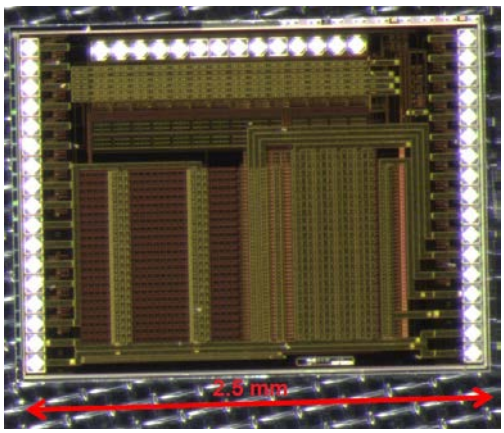

Figure 11 Picture of HVStripV1 chip.

4.3 CHESS1 Chip submissions

The main purpose of CHESS1 submission is to study the properties of the sensing diodes and readout amplifiers, as well as their evolution with radiation dose. To that effect, several different types of test structures were implemented on each of the CHESS-1 chips (see Figure 11):

- Passive pixel arrays to study the evolution of signal with increasing fluence
- Stand-alone amplifiers to study their performance as a function of ionizing dose

- Active pixel arrays which have the amplifiers connected to the collecting diodes. They are implemented inside the pixel layout.

- Transistor arrays for studying their detailed properties before and after irradiation.

4.3.1 AMS-HV35 CHESS-1

The CHESS-1-AMS chip has been designed by H. Grabas (UCSC) in consultation with I. Peric (KIT) (Figure 12). The chip was implemented in AMS 0.35 μm technology. It was the same technology node as HVStripV1 chip. Same strategy of implementing amplifiers inside the collecting n-well was followed. Design rules for 120 V bias were used. The array structures on the chip used varying length between 100 μm and 800 μm. Two active area fractions for collecting n-well inside the pixel were sampled: 30% and 50%. In one instance the guard rings around the n-wells were omitted. One of the passive structures was purposefully put near the edge of the device to facilitate laser TCT measurements (see section 4.5.1). A large passive pixel array of 2 x 2 mm^2 dimension was implemented to enable charge collection measurements with a beta source. One of the passive pixel structures was placed on the edge to facilitate Edge-TCT measurements (section 4.5.1).

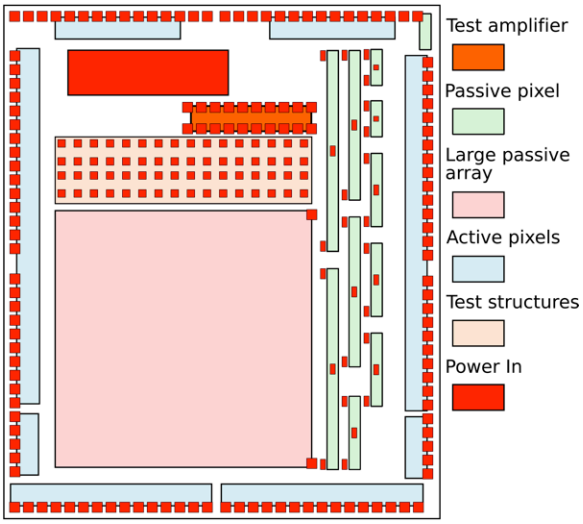

Figure 12 CHESS-1-AMS block diagram indicating the several types of test structures.

The chip was submitted in an MPW run in August 2014. It came back from the foundry in November 2014.

4.3.2 Tower-Jazz CHESS1

CHESS-1-TJ chip was designed by D. Dipayan and R. Turchetta (STFC-RAL) in the TowerJazz HR-CMOS 180 nm technology, which features a high-resistivity epi layer grown on a substrate. The collecting wells are n-type and the epi is p-type. Both p- and n- type substrates are being investigated. The electronics design features the amplifier designed in the middle of the pixel area, separated from the collecting n-wells in the corners. This leads to small values of input capacitance. The number and topology of the collecting wells has been varied. Several epi thicknesses have been used, varying between 5 μm and 25 μm.

The chip was submitted as an Engineering Run jointly with another project in January 2015. First wafers came back in April 2015.

4.4 CHESS2 Chip Submission

The purpose of CHESS-2 chip submissions is to fabricate large-scale devices in our target technologies. This would enable us to characterize several performance aspects crucial for using CMOS-based sensors:

- Readout architecture capable of processing large number of channels with single-bunch timing resolution. Given the binary readout method (which is a traditional ATLAS strips technique); this requires low timing jitter of threshold crossing in the analog front-end. In

the digital part of the chip fast hit scanning has to be implemented that guarantees near-100% hit readout for realistic chip occupancies.

- High-speed I/O bus streaming hit information in a synchronous way from a large pixel area. There is no handshaking between the readout chip and the CMOS sensors. The hit information is being sent out all the time. However, the number of I/O channels is being kept smaller than the channel density in the baseline strip design to help with the wire bonding as the limiting factor on the construction speed.

- Possible correlated noise effects that may affect the threshold level needed for realistic device operation. If present, this could increase the signal level requirements beyond the S/N estimate based on random noise components. One example of possible issues is cross-talk between high-density of output lines going to the periphery of the device from individual pixels (Section 1.3.1).

A successful implementation of the large-scale chips would also make it easier to characterize the essential performance parameters with sources and beams: signal, noise, hit efficiency. Additionally, it may allow starting of module prototyping effort.

The CHESS-2-AMS chip has been designed and most structures are laid out (see Figure 13). It will use reticle size of 2.45 x 1.8 mm^2. The area will contain three sections of 127 strips with 32 pixels per strip, as well as multiple test structures.

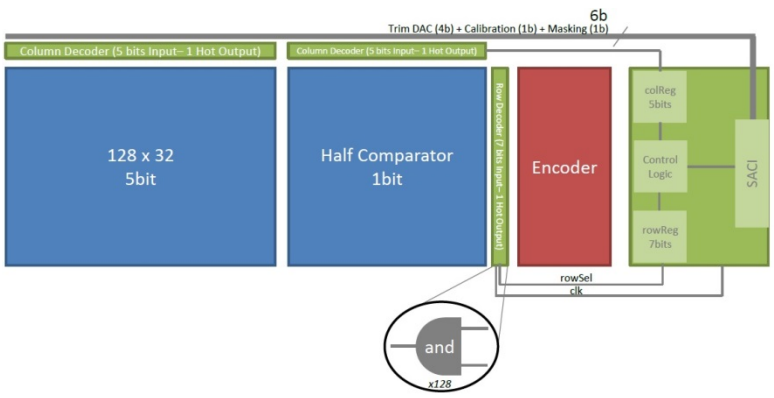

Figure 13 CHESS-2-AMS block diagram

Each section has its own 14-bit output bus. Several design alternations will be prototyped, such as implementation of comparators in the pixels, in peripheral region, or a "split" design. This will be an Engineering Run submission. Unlike the previous MPW run fabrication, the Engineering Run allows us to use substrates with non-standard resistivities. Four values between 20 Ωcm and ~1 kΩcm will be tested to find out the best signal yield over the relevant fluence range (Section 4.5.2). We had two design reviews with external reviewers. The final was held on July 1st (3) .

A CHESS-2-TJ design is currently being developed. It will be finalized following the CHESS-1-TJ characterization studies.

4.5 Support Electronics developments

A successful and diverse characterization program requires a well-developed infrastructure for testing. The HVStripV1 chip needed an FPGA-based digital readout, which was achieved with a commercial low-cost Atlys board (4) (see Figure 14). It was later adapted for the module testing in the baseline program.

Figure 14 The Atlys FPGA (with a Xilinx Spartan6) board used for testing

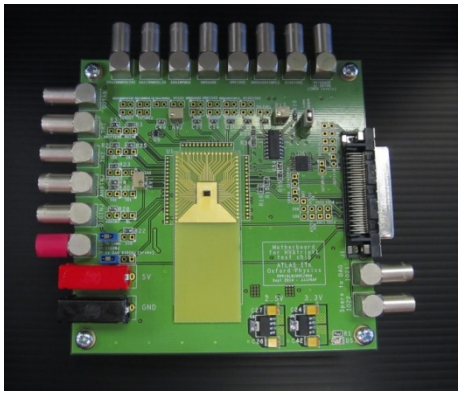

Figure 15 Photo of an HVStripV1 motherboard (green) with a daughterboard

Firmware and software from the standard baseline SCTDAQ readout was ported to enable the chip readout. The test chips were mounted on carbon fibre based carrier board to minimize amount of material in source and beam tests. The carrier board is placed on motherboard implemented in a standard PCB material to provide chip biasing and connection to the Atlys board (See Figure 15).

The CHESS-1 chips do not have the digital outputs. However, they feature high number of I/O lines due to the numerous test structures implemented on the chips. We still used motherboard/daughterboard separation in this case. However, the daughter board is also made from PCB material, and a high-density interconnect is used to route over 100 I/O signal lines.

4.6 Testing Efforts

The centralized support electronics development facilitated the chip testing among the different participating groups. The majority of the tests were done for AMS technology due to the chip availability. In the following sections we show results for AMS chips unless specified otherwise.

The maximal radiation level expected in the ATLAS strip tracker is 1.6×10^{15} neq/cm^2 and 60 Mrad. We have performed several irradiation campaigns:

- We have irradiated CHESS-1-AMS with neutrons in several steps up to 5×10^{15} neq/cm^2 in the nuclear reactor at Ljubljana.
- We also irradiated CHESS-1-AMS with gammas in Sandia National Laboratory in the range between 1 and 100 Mrad.
- HVStripV1 was irradiated with gammas in the range between 0 and 60 Mrad.
- Very recently we irradiated HVStripV1 chips with 27 MeV protons in Birmingham, with fluence likely to exceed 5×10^{15} neq/cm^2

We are planning on irradiating CHESS-1 chips with protons in CERN PS facility. The 27 GeV protons are rather attractive, since they present a combination of the bulk damage and ionizing dose which is not too far from the experimental expectations. The proton irradiation would complete the studies, since some aspects of the bulk damage can be different from neutrons. However, we do not think that our conclusions would change significantly, since in the real experiment hadronic damage in the strip region is dominated by neutrons.

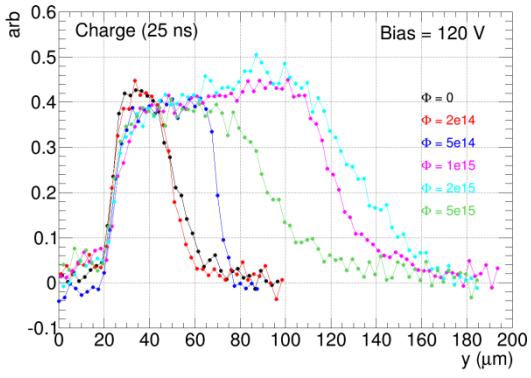

Figure 16 The signal amplitude versus laser injection depth for several fluences after neutron irradiation.

4.6.1 Edge TCT results

The edge-TCT technique involves sending a focused laser beam at the side surface of a sensor and reading out signal from the top side segments, strips or pixels. The focal point of the beam can be scanned along the depth of the device. One then can derive the depleted depth of the devices and the carrier velocity distribution from the collected waveforms. Figure 16 shows

the collected charge (the integral of the induced current pulse in 25 ns) measured in an Edge-TCT scan across the pixel centre as a function of laser injection depth for several fluences. (A standard annealing cycle of 60 C for 80 minutes was applied both here and for the charge collection study in the next section.) The size of charge collection depth can be assessed from these scans. Surprisingly, the size of the depleted region grows within the range of relevant fluences. This is attributed to initial acceptor removal process, which effectively increases the device resistivity.

Figure 17 shows the result of the scans with added dimension of the position along the pixel. One can see that before irradiation there are acceptance gaps between the pixels. This is likely due to a combination of small depletion region, ~20 µm, and guard rings between the collecting n-wells. The gaps largely disappear after $5x10^{14}$ neq/cm^2 neutron fluence, , when the charge collection region increases substantially. This observation underscores the need for higher initial wafer resistivity.

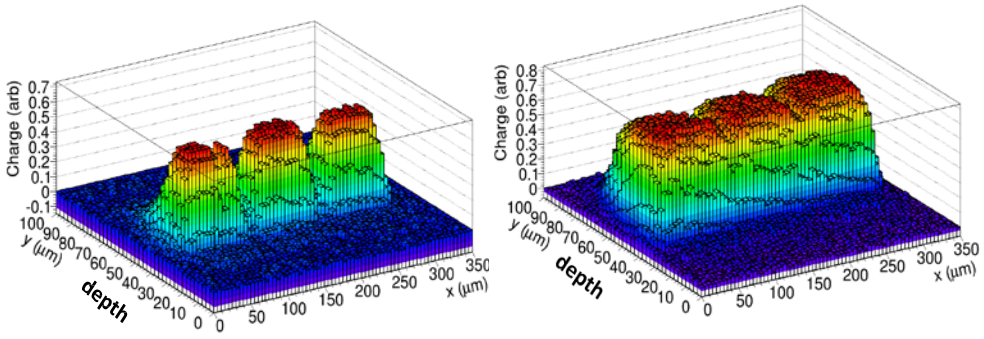

Figure 17 Signal amplitude in an edge-TCT scan as a function of depth and position along the pixel. The left plot is before irradiation. The right plot is after $5x10^{14}$ neq/cm^2 .

4.6.2 Sources

Charge collection studies with radioactive sources present a convenient way to find out the signal amplitude. Such investigation was enabled by presence of large passive array in CHESS-1-AMS chip, which allowed data collection within a finite acquisition time.

Figure 18 shows the evolution of the signal charge in the sensor as a function of fluence after neutron irradiation. A shaping time of 25 ns was used in this study. There are several phenomena affecting this dependence:

1. Quick removal of the signal component coming from the diffusion process.
2. Initial acceptor removal that leads to higher bulk resistivity and increase of the depletion depth (confirmed with Edge-TCT method).

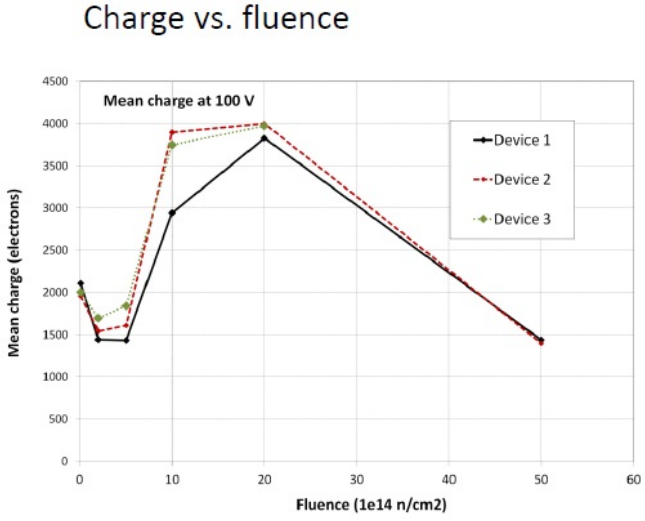

Figure 18 Signal charge collected in CHESS-1-AMS device with a MIP source as a function of the fluence after neutron irradiation.

3. There is eventual reduction of signal due to trapping. However it happens above the nominal strip system fluence.

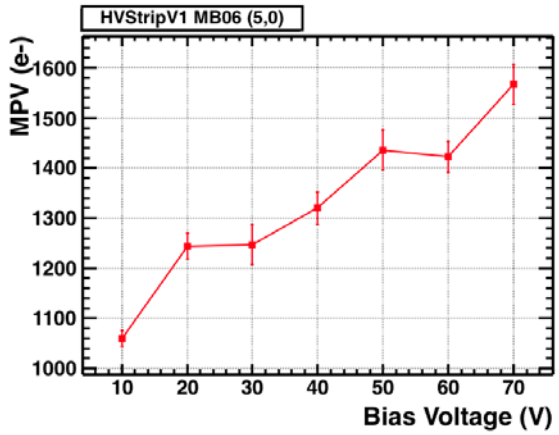

Figure 19 Signal charge collected in HVStripV1 device with a MIP source as a function of bias voltage

A key figure of merit is the minimal amount of signal one can get over the relevant range of fluences. One can conclude that for the initial resistivity of 20 Ωcm it is 1500 e-.

A MIP response was also studied with the HVStripV1 chip. The charge collection results are consistent with the corresponding values for CHESS-1-AMS chip pre-rad in the available bias range (Figure 19).

4.6.3 Test Beams

Feasibility of carrying out test beams has been demonstrated with HVStripV1 chips. In spite of the small size of their active area, response map corresponding to pixel geometry was obtained at a micro-focused X-ray facility (Diamond Light Source). Initial tests were done at the DESY-II Test Beam Facility using electron beams from 3-5.5 GeV. Further tests are being planned both at DESY and possibly CERN.

4.6.4 Characterization of Building Blocks

The implementation of separate pixel and amplifier test structures allows us to characterize some of the sensor properties, the signal amount in the system and its analogue processing.

4.6.4.1 Pixels

We have measured the pixel capacitances for different geometries and active area fractions. We observe a rather good match with expectations from simulations, especially for long pixels, 400 µm and 800 µm, where the agreement is better than 10%. We estimate the total pixel capacitance to be 0.45 pF for 800 µm, same as in simulations.

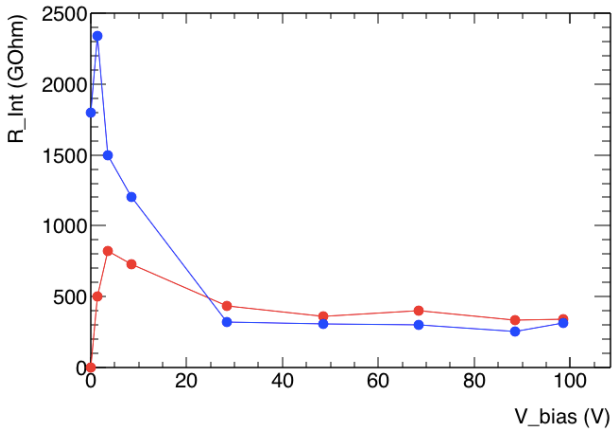

Figure 20 The Inter-pixel resistance as a function of bias voltage for gamma-irradiated sample.

We have measured inter-pixel isolation (Figure 20) after gamma irradiation. It remained very high even at low bias voltages for test structures without guard rings around pixels. This is due to the presence of significant p-type implantations between the pixels.

In IV tests of the pixels we have observed early (<120 V) breakdowns for structures with 30% active area fractions. These must be due to localized high field regions. The structures with 50% active area fractions did not have this feature, which makes them preferable for future designs.

In general, we find that the bias voltage range is very stable, even after irradiation, unlike the baseline sensors. The breakdown voltage is defined by the spacing between the collecting n-well and

the bias connection. For the structures with the more promising 50% diode area fraction it remains in the 130-150 V range over the relevant fluence range. This is unchanged compared to pre-radiation case and it is consistent with 120 V bias design rules used. A radical way to improve the voltage range and the signal level would be to implement back side biasing with post-processing. This should be feasible, but remains to be tested.

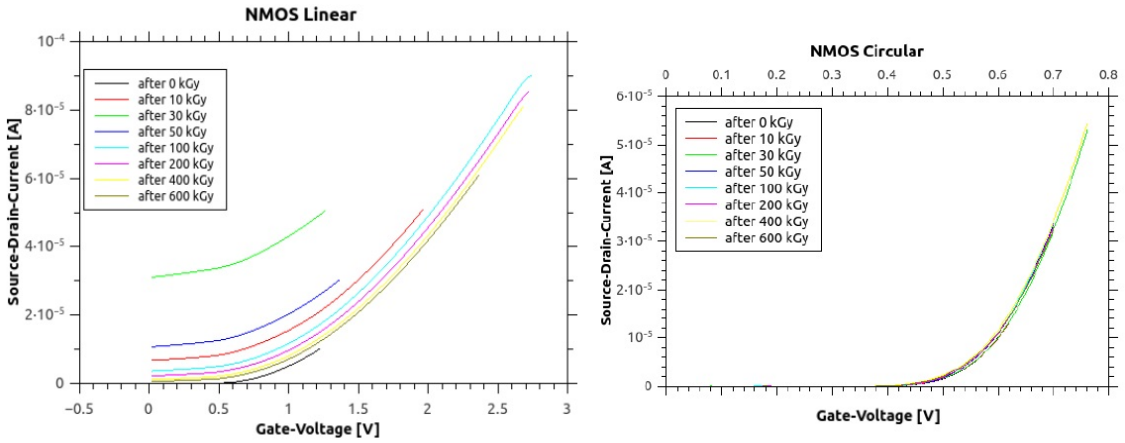

Figure 21 Test results of linear and circular transistors.

4.6.4.2 Transistors

The transistor performance has been characterized for HVStripV1 chip. One example is shown in Figure 21, where the differences between linear and circular transistors can be seen. As expected, the circular transistors are more immune to radiation effects. Characterization tests for CHESS-1 chips are in preparation.

4.6.4.3 Amplifiers

We have done first round of testing the isolated amplifiers in CHESS-1-AMS. Several biasing schemes have been tried to obtain the best response. Input-referred noise was estimated to be in 40-80 e- range. This is smaller than expected 100 e- specification. However, the input capacitance is larger in presence of collecting n-wells. So in the end we will likely have around 100 e- noise.

We also evaluated timing properties of the signal. The signal rise time varies between 10 ns and 27 ns for the signal up to 3000 e-, indicating that the analogue time resolution should be consistent with the signal bunch crossing. FWHM is under 250 ns in the same signal range (see Figure 22).

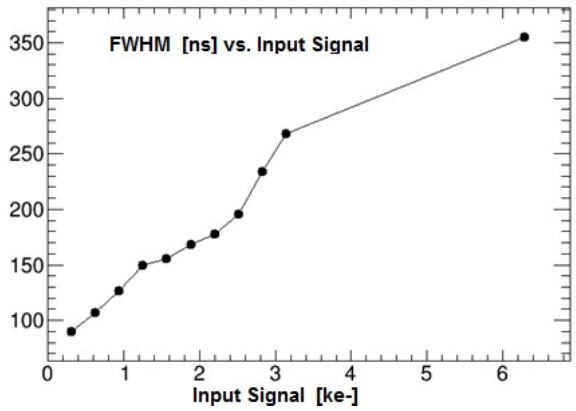

Figure 22 FWHM of the amplifier response as a function of input signal for the optimal amplifier biasing scheme.

Amplifiers in HVStripV1 chip feature a somewhat different design. Their

performance has been characterised using different x-ray sources before and after irradiation (sees Figure 23 and Figure 24). One can see a very linear response, with a small degradation after the full ionization dose of 60 Mrad. The design with standard linear transistors has higher gain. The noise

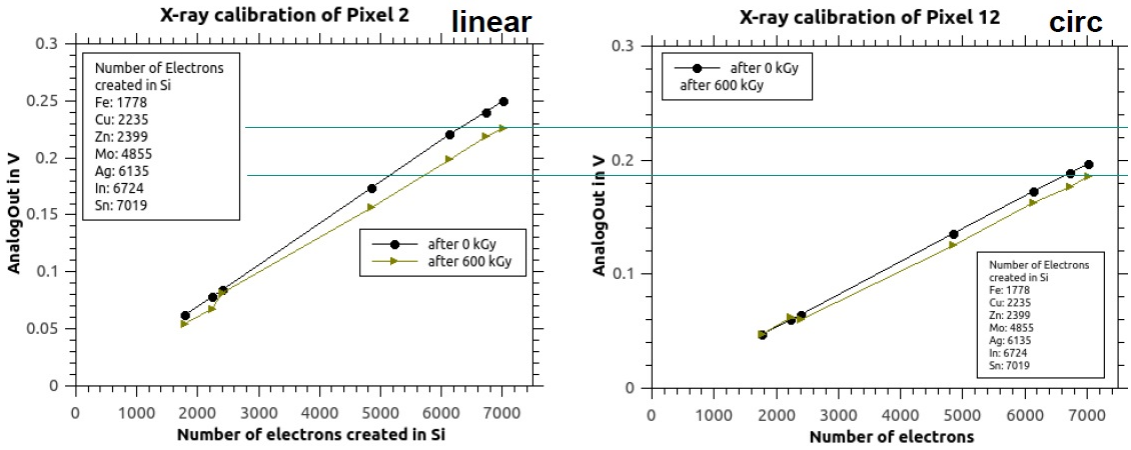

Figure 23 Response of the amplifiers calibrated with different x-ray sources before and after 60 Mrad of gamma irradiation. Left plot corresponds to design with standard (linear) feedback transistor. The plot on the right is for transistor with circular feedback

dependence on dose has more structure. Generally the noise increases, with an additional peak at around 5 Mrad value.

4.7 Radiation Hardness Summary

The following are key findings regarding radiation hardness of HV-CMOS technology:

- Signal gain is rather stable. There is fewer than 10% deterioration after 60 Mrad dose for HVStripV1 design.
- Pre-radiation noise level is very good, under 100 e-. It does rise with ionization dose, to the level of 300 e- for HVStripV1. The dependence of CHESS1 amplifiers will be tested in the near future.
- Signal dependence on fluence is non-monotonic. There is initial drop due to arrest of charge coming from diffusion, followed by increase due to effective resistivity increase. The minimal signal value for the initial 20 Ωcm resistivity is around 1500 e-.

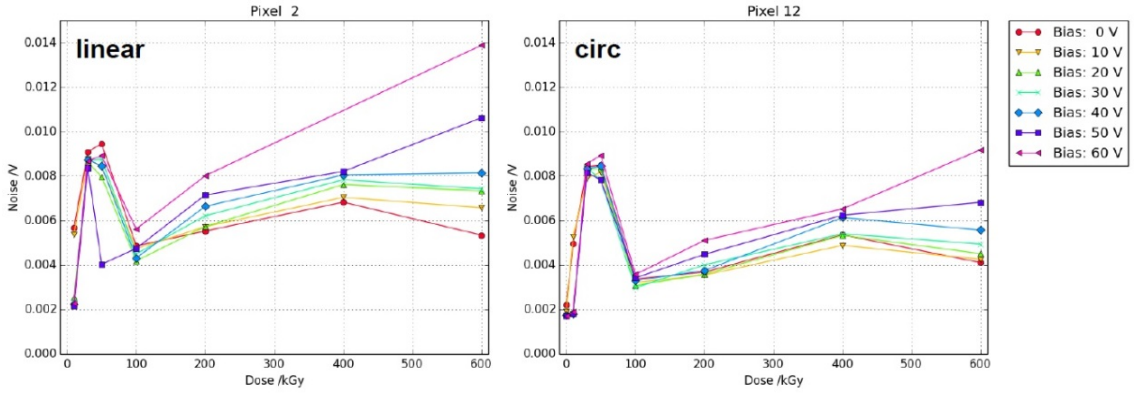

Figure 24 Noise of the amplifiers as a function of ionization dose. Left plot corresponds to design with standard (linear) feedback transistor. The plot on the right is for transistor with circular feedback transistor design.

- There is an initial loss of signal in the area between the pixels, which disappears when the charge collection depth is increased substantially.
- The inter-pixel isolation is maintained at high level due to built-in features of the technology.
- There is a preference for using pixels with higher active area fraction, since they maintain higher breakdown voltage.

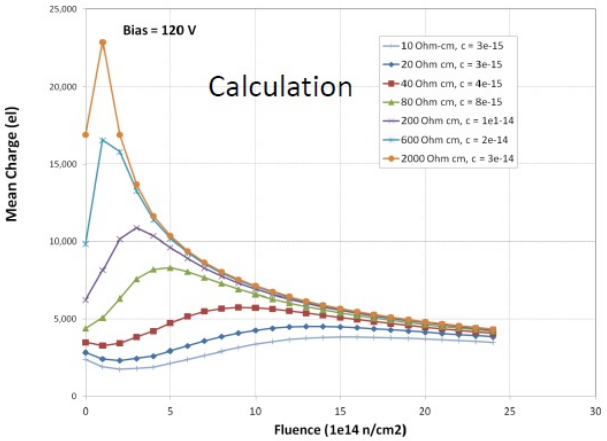

Figure 25 Calculation of charge collection in HV-CMOS sensors as a function of fluence for different initial resistivity values.

Several of these conclusions lead to high desirability of higher initial resistivity with associated higher depletion depth and larger minimum signal. Figure 25 shows estimates of signal as a function of fluence, which are based on CHESS-1 test chips and high-resistivity sensor studies.

The results indicate a preference for resistivities above 80 Ωcm, where the initial signal drop at low fluence is absent. In this case the minimal signal of at least 4500 e- is achieved at highest fluence. It does not grow with further increase in initial resistivity in spite of larger initial depletion depth (Table 2). This is due to dominance of charge trapping centers in the bulk of silicon. The additional problem with resistivity values above 600 Ωcm is distorted field configuration with top-side biasing (5). These considerations point to the range between 80 Ωcm and 600 Ωcm as most preferable.

We will investigate several high-resistivity values with CHESS-2 submission.

ρ [Ω*cm]	Depletion [μm]
10	11
20	15
40	22
80	31
200	49
600	85
2000	154

Table 2 The depletion depth before irradiation as a function of initial bulk resistivity. A uniform depletion model is assumed.

4.8 Signal/Noise Assessment

The signal to noise ratio for MIP signal is a key issue for our technologies due to small depletion region. It is rather high before irradiation (see Figure 26). If the noise were to stay constant, the minimal signal of 1500 e- (Section 4.5.2) would correspond to S/N of 13 to 15.

However, a possible increase of noise, up to a factor of 3, may lead to deterioration of the performance. The essential factor that can allow us to maintain the S/N is

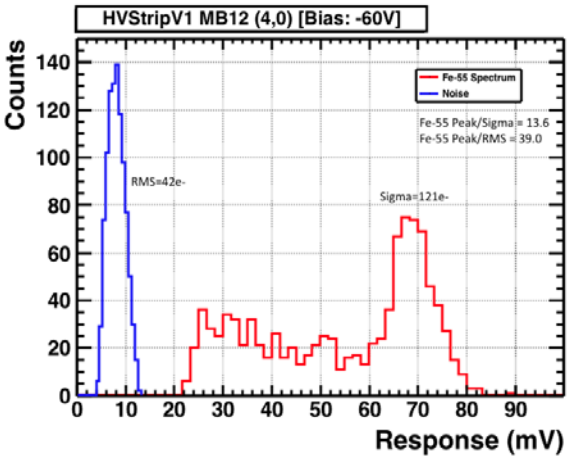

Figure 26 Response to Fe-55 signal for HVStripV1 chip.

signal increase due to higher bulk resistivity. We expect to gain a similar factor of three as the result, and to maintain the S/N of at least 13-15.

5 Plans for the second year

Given the progress already made, we are ahead of the schedule in some aspects of the programme, especially with the submission of the CHESS2 chip. Testing of the TowerJAZZ CHESS1 has been significantly delayed due to late delivery of the Chip from the foundry. There is still a need for further studies on the impact on the global mechanics and electronics and of course more refined studies on the impact on the track reconstruction. Overall the biggest challenges are the ABCN' development and the CMOS technology decision, which are described in section 5.1 and 5.2.

The overall resources for a successful second year are so far in place, as the biggest item (CHESS2 submission) has already been agreed upon. The available manpower is still tight, but we are confident to add a few more students to this effort which will significantly speed up the testing effort.

5.1 ABCN' and HCC development

In the original plan - as outlined in section 1.3.3 - we have envisaged having a prototype of the ABCN' available in year two. As already stated before, the ABCN' is effectively an ABC130 without the analogue front-end. However, delays in the production of the original ABC130 and a lack of chip design resources have rendered the original plan not feasible.

However, there is an implementation of the digital part of the ABC130 in firmware (VHDL implementation). Given the delays, we have investigated to read out CHESS2 using an FPGA and concluded that for the readout of a single or a few CHESS2 this will be quite feasible, however in order to assemble a complete module including hybrids further studies are needed and ultimately a ABCN' is required for a full StripCMOS-based module

5.2 Technology decision

In the original planning, we had foreseen to make a technology choice between the HR (TowerJazz) and HV-CMOS (AMS) technologies towards the end of year one or very early in year two. Given the late availability of the CHESS1-TJ, we have to postpone the decision until we have a full set of results from this technology as well. In order not to impede progress for CHESS2, the design of a CHESS2 chip in HR-CMOS is continuing in parallel. We are very hopeful to have a technology decision now in the second half of year two based on the complete testing results of both CHESS1 chips.

6 Outlook

6.1 Timeline of the ATLAS Phase-II Upgrade

The ATLAS ITk groups are currently preparing the Technical Design Report (TDR) for the Phase-II Strip Tracker. The TDR is due to be delivered in at the end of 2016. After the TDR there is a two-year phase for the pre-production and a three to four year production phase. The current planning is shown in Figure 25.

The StripCMOS three year programme (see section 1.3.3) however will only be completed in summer of 2017. This is of course not optimally synchronized with the baseline TDR planning, which we are very much aware of. Leaving aside potential delays and changes in the LHC schedule we are taking the following steps to minimize the impact. At the time of the finalisation of the TDR, we will plan to have compelling evidence that a StripCMOS solution is feasible and plausible on the given

timescales. Furthermore, we plan to use part of the pre-production phase to finalize the CMOS programme. Given the significant reduction in the number of wire bonds, we assume we can reduce the CMOS pre-production time by at least six month. It is clear however, that at the time of the signing the MoUs for the Strip tracker a decision has to be made by the collaboration. As this is foreseen in summer of 2017, this is nicely synced again with official schedule shown in Figure 27.

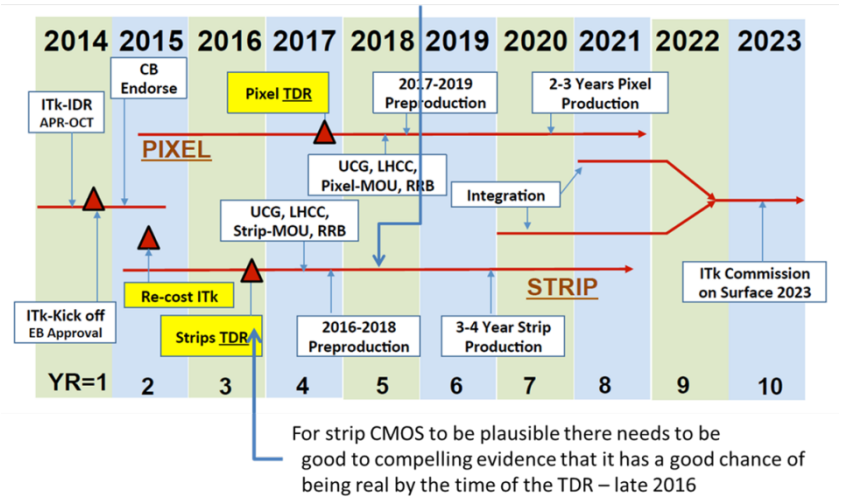

Figure 27 Time for the ATLAS ITk Phase-II Upgrade (May 2015)

6.2 Adoption for other projects within ATLAS ITk

The StripCMOS technology might have application for one of the proposed outer pixel layers. In particular the proposed 5th pixel layer might be considerably cheaper if it consisted of a modified StripCMOS sensor because the data rates are much lower per sensor at this radius, making strip CMOS appropriate (and indeed the purpose of this project is exactly to make a sensor suited to this radius), and the bump bonding could be avoided. The pixel pitch and particularly the pixel length would need to be adapted, but the basic building blocks that have been developed for StripCMOS would be appropriate at the high radius of pixel layer.

7 Bibliography

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