Optimizing the built-in amplifier in HV-CMOS CHESS1

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Isolated amplifier in CHESS1 chip

- HV-CMOS CHESS1 chip has built-in isolated amplifiers
- designed to optimize amplifier performance
  - Six amplifier biasing control
  - Optimization can be done with pulser, without using laser injection or beta source.
  - Change its gain and output signal shape by changing biasing control
- Try to study the amplifier performance as input to CHESS2 design

Table 3.4-e: Fast Amplifier Biasing for optimum performances

Pad number	Pad name	Value
1	iN	65µA
2	Casc	2.4V
3	VPload	1.85V
4	iBias	7nA
5	iFB	2nA
6	iNSF	20nA

3.5. Isolated Fast Amplifier

An array of 7 isolated fast amplifiers circuits is included with an input and out pad. This is to separately test the characteristics of the amplifier in order to separate its characteristics and their evolution with radiation from that of the passive pixel sensors. The amplifier used is the same as the one included in the active pixel array. However instead of being capacitively coupled to the nwell they are capacitively coupled to the input pad. Multiple copies of the amplifier are included to allow testing of matching of amplifiers in close proximity to each other. It will also allow comparing the performance of amplifiers on several of the test chips available to test similar matching across a wafer.

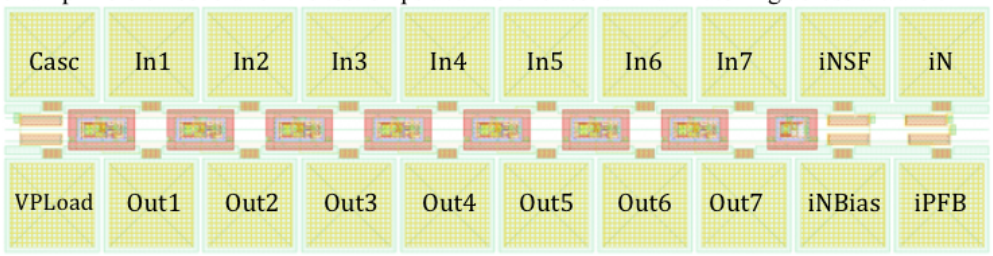
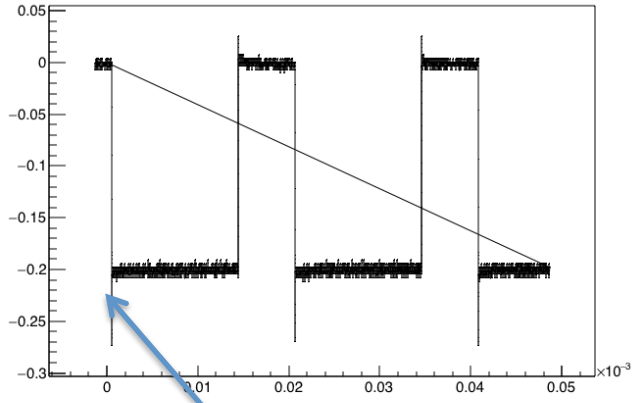


Figure 3–4: Layout of the isolated fast amplifiers.

Setup to test amplifier performance

Voltage (V)



50fF coupling capacitance

Pulser

Input pulse

Voltage source

3.3V bias for amplifier

Isolated Amplifier on CHESS1 chip

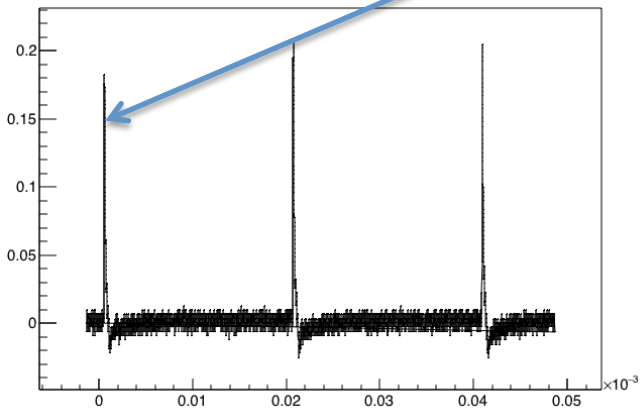
Amplifier output

Source follower

Scope

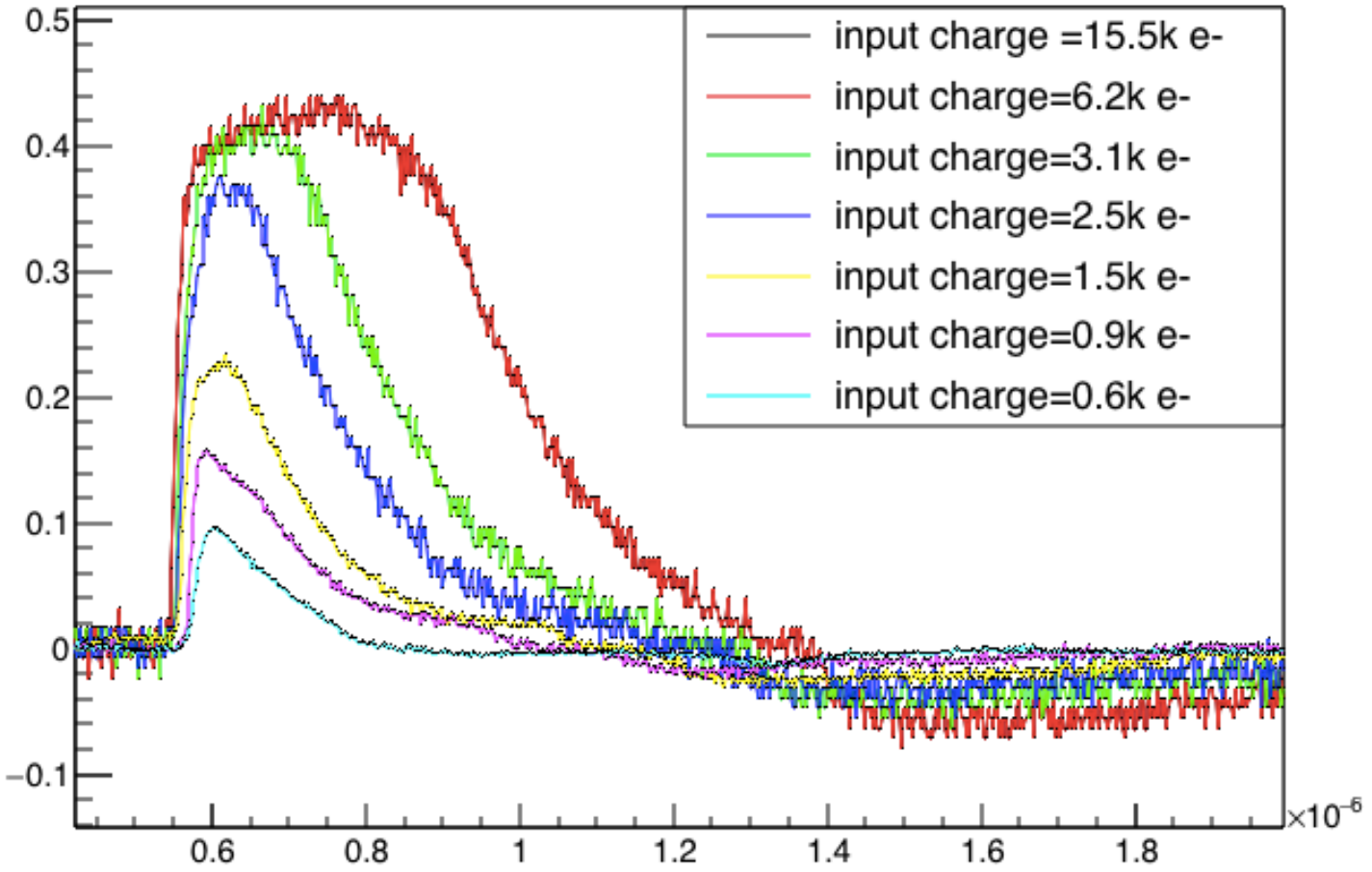
Falling edge

Voltage (V)



Time (s)

Reminder of the output from CMOS amplifier (from last update)

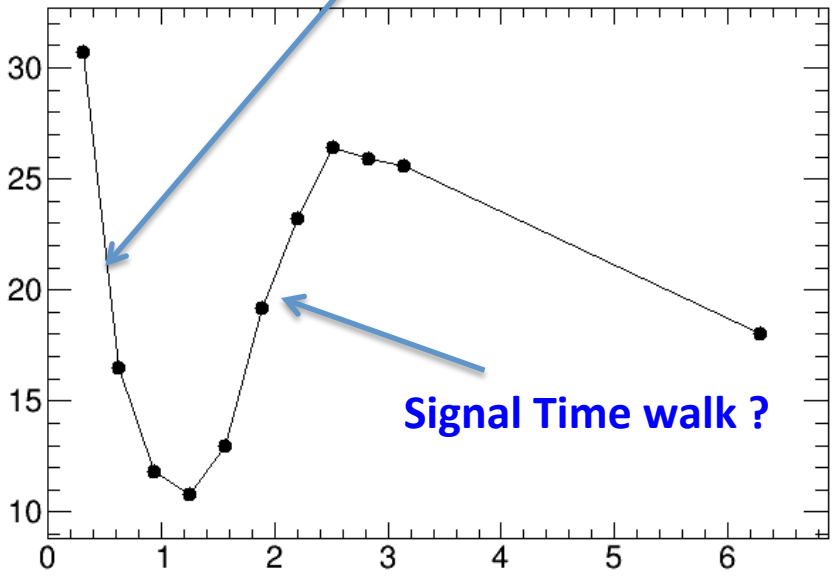


Amplifier output signal rise time (from last update)

- Rise time : 10~30 ns depending on signal size
- **Full width at half maximum is from 80ns ~360ns depending on signal size.**

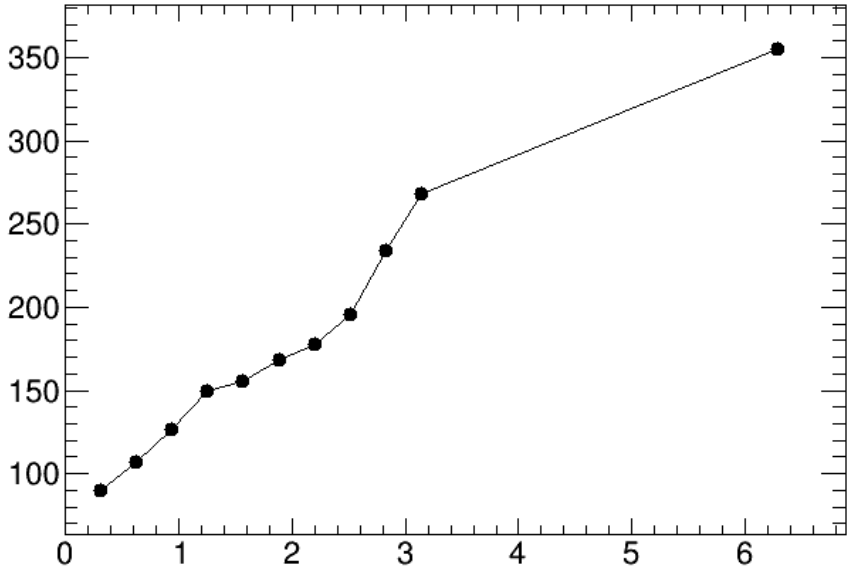
Jitter dominated region ?
Significant background contribution

Rise time (ns)



Input charge (k e-)

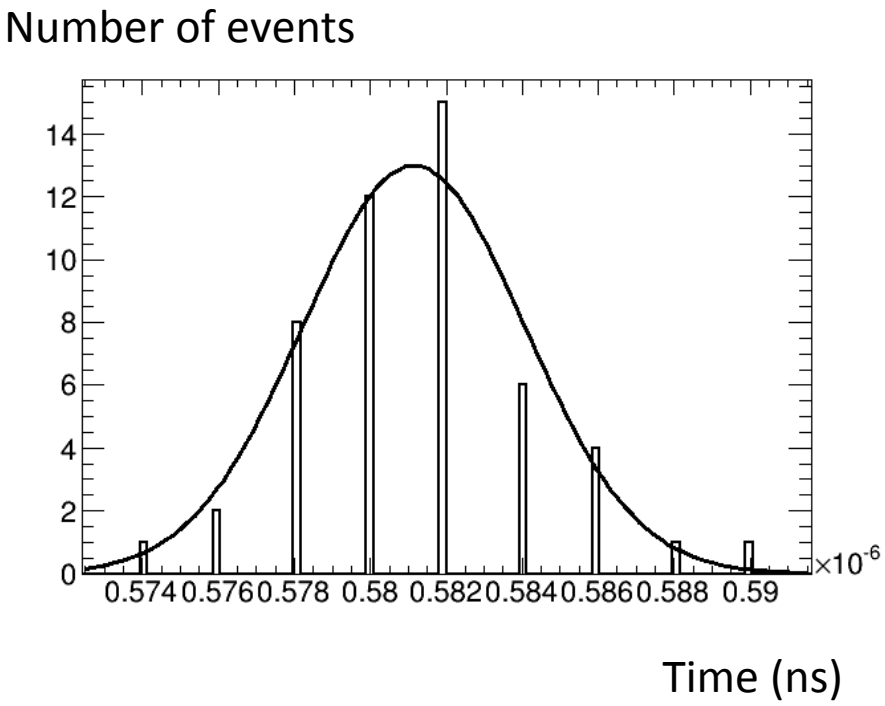
FWHM(ns)

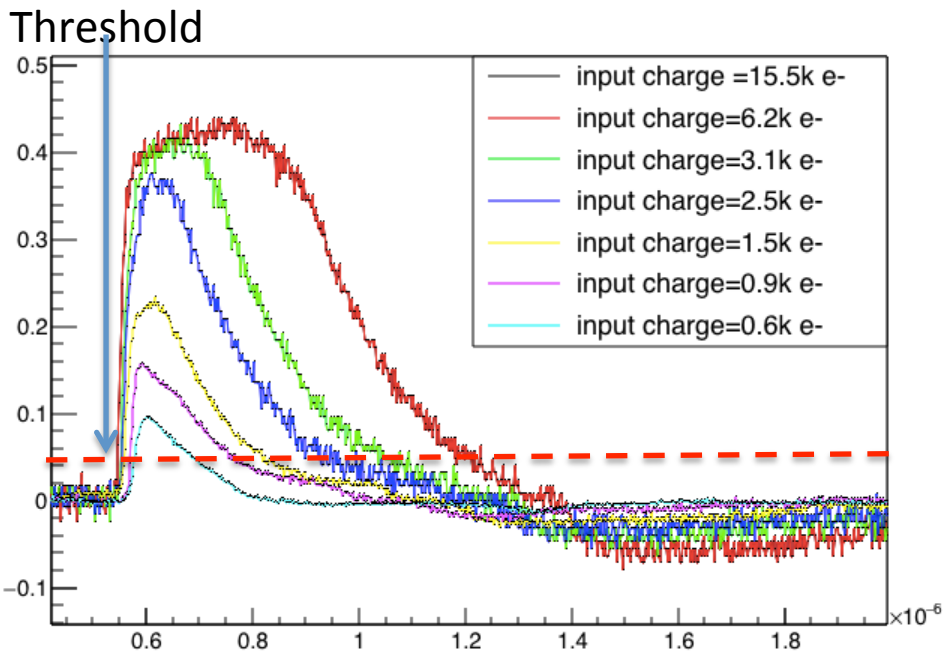


Input charge (k e-)

Timing distribution at a fixed threshold example 1:

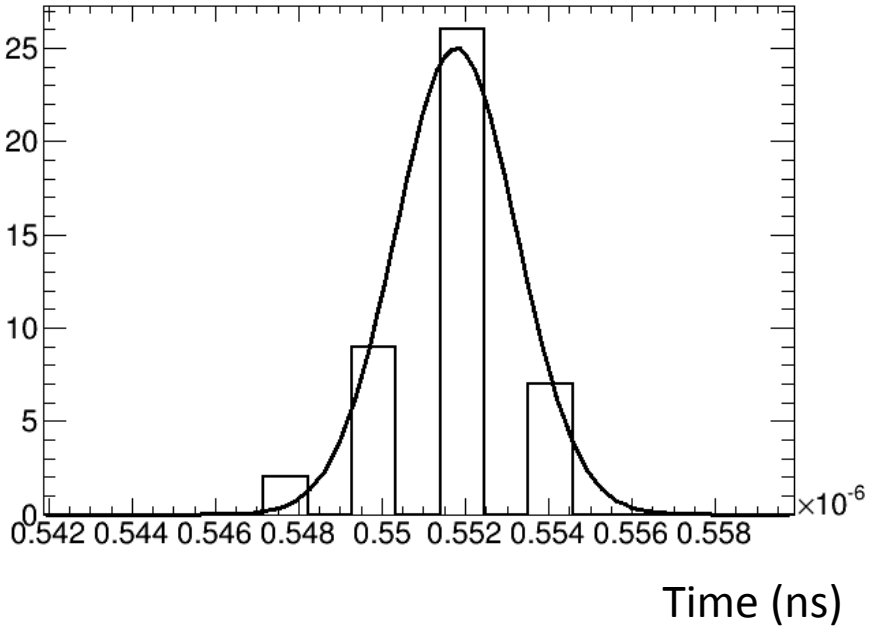
- Output Threshold =0.05V
- Input charge =0.6 k e-

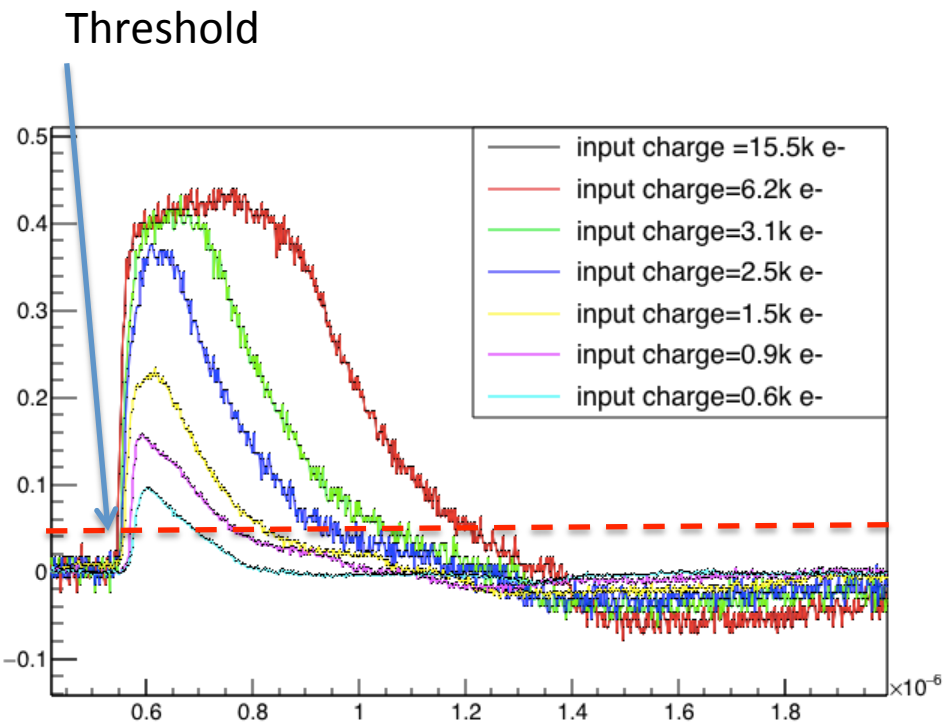




Timing distribution at a fixed threshold example 2:

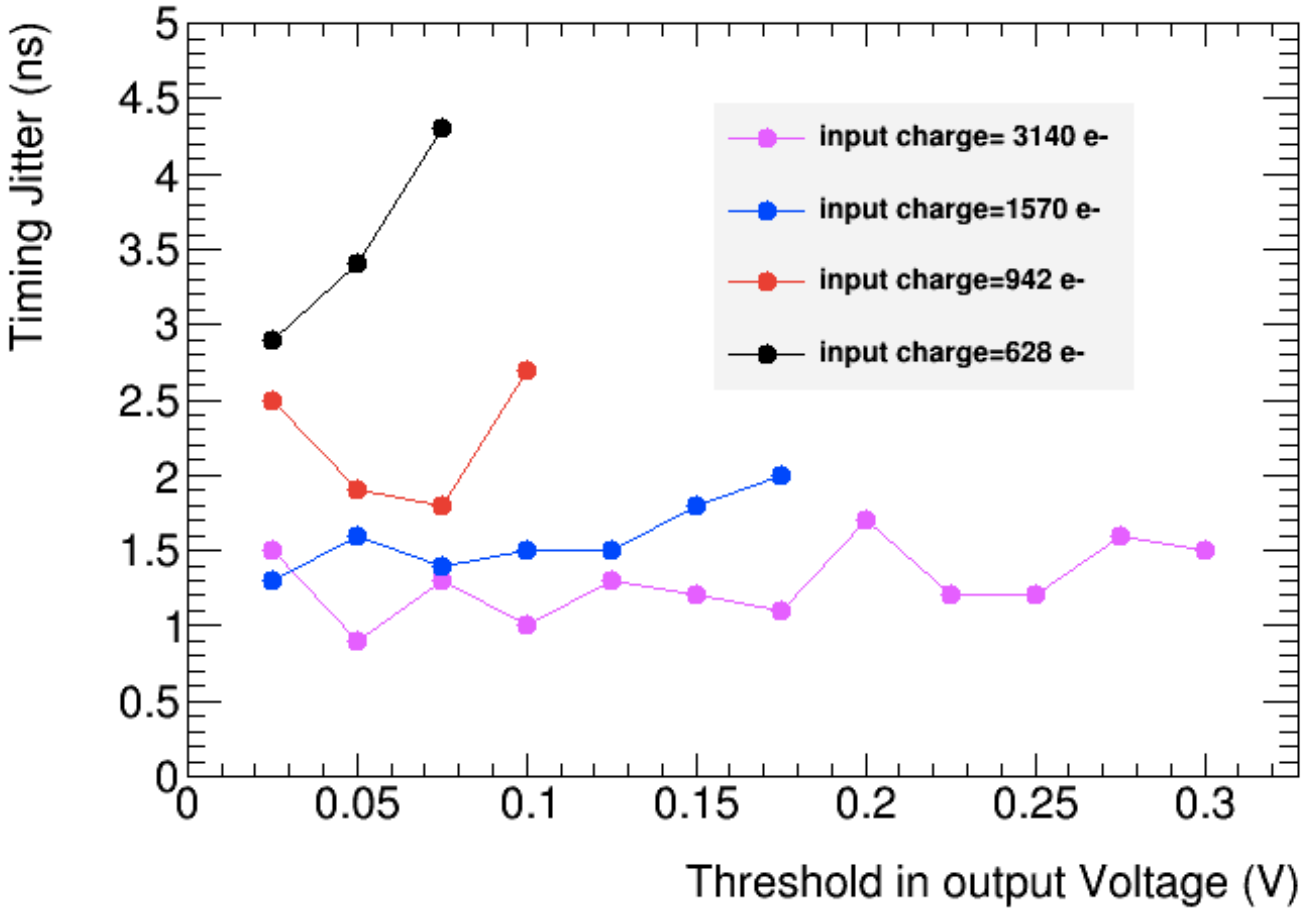
- Output Threshold =0.05V
- Input charge =3.1 k e-



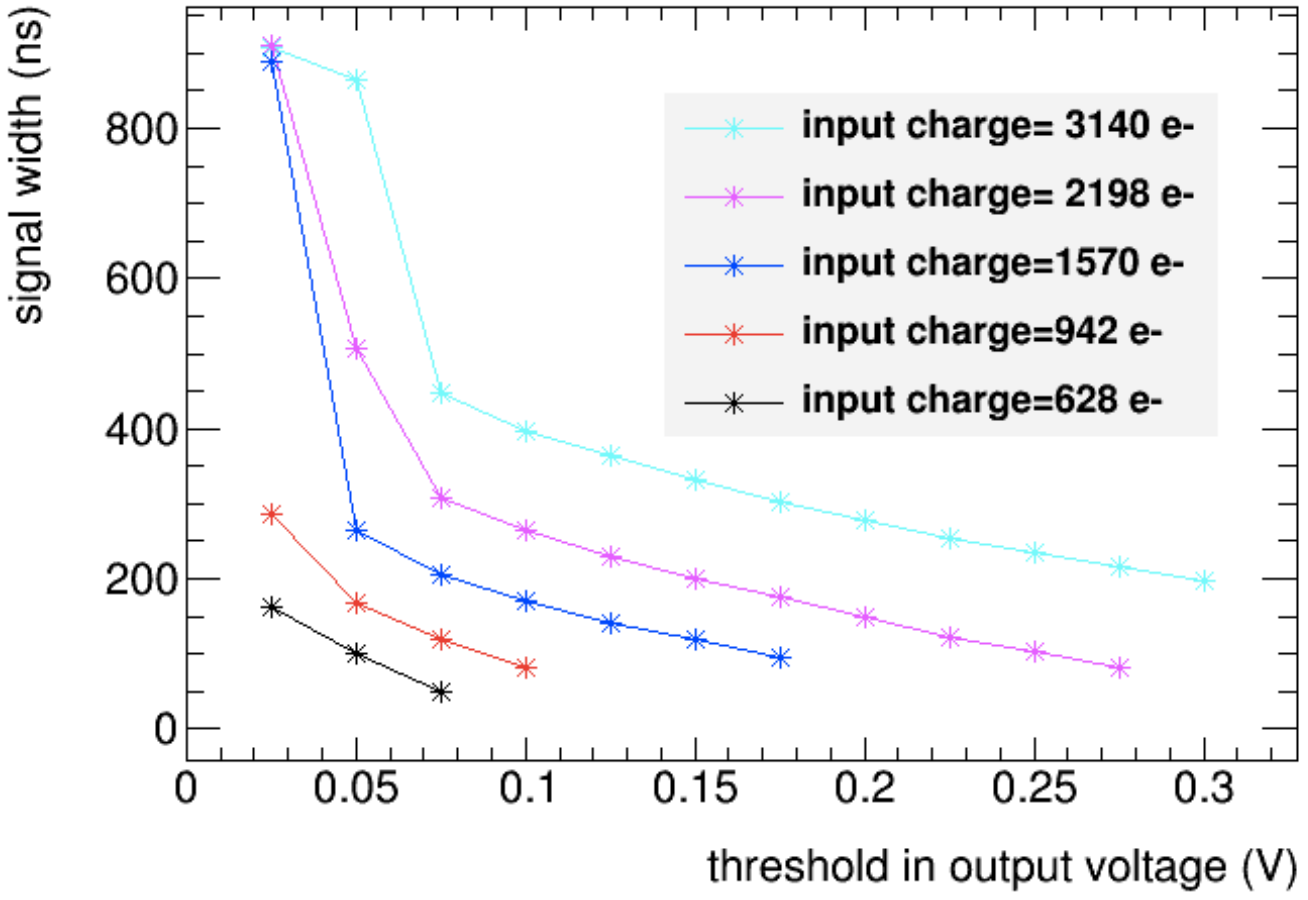


Timing jitter Vs output threshold

Larger jitter for smaller input charge (as expected)



Signal width Vs Threshold



summary

- Timing Jitter of the amplifier has been measured.
  - Less than 5ns
  - Larger jitter for smaller input charge (as expected)