



Introduction & Resources

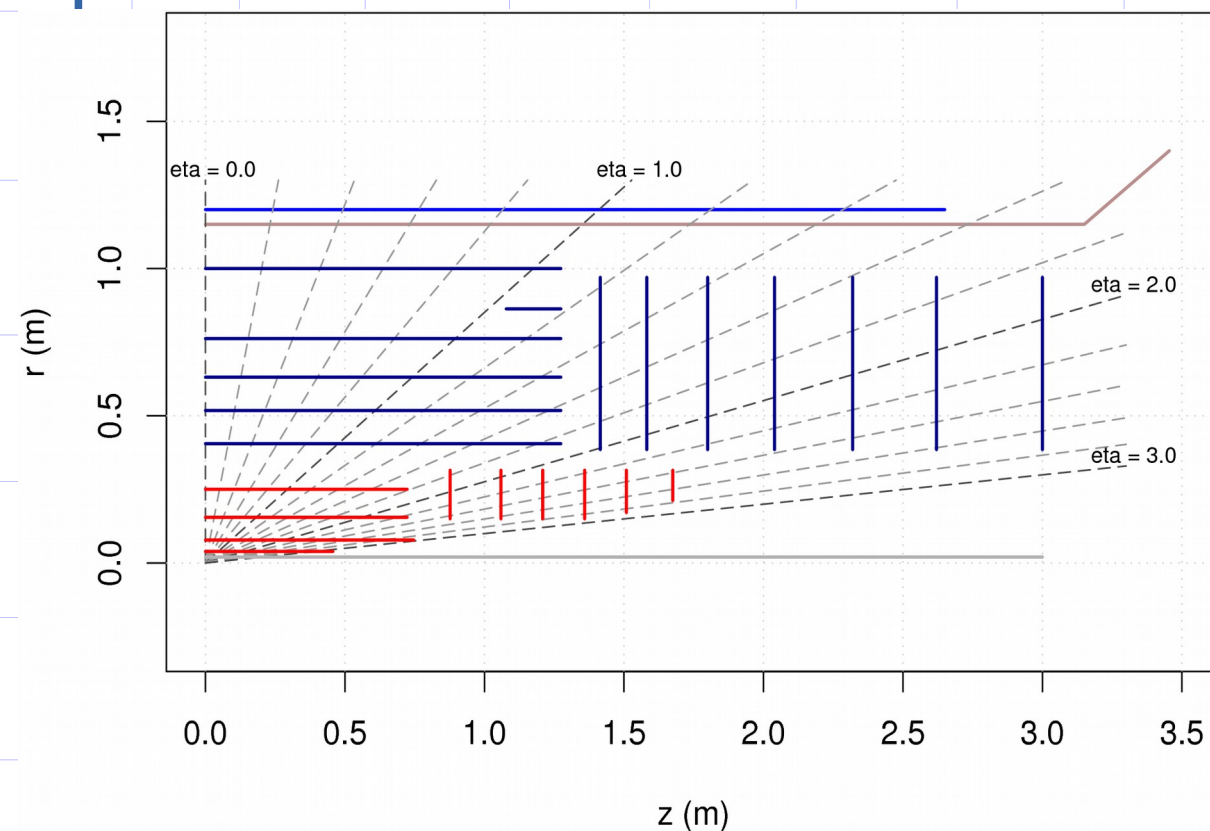
V. Fadeyev, R. Nickerson, M. Stanitzki



Presentations during this Review

- Introduction and Resources
 - M. Stanitzki
- Impact on mechanical & other electronics systems
 - R. Nickerson
- First year results
 - V. Fadeyev
- Second year of the program: Goals and Timeline
 - J. Dopke
- Summary

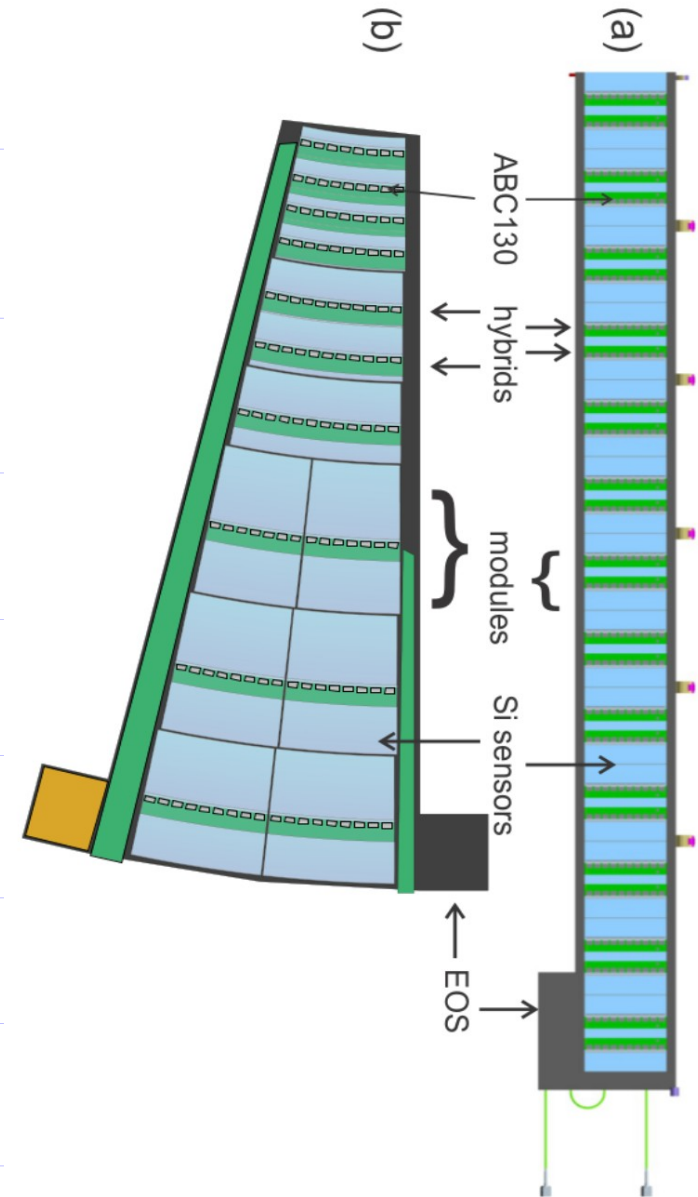
The ITk Strip Tracker Design



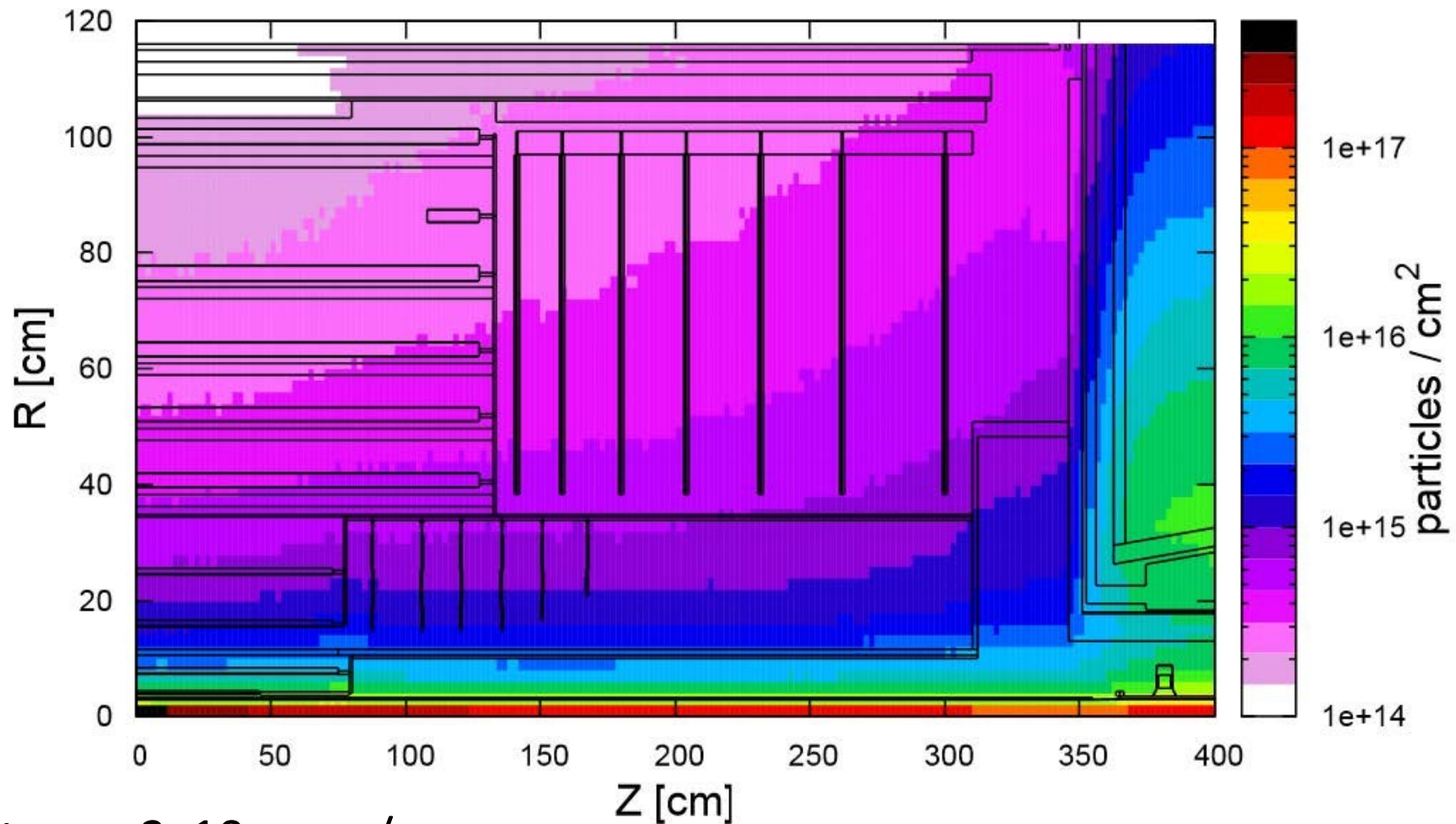
- As spec'ed in the Lol
 - And Subject to change
- Total area of $\sim 200 \text{ m}^2$
 - 95 % of the are in the strips
- Strip Tracker
 - 5 barrel layers
 - 7 disks (per side)
- Modular building blocks
 - Staves and Petals
- Current Design being re-evaluated

Strip Tracker Details

- Petals and Staves
 - Double-sided
 - Small-Angle-Stereo Configuration
- Basic Building Blocks
- Modules
 - sensor+hybrids + ASICs
- Shared “Core”
 - Bus tape
 - Power distribution
 - Cooling
 - High-speed Optical link
 - Mechanical support



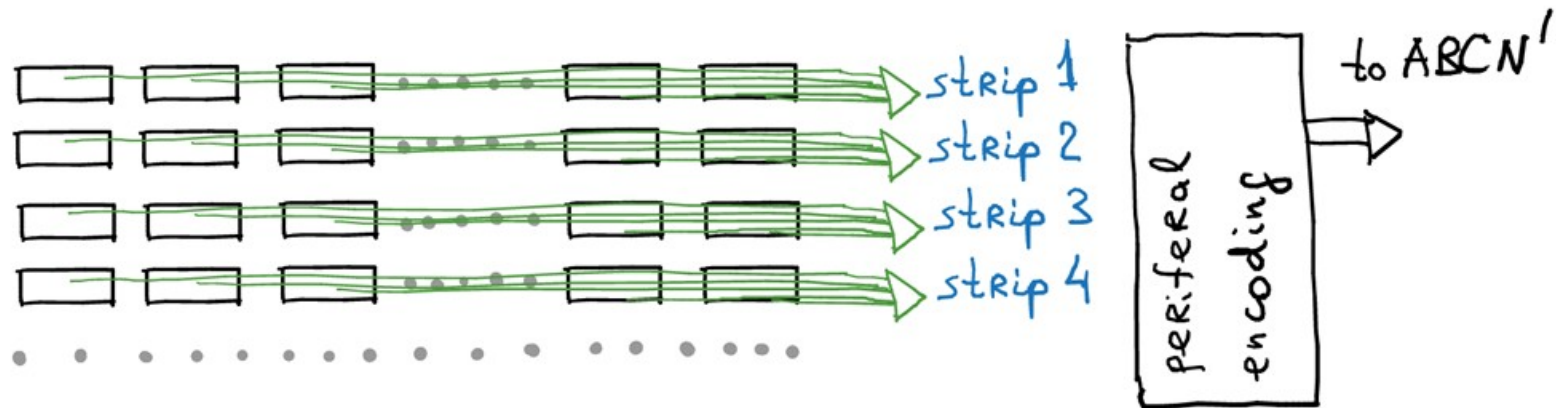
Radiation Hardness Requirements



Neutrons: 2×10^{15} neq/cm²

Photons: 60 Mrad

The CMOS approach for Strips



- Keep everything beyond the Module
 - Minor modification may be required
- Replace Module with
 - CMOS Sensor, 40 μm pitch, 2.3 cm strip length composed of 720 μm long pixels with HL-LHC level radiation hardness
 - Digitally z-encoding
 - New ASIC (ABCN') \rightarrow "ABC130 without analog front-end"



CMOS Advantages

- Three main benefits compared to the baseline silicon strip approach
- Reduction of material
 - Thinner sensors
 - Elimination of Small-Angle-Stereo
- Improved resolution
 - Finer sensor pitch
 - Less material
- Cost savings
 - Reduction of the silicon area by $\sim 50\%$ $\rightarrow \sim 30\%$ cost saving
 - Reduction of assembly time (non-core costs)
 - Cost reduction for the Silicon itself (commercial process)



For Reference

Parameter	Planar Sensor	StripCMOS Sensor
r- ϕ resolution	20 μm – 23 μm	11 μm
z-resolution	850 μm	280 μm
Two hit resolution in r- ϕ	160 μm -240 μm	80 μm
z-element length	2.5 cm	720 μm (2.4 cm / strip)
Fraction of two hit clusters	15% - 20%	2%-3%
Geometry inefficiency on stave	$\sim 0.7\%$	$\sim 1\%$
Radiation Lengths per stave	1.8%	1%
Insensitive crossings after a hit	1 BC	0.3 BC (1/32 of strip is dead for 10 bunch crossings)
Number of Signal Wire bonds	O(5100)	O(1100)

The StripCMOS Collaboration

- Main Goal
 - Develop a replacement sensor for the ATLAS ITk strip tracker
- The collaboration
 - 49 authors from 13 institutions
- Both ATLAS & non-ATLAS members
- RadHard CMOS Technologies
 - Interest also beyond ATLAS



The StripCMOS Collaboration



The Three Year Programme

- ATLAS started three-year programme to study CMOS as alternative for the base strip tracker solution
 - Clearly defined breakpoints after each year
- Phase 0
 - Mid 2014
- Phase 1
 - June 2014 - June 2015
- Phase 2
 - June 2015 - June 2016
- Phase 3
 - June 2016 - June 2017







Phase 0

- Define programme and identify Resources
- Establish Group with CMOS strip tracker goal which does not significantly impact planar preparations

Break Point 1 Mid 2014
Group established, resources secured for Phase-1

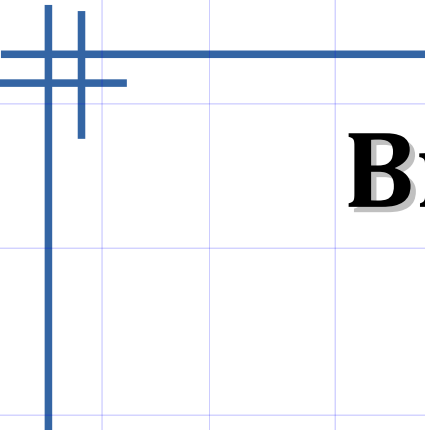


Phase 1

- Goal: Demonstrate Feasibility of CMOS
- Sensor:
 - Relevant foundries selected 
 - Radiation hardness evaluated 
 - Pixel Characterization
 - Boundary electronics architecture understood
 - Cut lines, stitching, multi-reticule possibilities at foundries evaluated.
 - Common read-out selected
- Architecture
 - Decision for Digital Z-encoding 
- Physics requirements
- Integration in the baseline design 

Vitaliy's Talk

Richard's Talk



Breakpoint 2 – We are here




Break Point 2 Mid 2015 –

- **basic technology demonstrated to be acceptable**
- **Foundries selected, architecture selected**
- **Layout and performance found to be compatible**
- **Requirements Established**
- **Resources for phase-II identified**



Phase 2

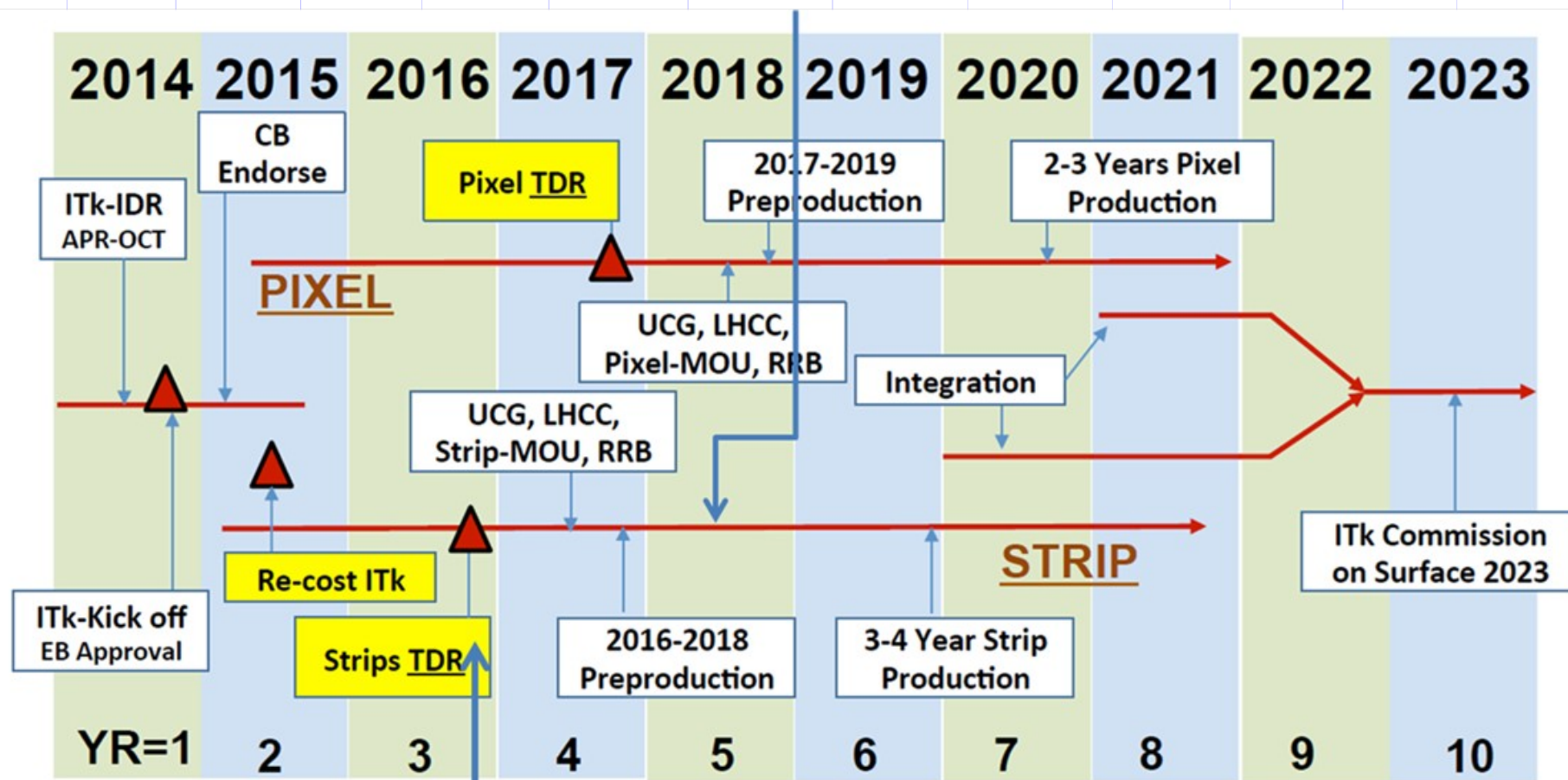
- Goal :Large size Sensor and ABCn' demonstrated
 - Large scale sensor with close to full functionality fabricated
 - Bulk and Surface Radiation hardness evaluated
 - Pixel fully characterized
 - Boundary electronics architecture tested
 - Mechanics
 - Any substantive changes required in mechanics evaluated
 - Test parts fabricate for any essential new elements
 - Consideration given to service module alterations.
 - Service tapes redesigned to accommodate new module configurations
 - ABCn'
 - ABCn' designed and test chips fabricated in multi-project run
 - Hybrid designed
- 
- Jens' Talk



Phase 3

- Goal : Full sized multi-sensor object demonstrated & Feasibility of use evaluated
- ABCn'
 - Tested with sensor prototypes from phase II
 - Fabricated in significant quantities
 - Optional: ABCn'' designed and fabricated in multi-project run
- Sensor
 - Full scale sensors designed and fabricated and characterized
 - Sensors and ABCn'' operated in module-like configuration
 - >1 module operated together on a service tape
- Mechanics
 - Changes to accommodate new layout and stave/petal designed
 - Assembly protocols and series production planning considered

Overall ATLAS Timeline



For strip CMOS to be plausible there needs to be good to compelling evidence that it has a good chance of being real by the time of the TDR – late 2016



Resources and Effort

- For year 1
 - Dedicated group of people with fractions of their time
 - Many things happened “in spare-time”
 - But: Already had dedicated “New Effort” for Chip design
 - Secured the necessary funds for chip submissions and support electronics
- For year 2
 - Already secured funds for first large chip submission
 - First estimate of resources made

Submission Costs

Strip CMOS Submission Costs

