# Results from 1st year of strip CMOS program

Vitaliy Fadeyev
SCIPP / UCSC

Work of Strip CMOS collaboration: Argonne National Laboratory, Cambridge University, Deutsches Elektronen-Synchrotron, Jožef Stefan Institute, Ljubljana, Karlsruhe Institute of Technology, University of Oxford, Rutherford Appleton Laboratory, SLAC National Accelerator Laboratory, SUPA - School of Physics and Astronomy, University of Glasgow, Universite de Genève, University of California Santa Cruz, Santa Cruz Institute for Particle Physics (SCIPP), University College, London, University of Liverpool, University of Ljubljana.

Version-0 ("raw draft")

TO-DO:

- A picture of CHESS-1-TJ ?
- Add several graphs
- Add simulations: Julie, Lingxin

# Chip Submissions

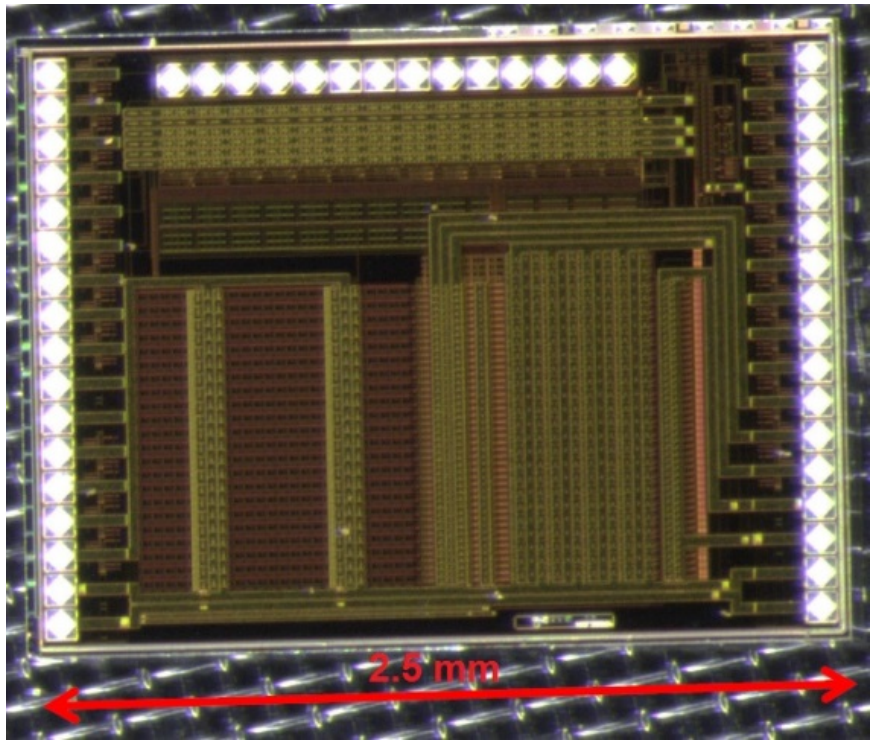
In the 1st year we had 3 chip submissions:

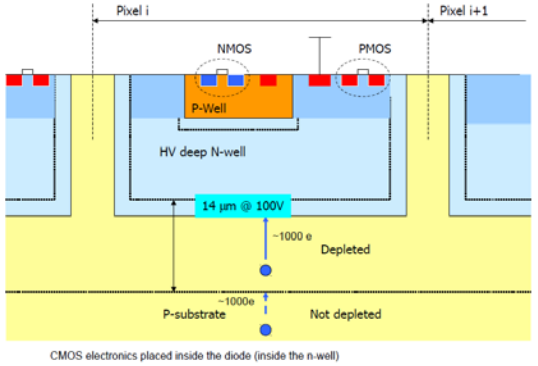
- HVStripV1
  - The chip was designed by I. Peric (KIT) to start investigations relevant for strip CMOS project.
  - AMS 350 nm technology, MPW run.
  - Received in July 2014.
- CHESS-1-AMS
  - The chip has been designed by H. Grabas (UCSC) in consultation with I. Peric.
  - AMS 350 nm technology (same technology node as HVStripV1 chip), MPW run.
  - Received in November 2014.
- CHESS-1-TJ
  - The chip was designed by D. Dipayan and R. Turchetta (STFC-RAL).
  - TowerJazz HR-CMOS 180 nm technology, Engineering Run.
  - Received in April 2015.

# HVStripV1

The chip contains:

- 22x2 array of active pixels with size of 40x400 $\mu m^2$.
  - There are discriminators and a digital readout scheme.
  - There is feedback variation in amplifier feedback:
    - std linear transistors
    - Enclosed transistor
- Pixel test structures with analogue readout.
- Three MOSFET structures (NMOS-linear, NMOS-enclosed and PMOS-linear) with drain connections.




CMOS electronics placed inside the diode (inside the n-well)

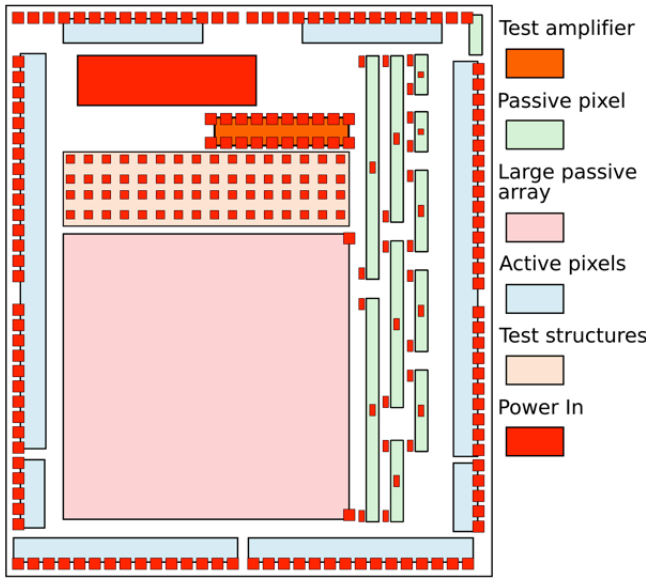
# CHESS-1-AMS

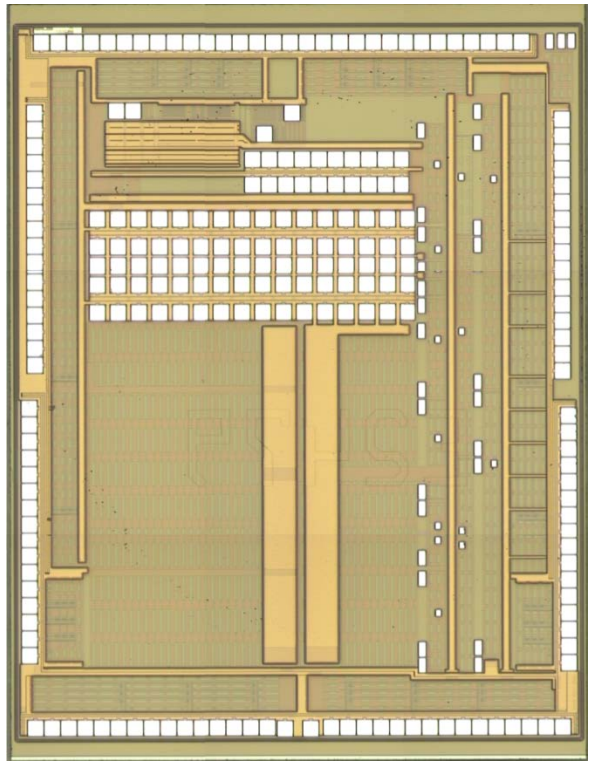
Same strategy of implementing amplifiers inside the collecting n-well was followed as for HVStripV1.

Design rules for 120 V bias were used.

The chip contains:

- Passive pixel structures
  - Length between 100 and 800 μm.
  - 30% and 50% active area fractions.
  - Mostly with guard rings; 1 structure without guard rings.
  - One structure near the ends for edge-TCT study.
  - One large array of 2 x 2 $mm^2$ .
- Active pixel structures.
- Isolated amplifiers.
- Transistors, Rs and C.



# CHESS-1-TJ

TJ HR-CMOS 180 nm features a high-resistivity epi layer grown on a substrate. The collecting wells are n-type and the epi is p-type.

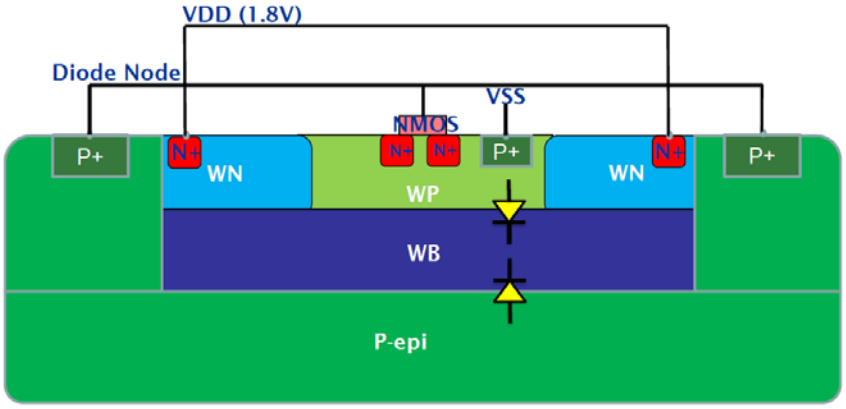
Design variations:

- p- and n- type substrates are being investigated.
- Epi thickness varies between 5 μm and 25 μm.
- Number and topology of the collecting n-wells.

The electronics design features the amplifier designed in the middle of the pixel area, separated from the collecting n-wells in the corners → small values of input capacitance.

The chip contains:

- Passive pixel arrays
- Active pixel arrays
- Transistor test structures



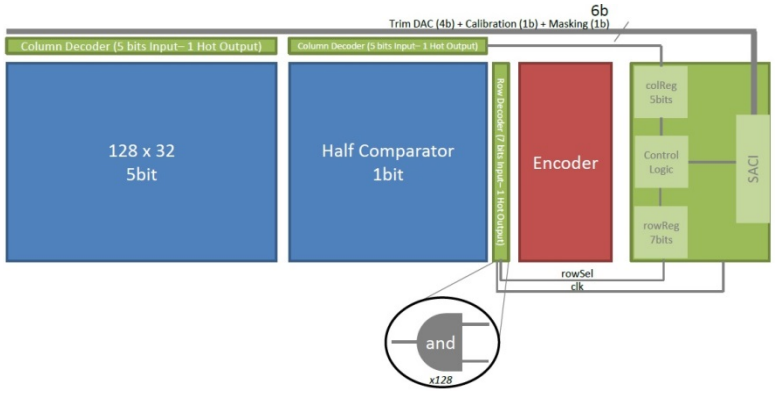

WN: Shallow N-well
WB: Deep N-well (~3μm)
WP: P-well

Two back to back diodes form between WP-WB and WB-Pepi!!

# CHESS-2-AMS

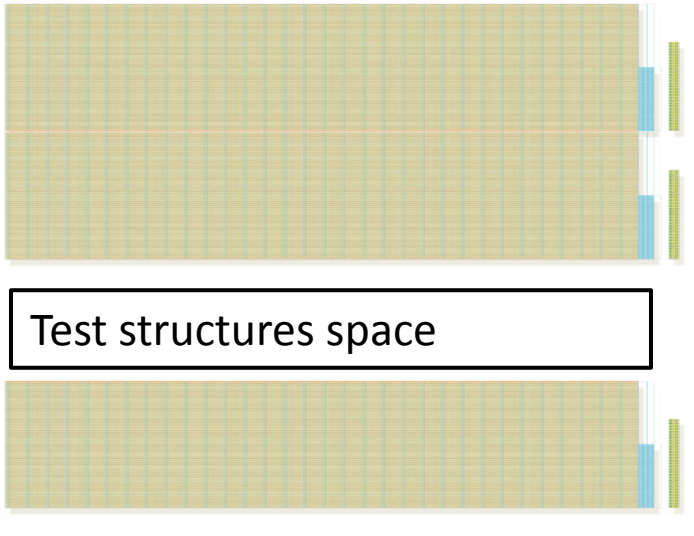
Goals:

- Readout architecture capable of processing large number of channels with single-bunch timing resolution.
- High-speed I/O bus streaming hit information in a synchronous way from a large pixel area. Small number of I/O channels to help with the wire bonding as the limiting factor on the construction speed.
- To test for possible correlated noise effects.
- To investigate higher substrate resistivities as a boost for S/N.




Will include 3 arrays of 127 strips (strip = 32 pixels), and multiple test structures:

- Passive pixels
- Edge-TCT structure
- Large passive array
- Transitors
- Latch-up
- LVDS transciever
- HV switch

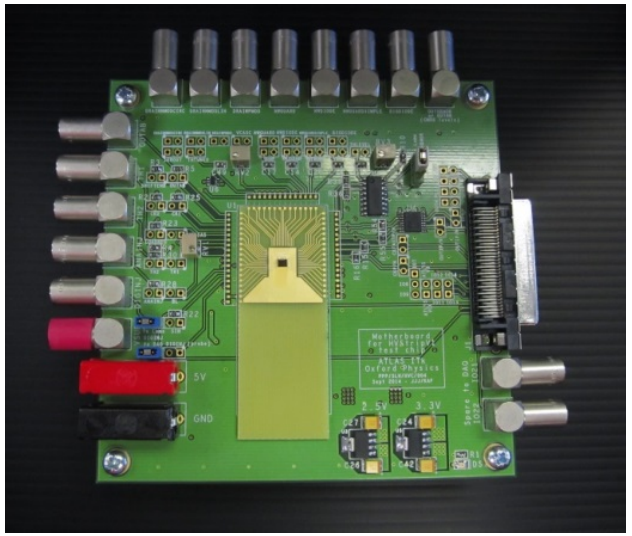


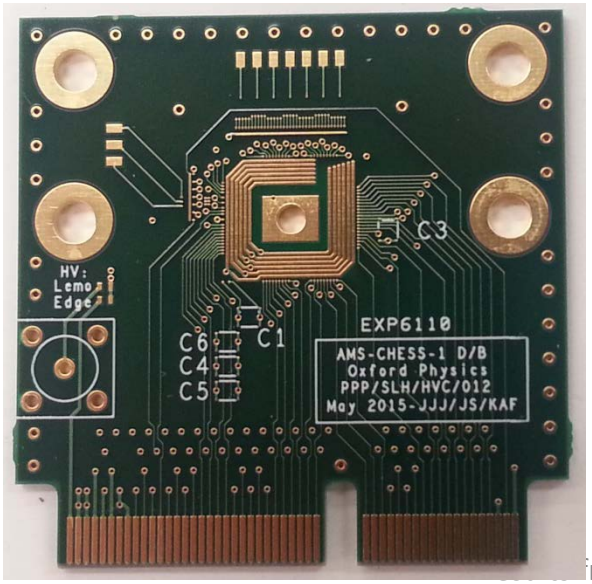

The design is well progressed. Had 2 design reviews:
https://indico.desy.de/conferenceDisplay.py?confId=12358
https://indico.desy.de/conferenceDisplay.py?confId=12685

# Support Electronics

Readout systems for the chips followed motherboard/daughterboard separation:

- For HVStripV1 Atlys FPGA board was adapated for readout digital signals.
- For CHESS-1 chips readout is analog, but there is high-density layout (> 100 signals)




Oxford, UCL

# Irradiations

The maximal radiation level expected in the ATLAS strip tracker is $1.6 \times 10^{15}$ neq/cm$^2$ and 60 Mrad.

Several irradiation campaigns:

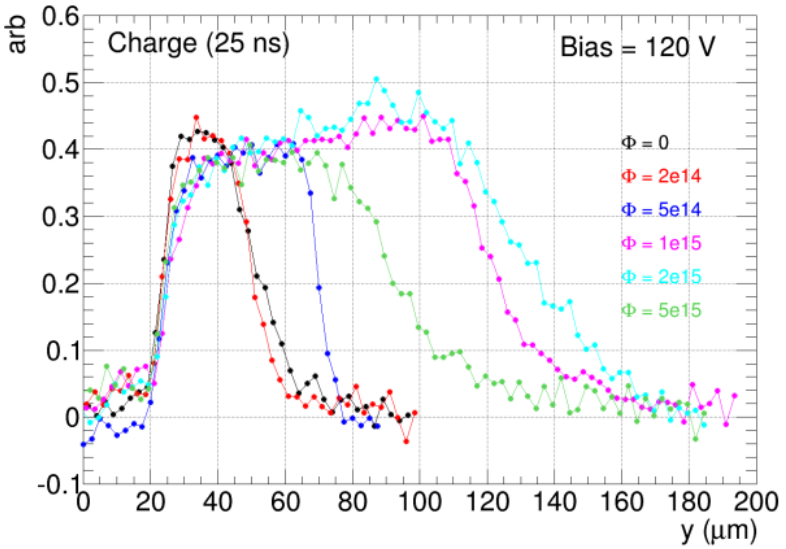
- Neutrons in Ljubljana up to $5 \times 10^{15}$ neq/cm$^2$ (CHESS-1-AMS)
- Gammas at Sandia between 1 and 100 Mrad (CHESS-1-AMS)
- Gammas between 0 and 60 Mrad (HVStripV1)
- 27 MeV protons in Birmingham to $> 5 \times 10^{15}$ neq/cm$^2$ (HVStripV1)
- Planned CERN PS protons (24 GeV)

# Edge-TCT Measurements

Insight into fields and depletion

Specialized edge structure.

See initial growth of depletion with fluence.




Ljubljana

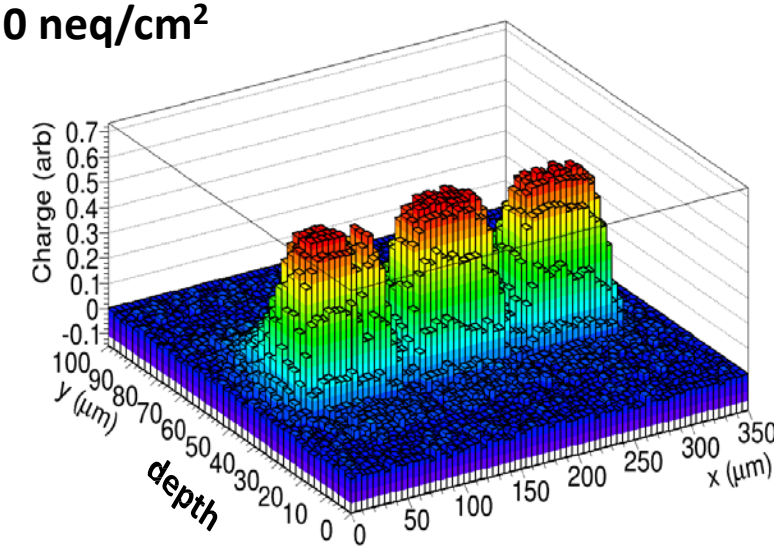
Add more plots ?, pix

# Edge-TCT, Cont

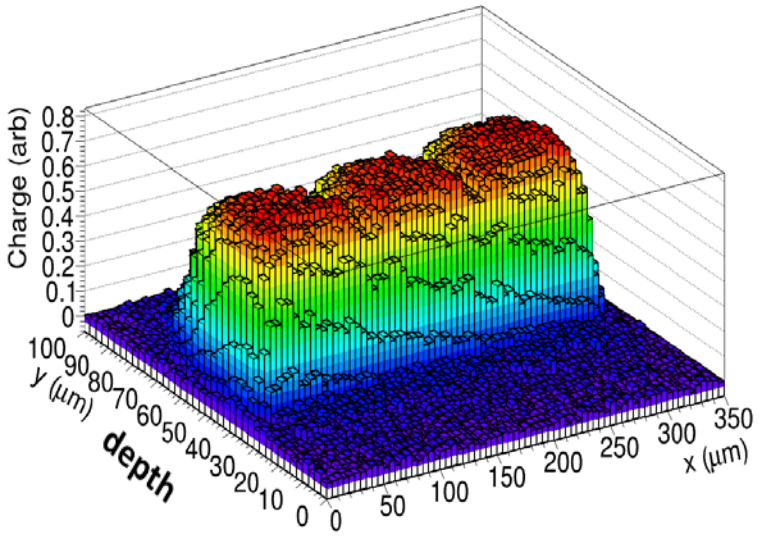
Scan of depth and pixel length:

- Initial gaps of acceptance/signal
- Disappear with fluence, consistent with higher depletion

$\Phi$ = **0 neq/cm²**



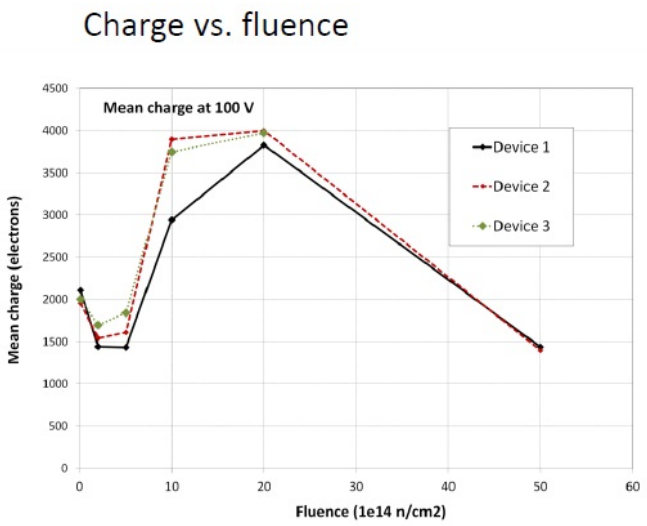

$\Phi$ = **5x10¹⁴ neq/cm²**




Ljubljana

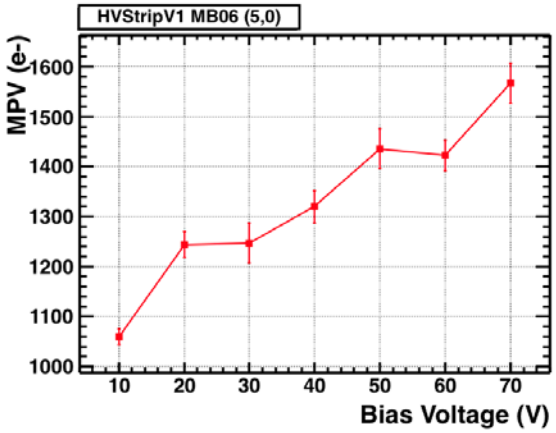
# Charge Collection

A lot of results with large passive pixel array on CHESS-1




Ljubljana

Add more plots



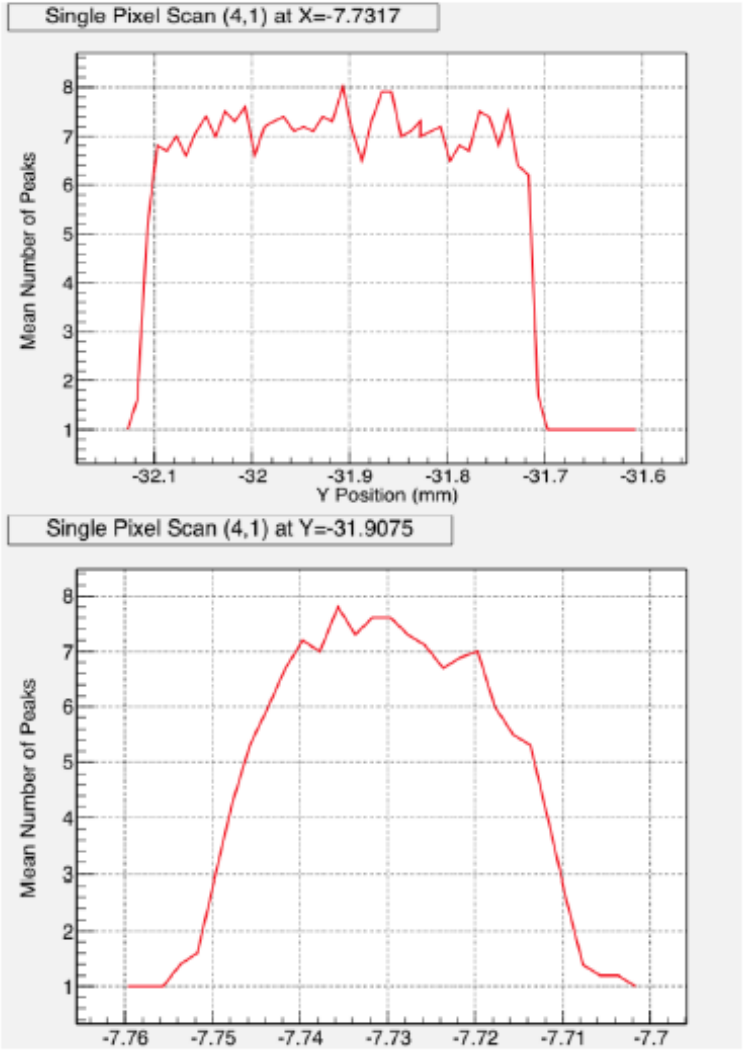

Glasgow

# Beam Tests

Beam tests are not easy due to a) small active areas used, b) small pixel dimensions.

Feasibility has been demonstrated with HVStripV1 chips:

- Micro-focused X-ray facility (Diamond Light Source). Observed pixel dimensions (pix).
- Initial tests were done at the DESY-II Test Beam Facility using electron beams from 3-5.5 GeV.
- Further tests are being planned both at DESY and possibly CERN.

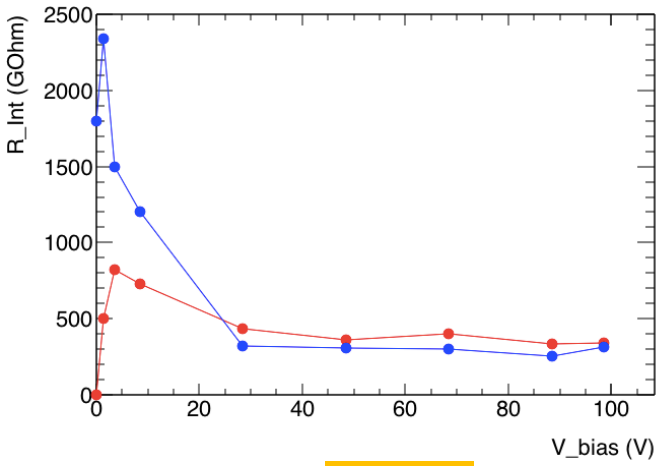



RAL, Oxford, Glasgow, DESY

# Passive Pixel Properties

We've measured several properties of passive pixels:

- Capacitances
- Inter-pixel isolation
- Breakdown voltages

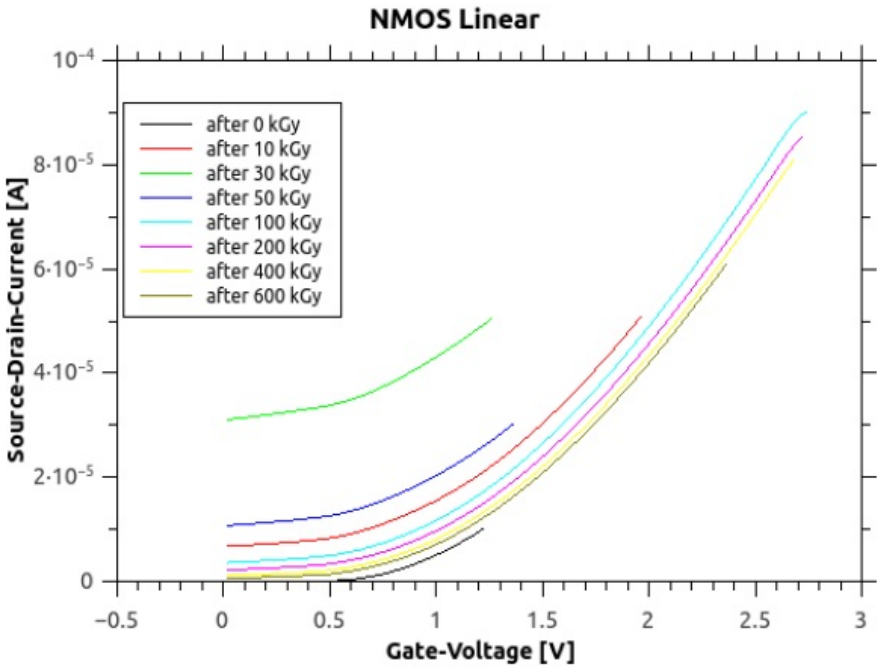


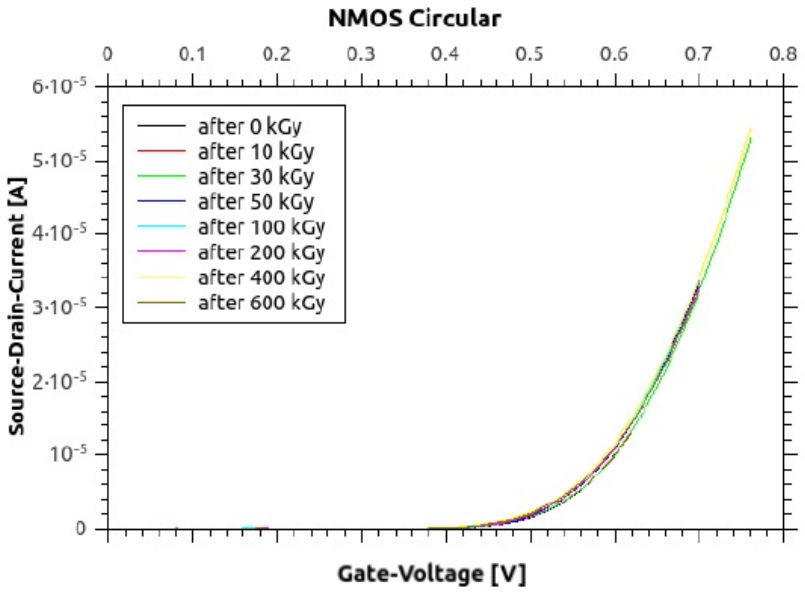

SCIPP

Add C-meas plots

# Transistors

Transistors have been looked as a function of ionizing dose (with gammas). As expected, the enclosed transistors are much more immune to the dose.

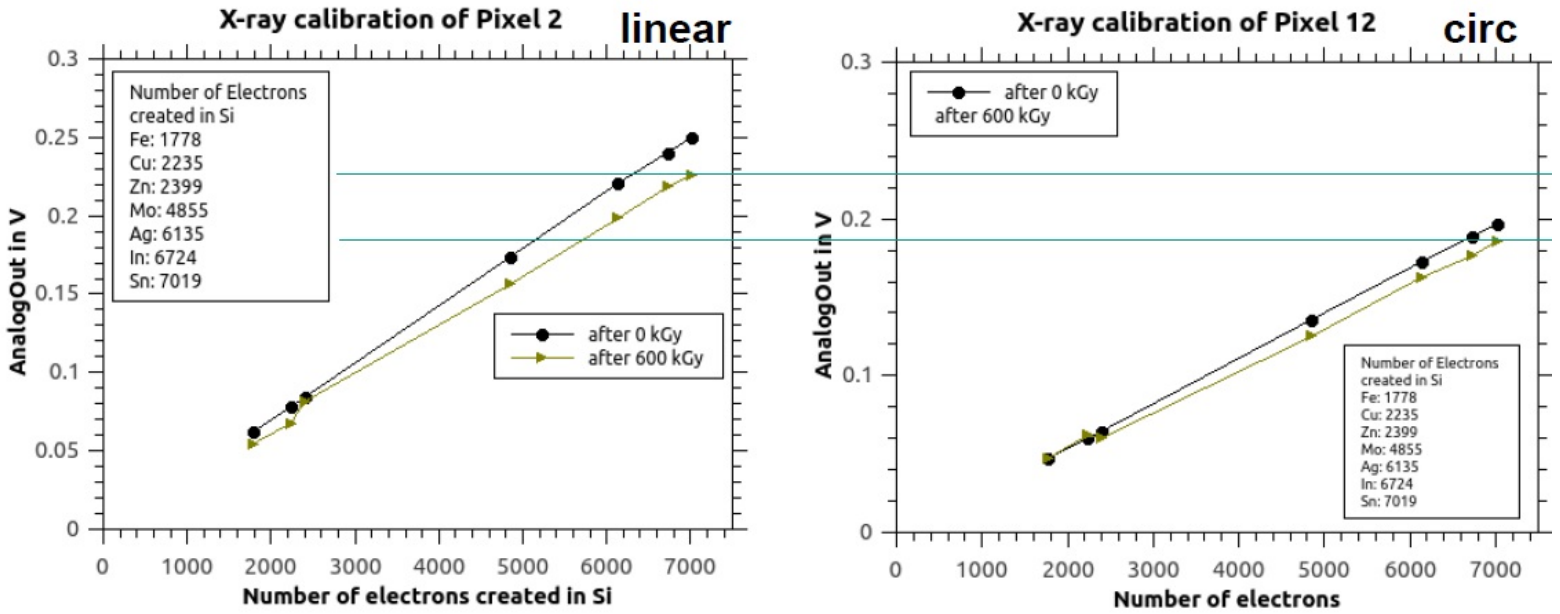



KIT

# Amplifier Gain

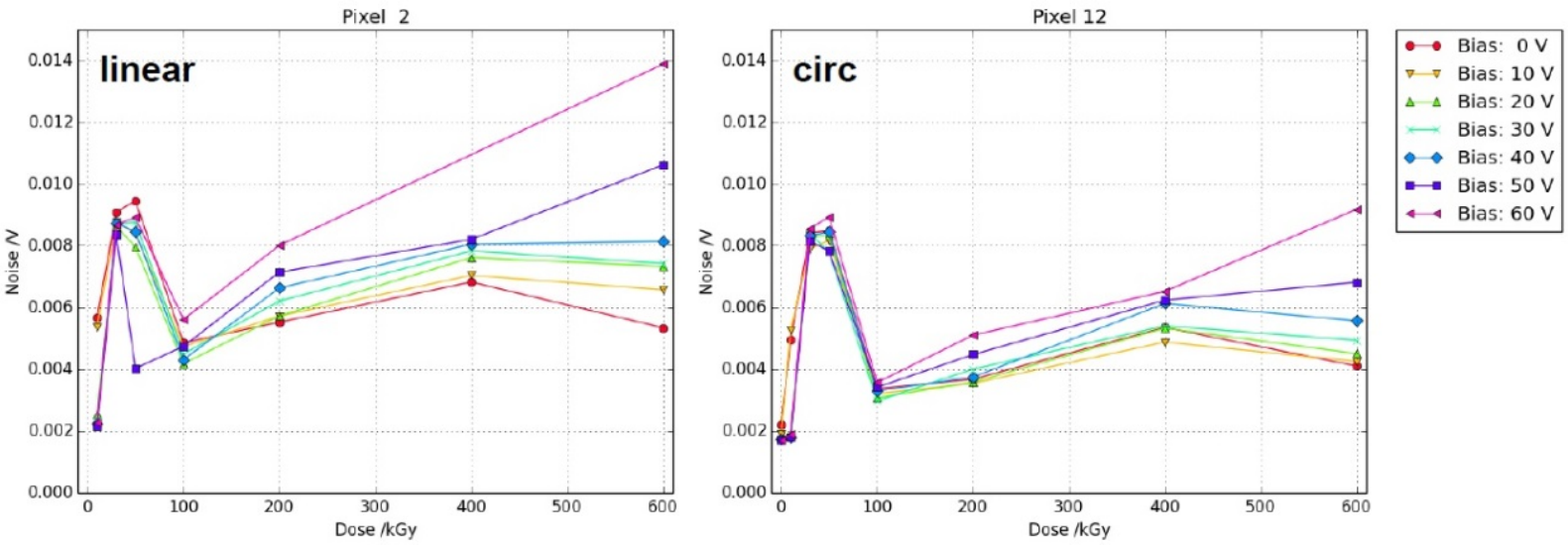
Amplifiers on the HVStripV1 chip have been calibrated with different x-ray sources. They show quite linear behavior. The variation with dose is relatively small.




KIT

# Amplifier Noise

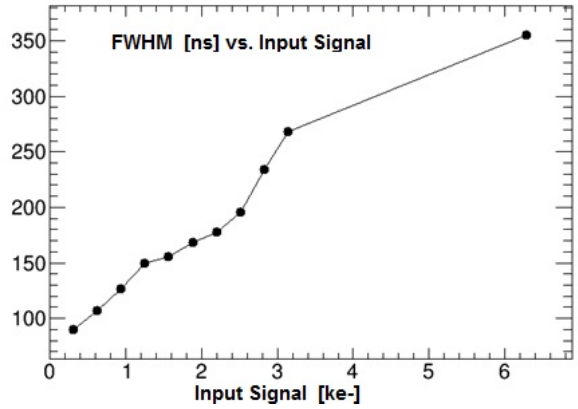
Amplifier noise was studied as a function of dose as well.
There is a peak at ~5 Mrad, that deserves further attention.




KIT

# Amplifier Timing Properties

We looked at amplifier timing properties: rise time, pulse width.




SCIPP

Add more plots

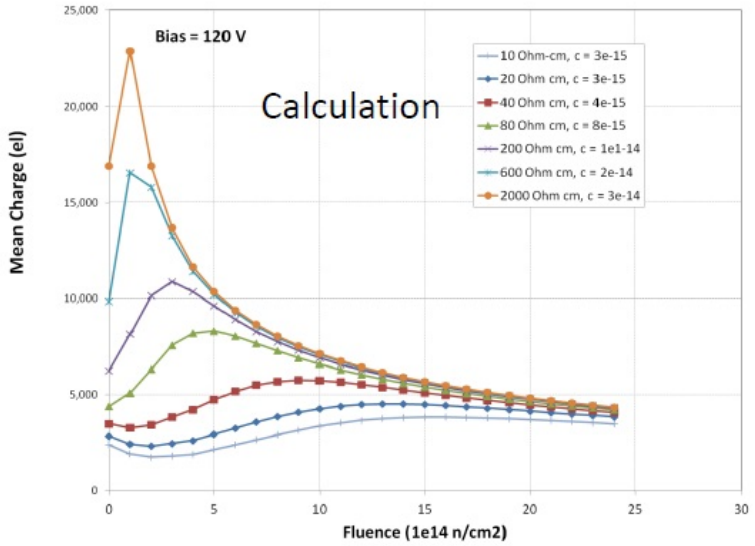
# Optimal Resistivity

In HV-CMOS, we have worked with 20 Ωcm resistivity so far. This is very far from the standard (well studied) > 3000 Ωcm values.

Our projections indicate optimal region between 80 and 600 Ωcm based on charge collection estimates and field properties with top-level biasing.

Of course, this needs to be studied, which is one of the goals for CHESS-2-AMS.

Add field pix




Ljubljana

| r | Depletion |
|---|---|
| [W*cm] | [mm] |
| 10 | 11 |
| 20 | 15 |
| 40 | 22 |
| 80 | 31 |
| 200 | 49 |
| 600 | 85 |
| 2000 | 154 |

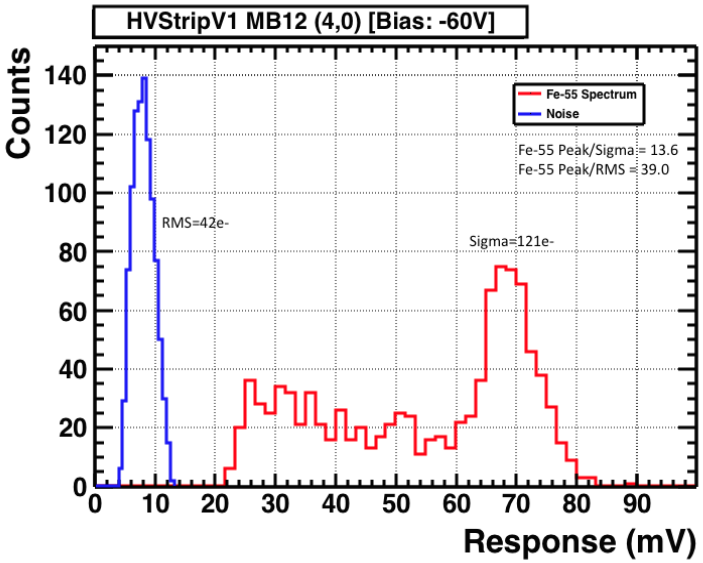
# S/N

The most direct inference in the S/N was obtained with Fe-55 measurements on HVStripV1. We see indications of S/N of 13 for noise of ~100 e-.

There are expectations of:

- Amplifier noise growth by x3 with dose.
- Signal grown by x3 with higher initial resistivity.

=> S/N of 13 may be a realistic factor unless we see common-mode noise.




Glasgow

# Summary of Findings

- Stable amplifier gain (less than 10% variation).
- Pre-rad noise of 100 e-. It does depend on dose, rising by x3.
- Signal (CCE) dependence on fluence is non-monotonic. The minimal value for initial 20 Ωcm is 1500 e-.
- Higher initial resistivity should help with boosting the initial signal significantly, likely by x3, as well as maintaining uniform acceptance.
- Inter-pixel isolation is very high due to process features.
- There is a preference for using pixels with high active area fraction.

# Backup