Integration of CMOS sensors into the detector

- Sensors are one element of the tacker, the other components also require years of R and D to optimise.
- This cannot be undertaken, so vital to understand that any alternative sensor can be used with the already planned supporting systems.
- There is some interaction between sensor/ASIC design and the module/stave/petal into which they are integrated. Electrical stability of system is not assured by stability of sensor.
- Rely very heavily on lessons from planar work.

First year of the programme called for

"Furthermore, the impact on the physics is to be evaluated and the integration in the baseline design needs to be studied."

The main effort on understanding integration into the mechanics comes in year-2

However it is important to ensure that the direction taken is consistent with being able to use the sensor in the detector

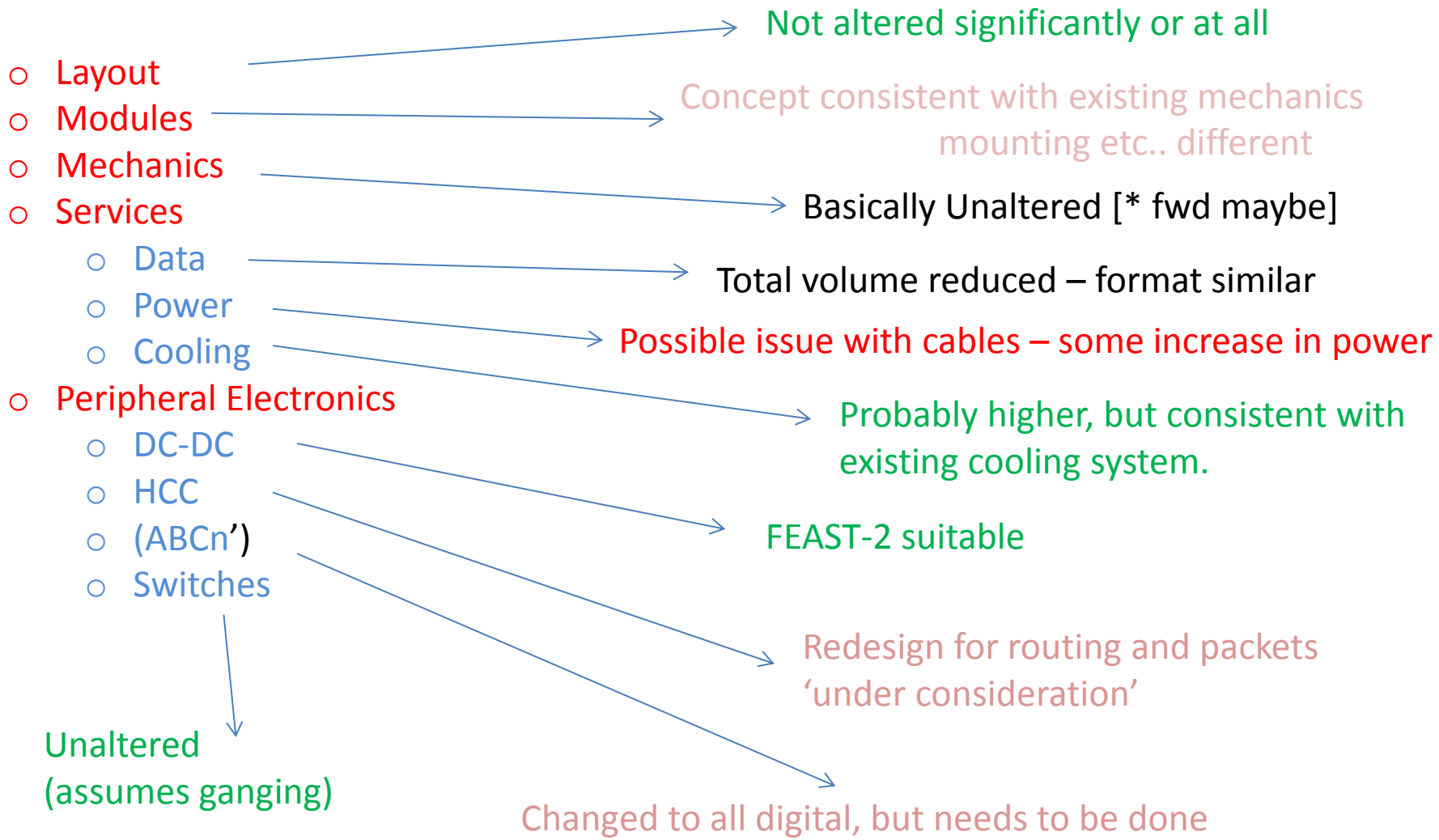
- Layout
- Modules
- Mechanics
- Services
  - Data
  - Power
  - Cooling
- Peripheral Electronics
  - DC-DC
  - HCT
  - (ABCn')
  - HV Switches

Physics impact has not been evaluated explicitly.
CMOS sensor system has better parameters and this is taken to mean that the physics is not degraded, and may be improved.
(X0, point sigma, …)

Parameter	Planar Sensor	StripCMOS Sensor
r-ϕ resolution	20 μm – 23 μm	11 μm
z-resolution	850 μm	280 μm
Two hit resolution in r-ϕ	160 μm-240 μm	80 μm
z-element length	2.5 cm	720 μm (2.4 cm / strip)
Fraction of two hit clusters	15% - 20%	2%-3%
Geometry inefficiency on stave	~0.7%	~1%
Radiation Lengths per stave	1.8%	1%
Insensitive crossings after a hit	1 BC	0.3 BC (1/32 of strip is dead for 10 bunch crossings)
Number of Signal Wire bonds	O(5100)	O(1100)

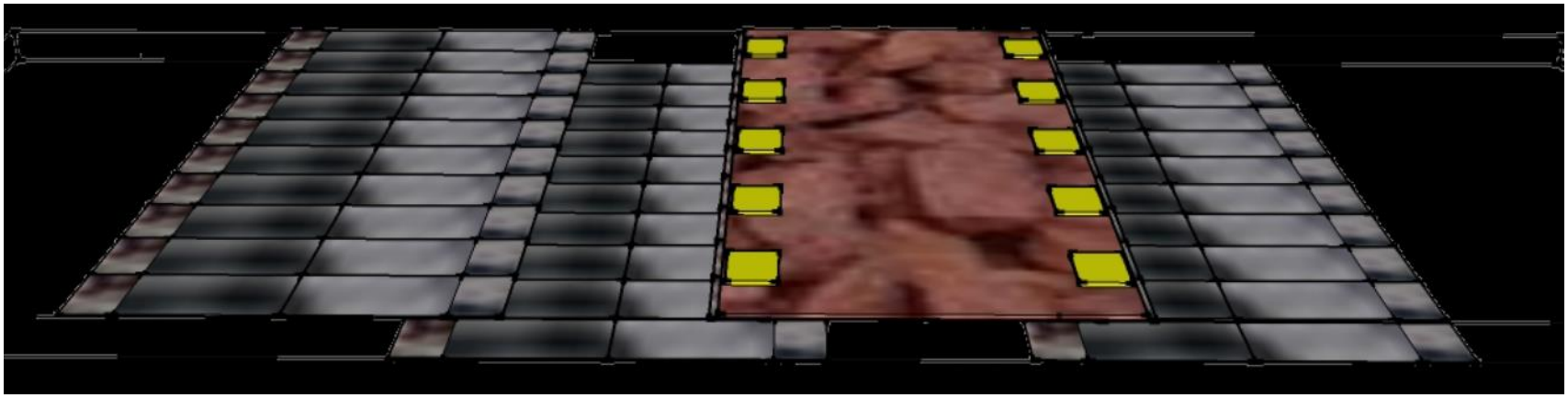
Planar values are mostly measured or engineering values
StripCMOS values are estimates. Assumptions are listed in the 'layout document'.

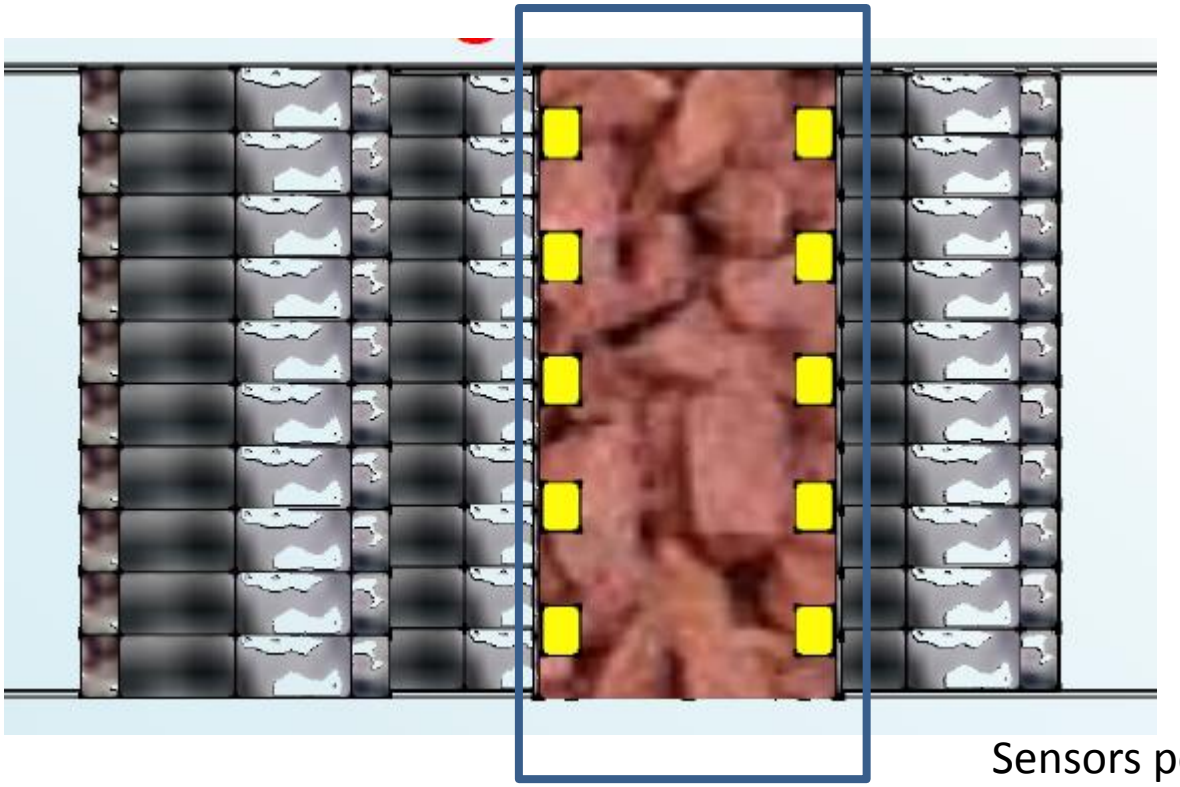
Note that recent study showed a fifth pixel layer improved fake rate by 25%
These strip sensors are close to being pixel-like in resolution at 40x720μm.



By construction, major issues of layout, support mechanics and peripheral electronics are rendered tractable by designing to use existing planar systems

Module Concept - Barrel



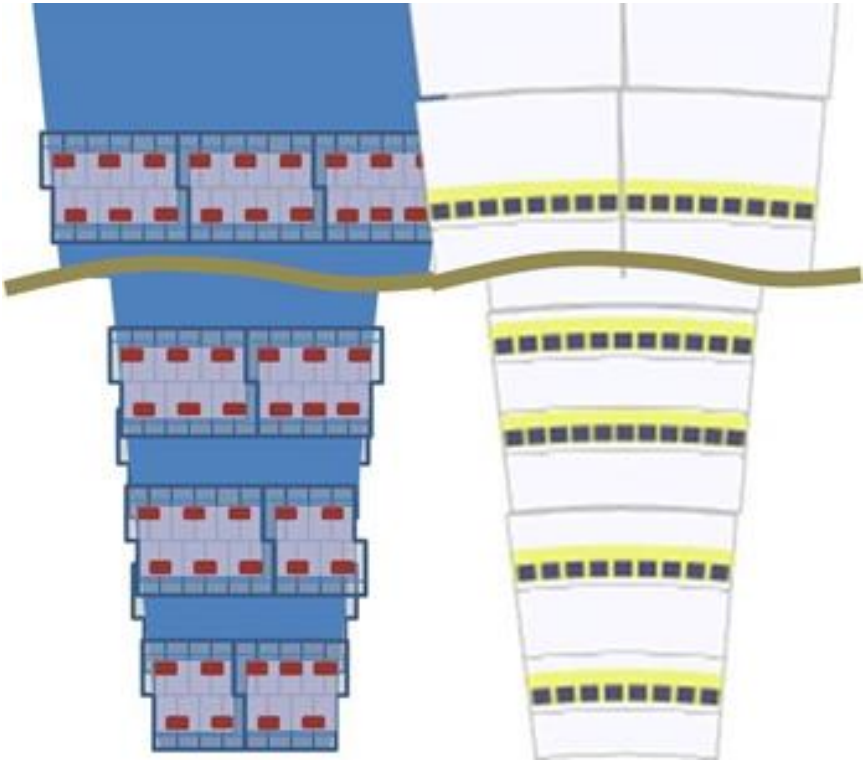


Barrel module

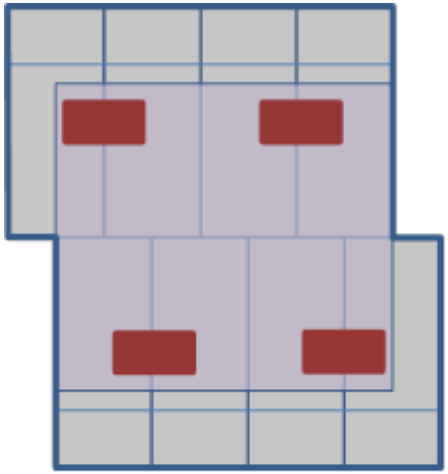
- 10cm x (2 x 2.1) active area
- Sensors in ‘blocks’ of reticules
- Single hybrid
  - ✓ 10 ABCn’
  - ✓ HCC
  - ✓ DC/DC convertor
  - ✓ Mechanical support

Sensors possibly with duplicate pad sets

Module Concept - Forward



Barrel module is a special
case of a forward module (10-10)



A 4-4 module
2 x 4 reticule blocks

Final Details of sensor dimensions,
Strip pitch, dicing blocks
fixed by overall mechanical considerations forward+barrel in year-2 of programme

DC-DC convertors

Engineer suggested that re-laying out the geometry would be the design task and that FEAST2 is already capable of supplying the current and voltage needed for the electronics in a CMOS sensor + ABCn'. [but maybe multiple voltages, not evaluated]

HCC

This is being redesigned to allow L1 trigger. FA is aware of the possible different data payload with the CMOS system and is bearing it in mind during the redesign for the planar system.

Data

The data packets should be the same, but the payload different. An additional six bits per hit is required. However the total number of hits is reduced by about a factor of two. This because the probability of two hit clusters is higher in the planar design but clustering is employed to reduce the extra hit effect on data rates. Clustering is not planned for the stripCMOS system as two hit clusters are improbable. A net reduction in data rate is expected despite increased resolutions.

HV Switches

Largely unaltered, though wider range of materials could be used.

Major Mechanical/System Challenges

these are often schedule driven

Demonstrating large-scale electrical system stability
Detailed analysis of forward region mechanical implications
Total power consumption and power cables

Mechanical/System Challenges

Redesign of ASICs
Redesign of stave/petal tapes/EoS cards

First year goal was not to solve all the mechanical/system issues, but to consider if the design direction was at least consistent with a minimum impact scenario.

Claim is that this is the case.

Improbable that there is a design direction which could have less impact whilst retaining the potential advantages of stripCMOS