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CHESS program beyond the first year Review

Questions that a second year program should answer

TDR deadline

- With the ITK TDR being planned for late 2016/early 2017, we do not only have a project internal deadline for the second year review
  - The assumption is that we're not re-designing general infrastructure
- The Major goal will be demonstration of a full system concept before that:
  - Sensor
  - Readout circuitry
  - Integration into the current mechanical and electrical system (a full module)

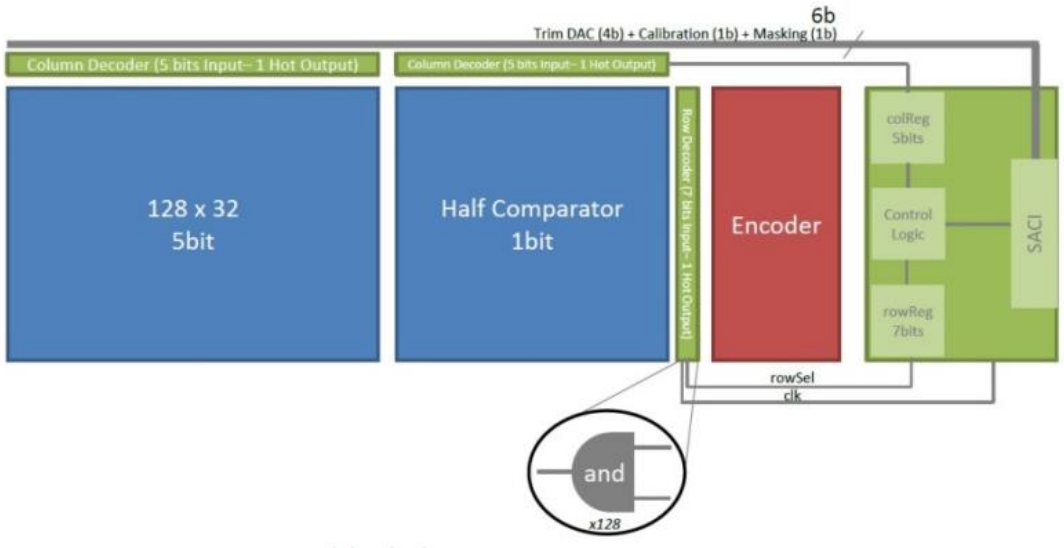
Deliverables for the next year review

- Process Decision:
  - Awaiting results from the first TowerJazz submission:
    - First results from low res test wafers look promising
    - High res. epitaxial layers are only expected back around end of August
    - Tests and irradiation will probably bring us to December
  - Next design iteration design ongoing
- A sizeable structure (CHESS-2) that is an active sensor with all components needed in a final submission:
  - CHESS-1 was purely focused on pixel responses, this one should be on system response
  - A chip that provides full processing:
    - Analog front-end (from CHESS-1, lessons learned to be integrated)
    - Discriminators
    - Hit processing
    - Digital readout
- Trigger, Command/Config and Readout Infrastructure:
  - An interface to the current
  - A processing strategy to feed the digital information into the ITK readout systems
    - Implies design of a buffer and timing circuit (ABCN' in the documentation)
- Module Assembly:
  - How do we arrive at a module sized object (10xXcm) to be integrated mechanically?

Status of HV/HR

- Many tests still awaited from the HR side
  - Only 5um, 20Ohm/cm PonP has been delivered so far, not useful for particle physics, but gives us the option to verify the metal in the submission is correct
  - Tests show the structures do work (amplifiers with injection, Laser injection in active sensor), hence we're expecting good results from the actual HR wafers
    - After go ahead, takes another month to be delivered, including safety factors possibly end of August, early September (We're not the only project in this submission)
- A fair comparison of the two technologies will probably only be possible in December/January this year
  - HV CHESS shows very good results, hence the submission for CHESS-2 in AMS will continue as early as possibly
  - HR CHESS 2 will be prepared for submission, so as to be ready for submission when results are available from the first round
    - Funding for the Designer is external (STFC CFI)

CHESS-2



- Both HV- and HR-designers are preparing a second round submission:
  - All features of a full sensor to be integrated
  - Large chip (approximating a full reticule)
- Should provide a structure that can be run in testbeams early 2016
  - Allows measurement of on-track resolution, efficiency, timewalk…
- Possibly basis of a first conceptual “module”

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CHESS-2 Status and plans

- Status:
  - …
  - …
  - +…
- Testbeams
  - Pre and post irradiation
- Module prototyping
  - Integrate with HCC close by
  - Demonstrate handling of CMOS sensors to build a large object (10 x X cm)

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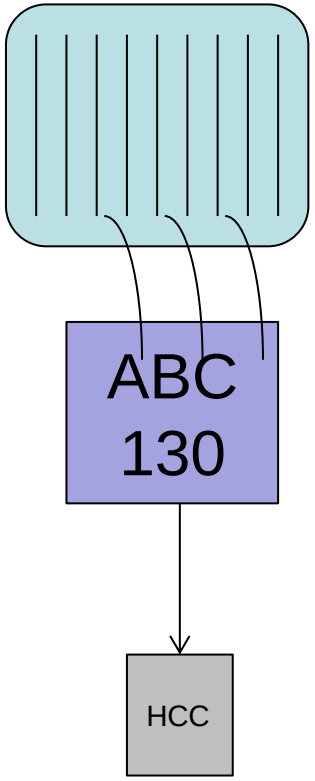
ABCN’

- Classic Architecture does all processing in ABC130(*)
- CMOS sensor will spill out hits every 25ns with known propagation delay
  - No timing information
  - Triggerless
- HCC needs data to come “as if” an ABC were talking, otherwise too much effort in two individual dataflow designs



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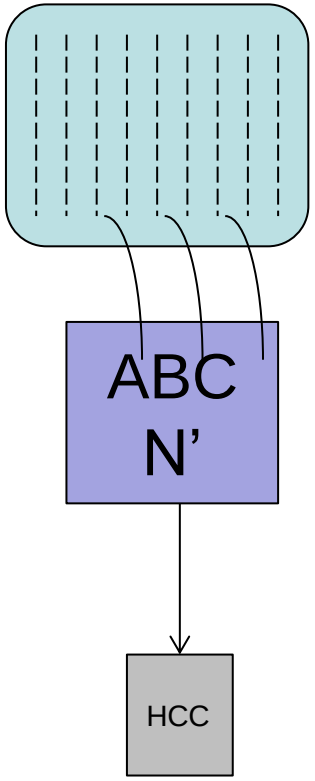
ABCN’

- ABCN’ supporting the CMOS readout by:
  - Buffering incoming hits for the trigger latency
  - Trigger Processing
  - Receiving configuration and command from the HCC and sending out the corresponding format for the CMOS sensor (SACI)
- Circuit is, in a first approach, laid out with HDL (for an FPGA), to then be translated into a VLSI circuit
  - TMR/ECC should easily deliver SEU tolerance for the configuration storage (trigger latency, configuration values for sensor)
  - Feature size can be much smaller than sensor feature size, hence memory will not occupy too much area
- All logic for the ABCN’ exists (to first Order), hence the design effort should be low (memory, output buffer and serialiser, command and trigger input interface, SACI Master)
  - Input de-serialiser to be done for the format delivered by CHESS-2 sensors



Person power estimate

- 11 FTEs spread across the project

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Summary

- Finish up the comparison between HR- and HV-CMOS (Results by end of this year)
- Submit a large chip with full functionality for:
  - Testbeams
  - Module prototyping
- Implement a concept (FPGA->VLSI ASIC) for readout of CMOS through the current infrastructure (HCC)

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What's missing

- Simulation input
  - A 10 hits-in-strips argument keeps popping up, but is that based on a strip architecture and would actually be half for a pixelised detector?
  - What is the maximum number of dense hits we have to cope with per Bunch Crossing?