- What is input capacitance? How was estimated/measured?

The input (detector?) capacitance depends of the high voltage applied as well as the substrate resistivity.

It has been measure on CHESS1 for a 800x45µm pixels. The pixels in CHESS2 will be smaller ~700µm x 40µm.

It was measured on CHESS1 to be ~400fF.

- What is size of AC pixel capacitor size (and feedback)?

The AC pixel capacitor is 435fF.

The feedback capacitor post extraction is ~2.5fF



- What is rise time behind 1/2 pixel comparator with all capacitance (worst/best case)?

The ½ comparator sends a current to the periphery. The rise time after the other ½ comparator is ~4ns. Best and worse case needs to be determined.

- Why multiple wells for single pixel (it will increase capacitance)?

Interpixel capacitance between wells is only due to capacitance to the p-contact between NWELLs. In the end a big NWELL or small one should not make big difference

- Are all periphery isolated from sensor (in deep-n)?

Yes all the periphery is in a deep n-well

- Is there power/ground split matrix/periphery?

Yes

- What is within chip clock spread (25ns)?

To be determine when we do the clock tree.

- Is full chip (post-ext) simulation done?

It is not possible to extract a full chip and do the simulation (just too many components to simulate.

However, the plan is to do full chip pre-extraction simulation and have individual block post extraction simulated.

- Do you expect any problems with power drooping ?

Short answer: No. Needs more simulations. Worse case 10mV

There are no dynamic power consumption in the pixel except during RAM configuration. For that reason, full matrix RAM configuration could be an issue that the designers don’t plan to address in this submission (full Row and full Column configuration being possible).

The typical current consumption in the pixel is ~20µA. That is a consumption of 32\*20=640µA per strip. The resistance of the power distribution network for 1 strip is:31\*800µm/20µm = 1240◻

The metal resistance is 10Ohm/◻, therefore we expect a 8mV droop between the first and last pixel. The comparator design is

- (Giulio ?) Vdd difference along the readout trace and related power

supply rejection ratio.

- (Francis) What is the potential of the Nwells.

~3.3V resistive bias.

- (Francis) On the presentation of the SACI block there is a mention of “floating bus” :

If well controlled these floating lines may not be a problem Anyhow it should be very carefully simulated what are the consequences of the various possible states of these bus lines when they come back to be used (initial state dependence)

Answer:

We were referring to the data bus lines as floating when they are not driven by any gates and that can happen because the data bus lines are bidirectional. When this happens the state of the data bus lines is brought to 0V because we inserted a pulldown to avoid level uncertainty (for example when the ASIC turned on). We discussed also the floating data bus lines in the hit encoding and the proposed solution in order to avoid uncertainty was to reset the data bus lines every 25ns. We simulated this in all corner and the data bus are not able to move if not written in such short amount of time. In fact it moves worst case 5mV/100ns.

- (Marcel) If 4-bit trim DAC is sufficient.

We measured 2mV of fixed offset between far and close comparator.

Monte Carlo simulation of the comparator gives a 7.6mV sigma of dispersion = 38mV dispersion at 5sigma.

Let’s assume with both contributions a dispersion of 40mV on the thresholds. A 4bit DAC allows to divide that dispersion by 16: 2.5mV at 5sigma. We believe that is sufficient.

- (Mitch) Input offset in the receiver for LVDS driver.

We re-simulate the offset of the LVDS receiver that confirm the 3mV value given during the review meeting.

- (Francis) What makes rad-hard register radiation resistant

(enclosed transistors).

All the nMOS are enclosed and there is heavy use of guard rings in order to prevent latch-up. We are also using static flip flop that avoid high-z nodes making them more SEU tolerant.

- (Francis or Mitch) If the peripheral circuitry is placed in n-well.

Yes it is, each block is sitting in its own NWell (encoding of strips, encoding of hits, Registers, SACI control Unit.

- (Mitch) Temperature dependence of the comparator.

From -40 to 40deg deltaT = 5ns.