Interim Review of the ATLS-ITk-Strips CMOS project on Friday 10th July 2015

From 14:00 – 18:30 CET

The 4 reviewers were: P. Allport, I. Gregor, S. McMahon, P. Riedler (ALICE)

The material presented during the meeting can be found at:

https://indico.cern.ch/event/406791/

The reviewers would ask the Strips CMOS team to upload all of the supporting documentation to the INDICO page for others in the strip community to see.

Before doing that please add the names of: Weimin Song, Hongbo Zhu and Qinglei Xiu from the Institute of High Energy Physics in Beijing who have completed measurements on AMS HV test structures at RAL. Please also update the world map that shows the location of participating institutes

Please also note that there is an error which occurs at several points in the presentation and submitted documentation. The Z resolution of the CMOS sensor would be 208μm not 280μm.

Introduction

The review is one of a set of break points throughout the project at one year intervals to see if work is progressing well and could possibly be used as a technology for the strip detector for the ITk. The reviewers were looking at the technical developments and results, the demonstration of the possible performance enhancements that could come with CMOS, preparation for scaling the technology to the full detector (including the required resources), the progress on the development of a strip module, a clear understanding of the timeline and how the CMOS program fits in to the overall strip program and how it interrupts the production of planar modules.

Executive Summary

The referees would like to congratulate the CMOS-strips team for the supporting documentation prepared and circulated ahead of the review and their clear presentations and answers to questions during the review. It is

noted that the team has made very significant progress in the last year, they have developed a considerable momentum within their collaboration and have answered many or most of the criteria required to progress to the next year. The reviewers would encourage the CMOS team to continue their investigations and to strive to meet the goals set out for the second year of the program.

However, the reviewers noted with some concern that there are a number of significant challenges in the second year. Some of these challenges require considerable resources (money and manpower) to satisfy the goals as presented in the review. Some of these resources are scarce and in some cases the required expertise is outside the skill-set of the team as it is constituted today. We would encourage the team to work with ITk and Strips management to try and identify the resources required to complete the second year of the program.

In more detail

1. **General Comments on the AMS and TJ developments.**
    - The results the Strips-CMOS team are seeing with the AMS-350nm process (HVStripV1 and CHESS1-AMS) are looking very promising as a candidate technology for the ITk-strip detector.
    - The referees would like to see more understanding of the evolution of both the signal and amplifier noise as a function of TID and eventually hadron irradiation.
    - When these evolutions are understood the team need to be able demonstrate a good signal-to-noise for the strip tracker at the end of the life of the HL-LHC. The required signal-to-noise should be set out in a requirements document for the CMOS strip module.
    - The reviewers would encourage the team to present the results on signal-to-noise for MIPS up to the maximum available bias voltage.
    - If they are submitting the CHESS-2 design soon, the reviewers recommend getting pad wafers to aid the mechanical developments.

- The reviewers would encourage the team to use the existing radiation damage models to see if they can predict the reductions in acceptor concentration that they seem to observe in their data.
- The reviewers would encourage the team to choose a sensor thickness that would take optimal advantage of the acceptor reduction after irradiation.

- The reviewers were disappointed that there were no results from the CHESS1-TJ chip presented at the review but do encourage them to continue with this development.
- There were concerns at the assertions of the CMOS team that the TJ results will be understood at the same level by the end of the year. The reviewers would like to understand this timeline as soon as possible.
- Having a second (and complementary) process could help understand the evolution of both signal and noise with irradiation. A second vendor will significantly reduce risks and therefore increase the chances that at the end of the process there will be a viable alternative to the planar solution.

2. Strip Modules

- The reviewers would encourage the team to write a set of requirements for the strip modules that would be used in a CMOS tracker. We would urge the team to prepare these requirements with the highest priority and share them with the broader strip community. This will help focus the team on the task ahead.
- It will be important to understand the power consumption of such a module
- The reviewers would like to see a more complete plan for the development of the ABCN that would be used if CMOS were to be adopted as a solution for the strip tracker. The plan should include identified resources, costs and a timeline. *It should be stressed that developments of TSMC 65nm technology for the existing planar*

solution currently have a higher priority on the existing resources than CMOS developments.

- The reviewers asked the team to consider the following
    - Can the existing ABCN be used to accelerate the process?
    - Are there other chips with similar functionality that might be used for this development?
- At the next review the reviewers would like to receive more information on how CMOS strip modules would be assembled.
    - The total number of modules to be produced for the latest layout.
    - Does the module have multiple reticule size objects joined together or are they relying on larger structures? Building a strip tracker from reticule size objects is never going to work. The referees would like to see this discussed in the module requirements document.
- The reviewers would like to see more information on how the parts will be diced and picked. Have they considered thicker structures that would increase the yield and ease the module construction?

3. Physics simulations

- The reviewers believe it is mandatory to start physics & performance simulations with CMOS strip modules in a realistic ITk layout. It will be important to understand tracking efficiencies/inefficiencies and fake rates in a tracking system with a strip system that provides space points from a single sided module. The results should be compared to the requirements as set out in the ITk High Level requirements document. (ATL-COM-UPGRADE-2015-015). https://cds.cern.ch/record/2025549
- The team should consult with ITk management and the simulation and performance team about the availability of simulation experts.

4. Project timeline and deliverables

- Before the next review the reviewers would like to see more information on how the CMOS project would interrupt or stop the production of planar strip modules.

- As the current CMOS program will not conclude before the currently expected ITk strip TDR schedule, it is important to understand what can reasonably be available on that timescale since at that point a decision would be needed to either delay planar strip ordering or abandon the CMOS strip option.
- A set of deliverables should be defined with ITk and strips management to aid the focus of the work.

5. Costing a CMOS solution

- The reviewers would recommend that the CMOS team improve the costing of the CMOS strip tracker.
    - This would include input from their considerations of how strip modules would be made.
    - The team should present the costs of all of the processing steps.
    - The team should not wait to the end of year 2 to do this and should present it to ITk and ITk-strip management
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CERN, July 17th 2015