Beta test of CHESS1 chip

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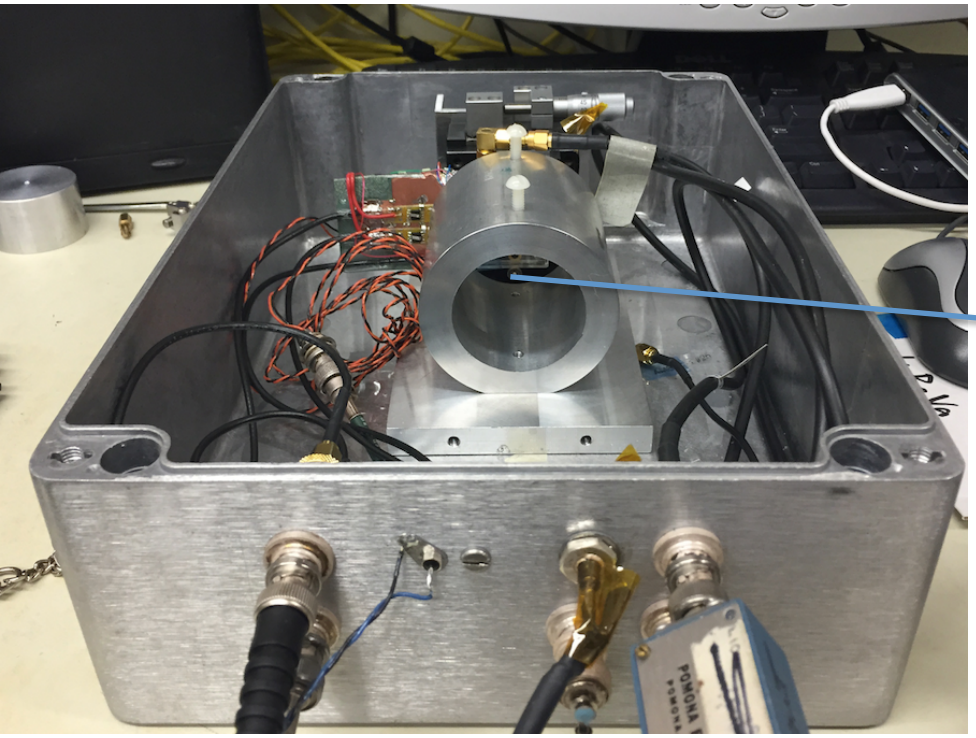
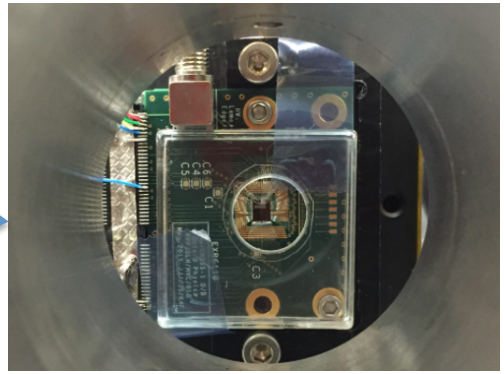
Beta test setup

- CHESS1 chip Mount on daughter board from Jaya John
- Sr90 beta source is used
- Trigger rate ~0.1 Hz
- CHESS chip Biased at 110V





Reminder of active array in CHESS1 chip

- Active array APA08 is used
- Channel 7,8 is connected for readout
- Self trigger
  - Trigger on pixel 8

Table 3.4-a Active Pixel Array Spatial Specification for HV-CMOS Technology

APA #	Pixel Dimensions	Diode Area Fraction
APA01	45µm x 100µm	30%
APA02	45µm x 100µm	50.4%
APA03	45µm x 200µm	30%
APA04	45µm x 200µm	50.4%
APA05	45µm x 400µm	30%
APA06	45µm x 400µm	50.4%
APA07	45µm x 800µm	30%
APA08	45µm x 800µm	50.4%

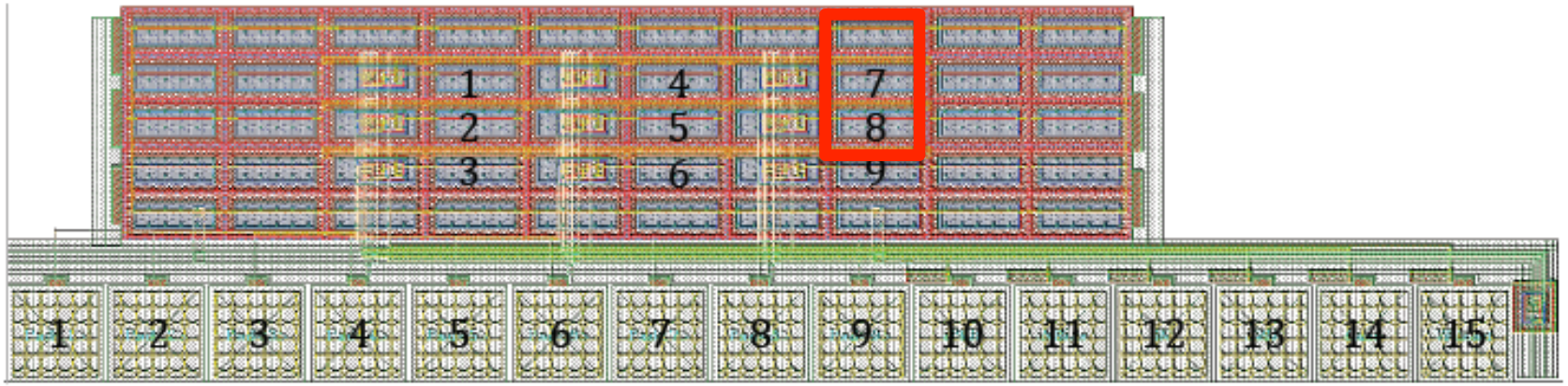
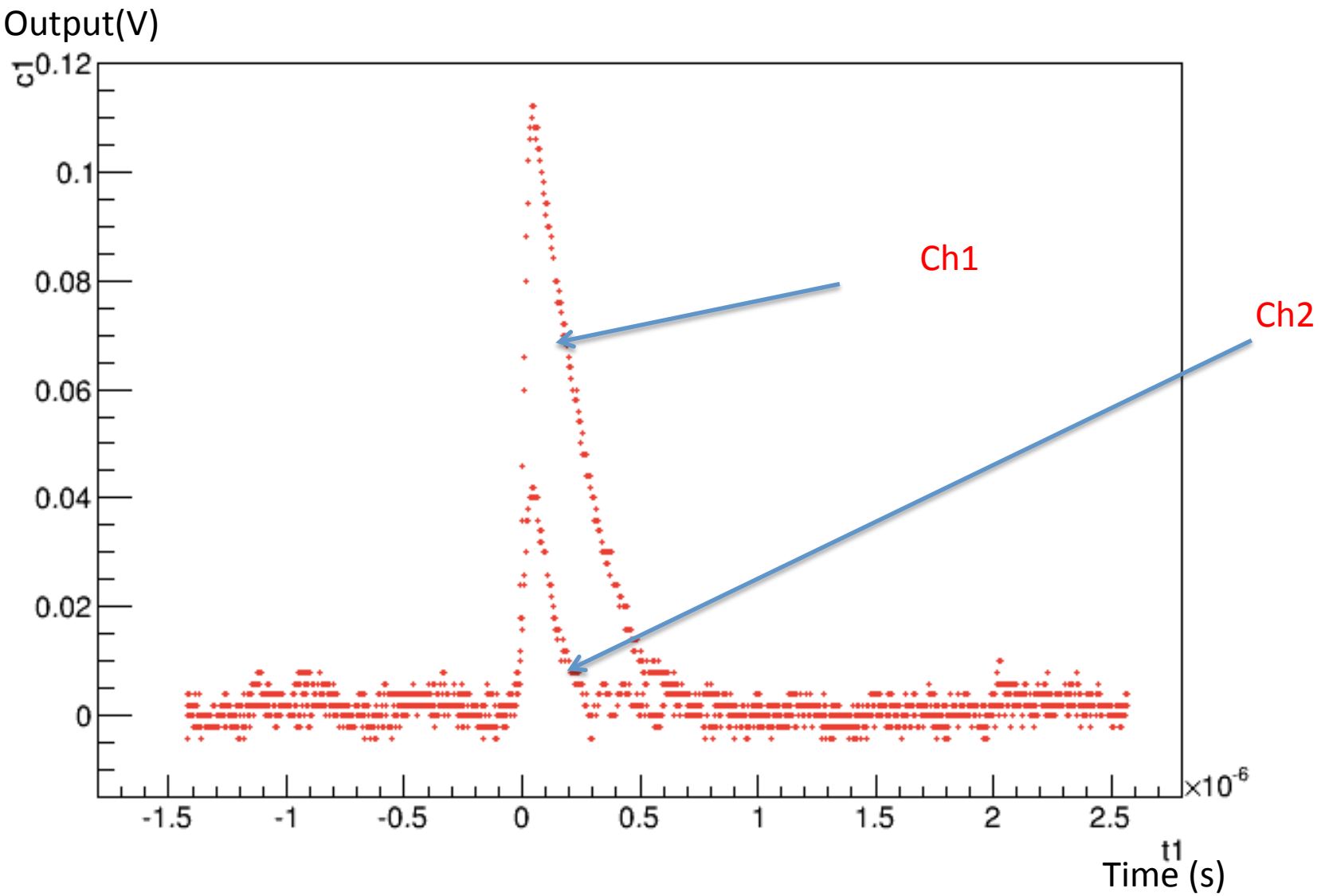


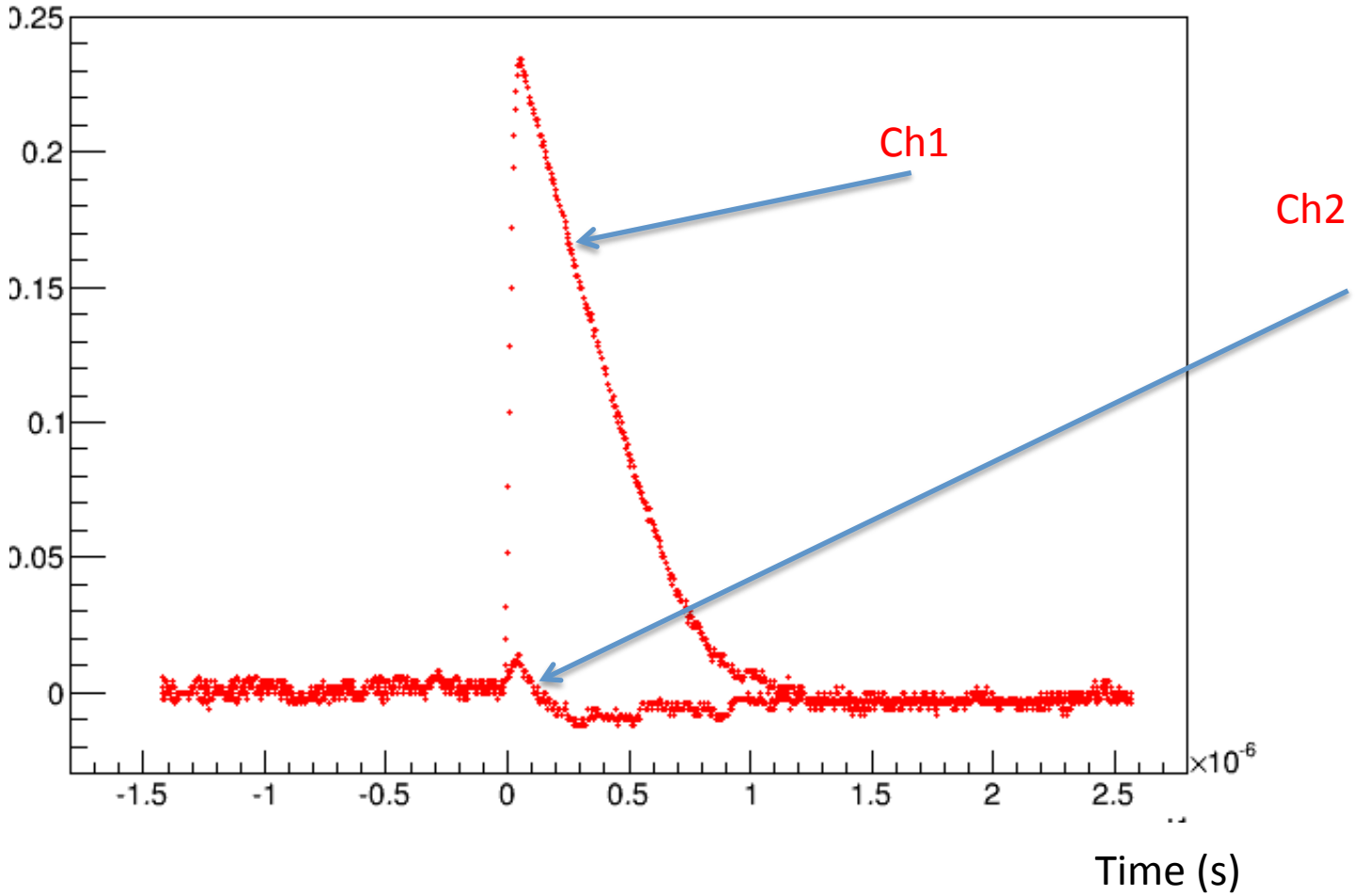
Figure 3–3 Layout for the 45µm x 200µm Active Pixel Array with pixel numbering and pad layout. The connection to the pad layout are identified in Table 3.3.2

Pulse shape in charge sharing case

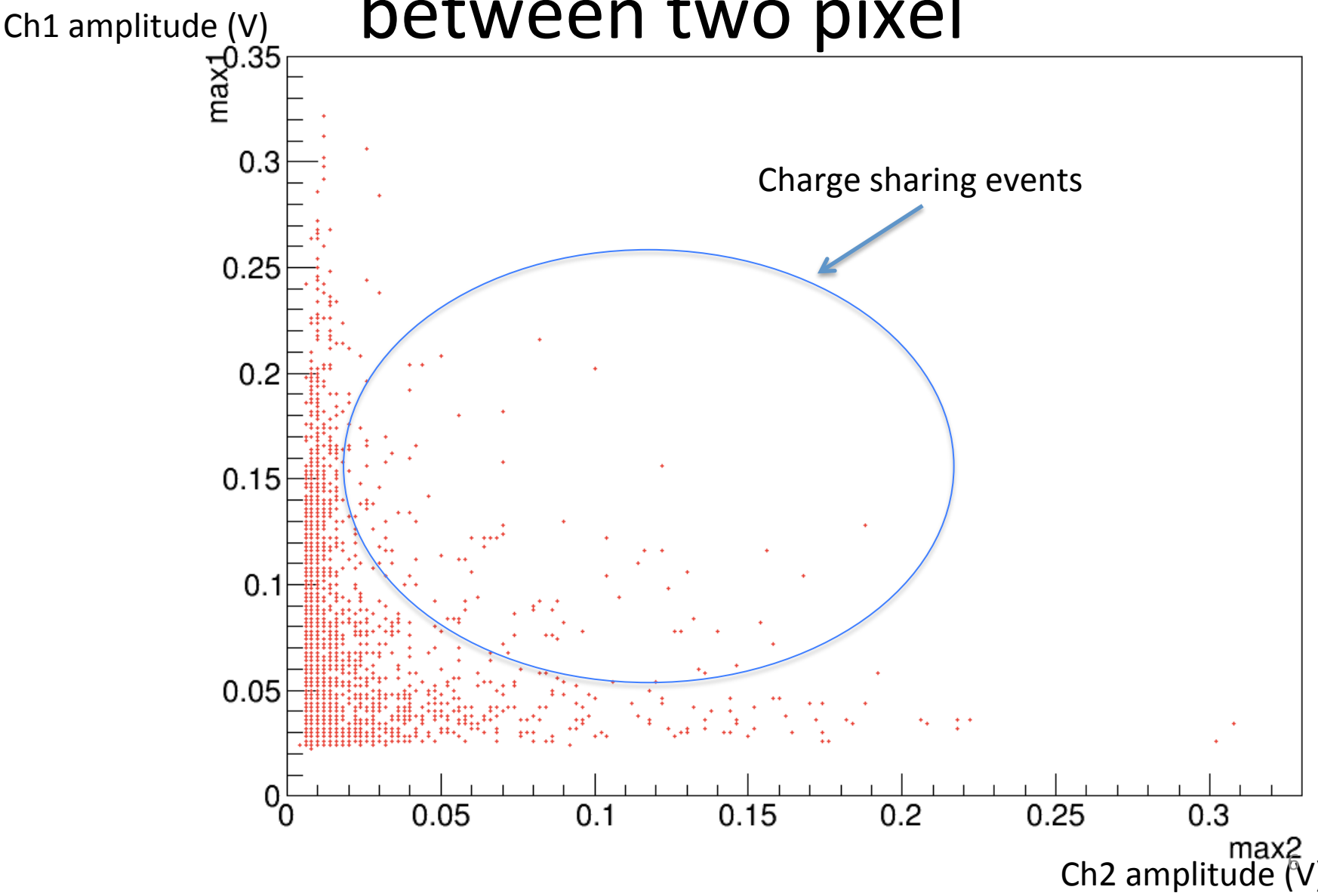


Pulse shape in usual case without charge sharing

Output(V)



Correlation in signal amplitude between two pixel



Summary

- observe significant signal from active pixel in beta source test
- Next step :
  - Quantify the landau peak position of MIP in beta test
  - Quantify the fraction of charge sharing between pixels
  - Reduce the readout noise by optimizing the built-in amplifier configuration.