HR-CHESS2 update

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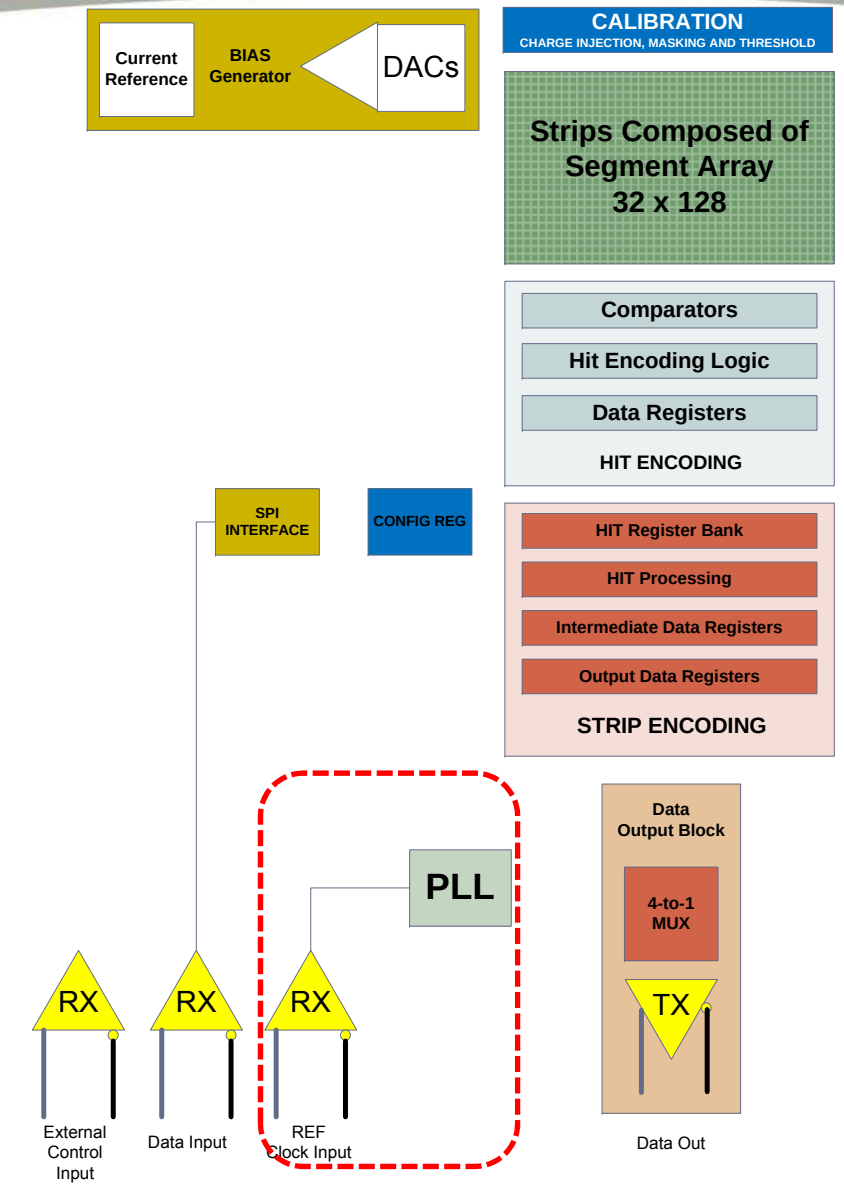
Architecture Demo Chip Block Diagram



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Technical Specifications Summary

Close to HR-CHESS spec (Physics requirements!)
Specifications below for one block:

Technology: TowerJazz 180 nm
Voltage supply: 1.8/3.3V
Wafers: Epitaxial
Epi resistivity/thickness: up to 25um/up to >1kOhm cm *
Segment size: 40umx800um (Segments could contain smaller pixels *)
Number of strips: 128
Number of segments per strip: 32
Readout speed ≥ 320 Mbit/sec
Output buffers: LVDS with adjustable bias current and CM level
Maximum number of hits per strip: 1 + overflow flag
Maximum number of hits in block: 8
Size of data output per strip: 13 bits
Format of data output: 5 (segment) + 1 (segment overflow flag) + 7 (strip address) bits

* pending results from HR-CHESS1

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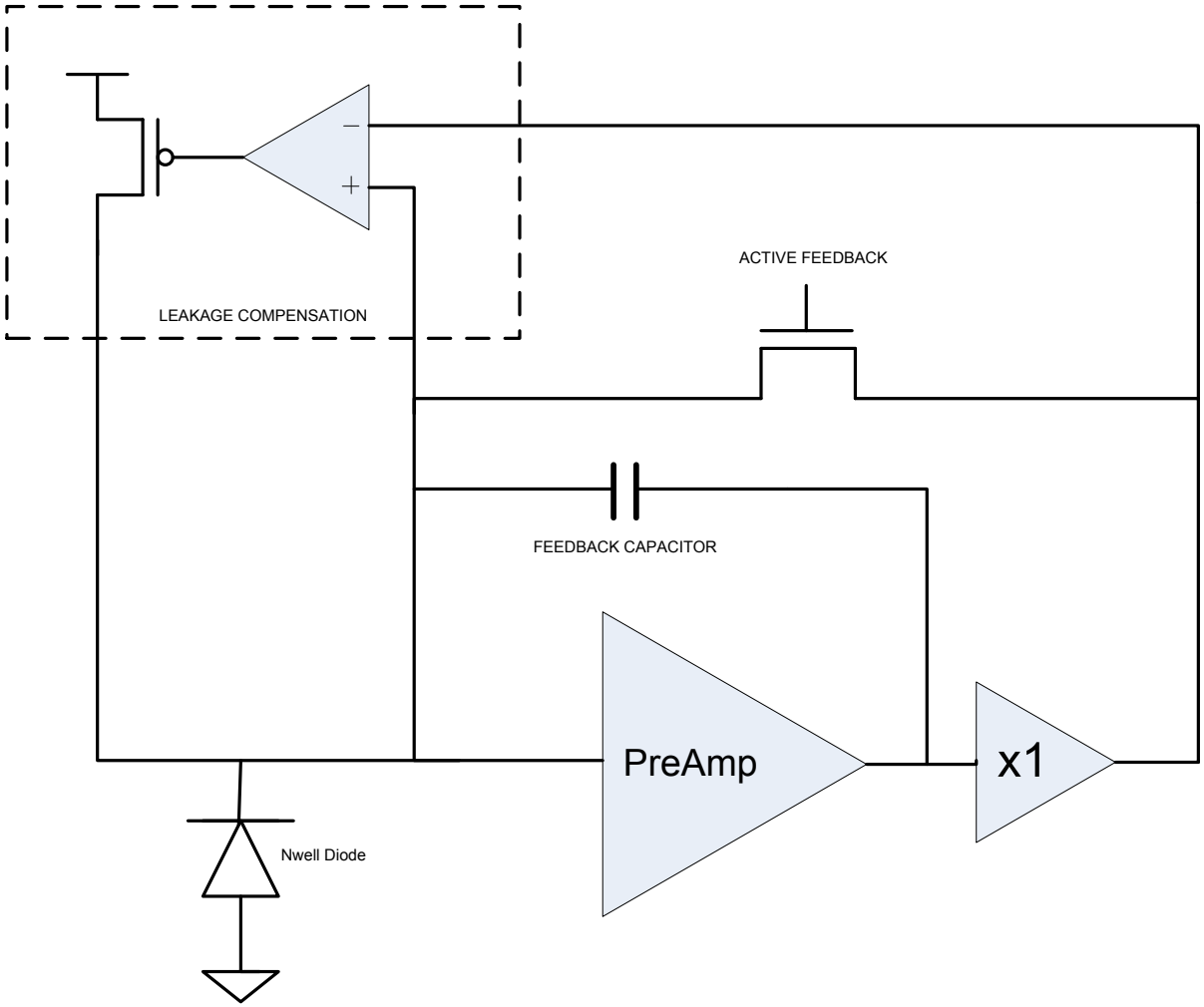
Pre-Amplifier diagram



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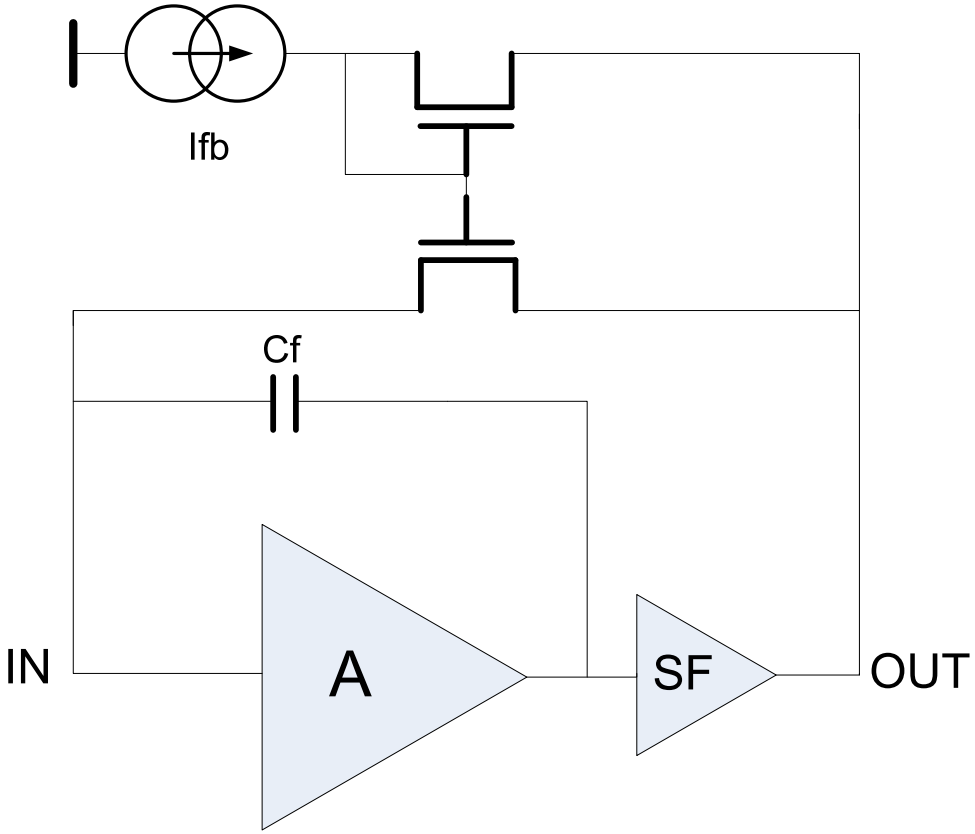
Continuous reset



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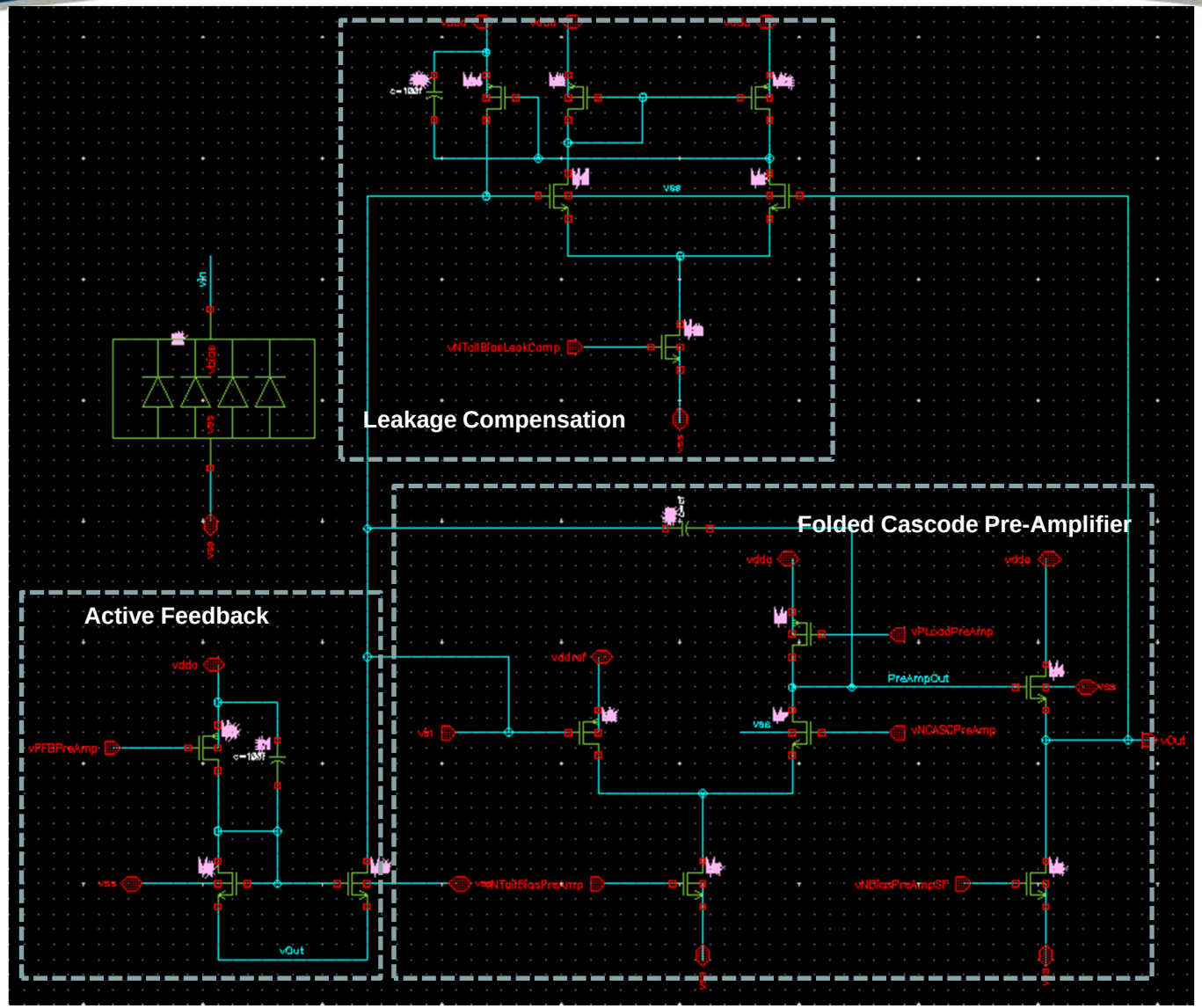
Pre-Amplifier schematic



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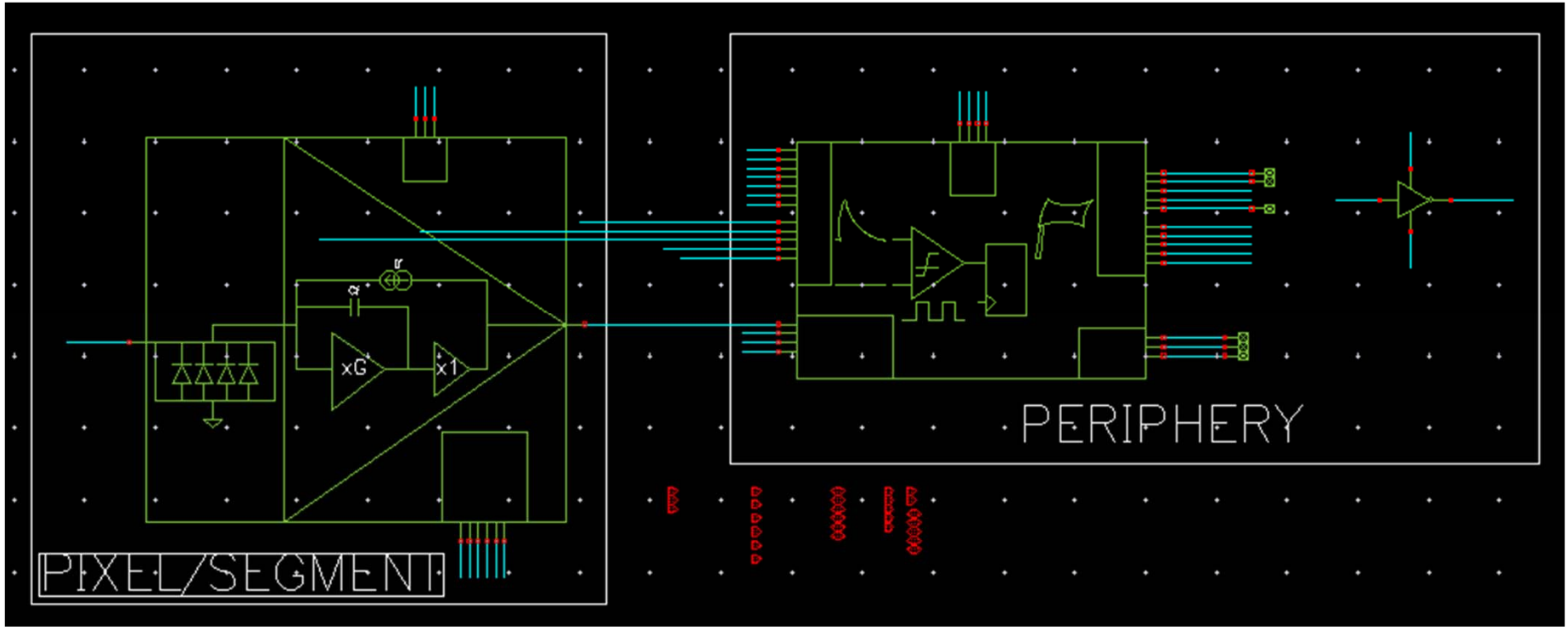
Front-end schematic



x32 in 1 complete column

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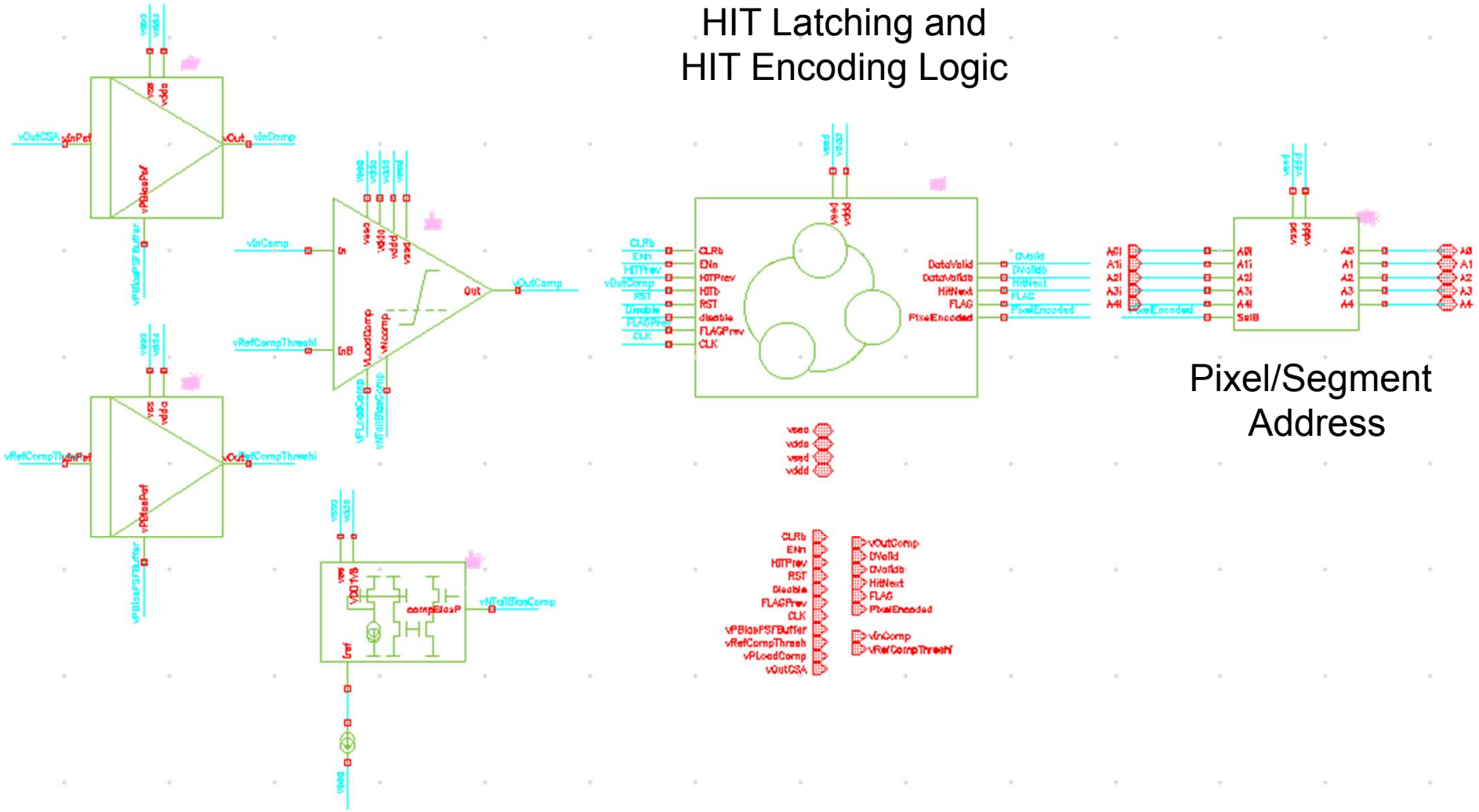
Front-end (periphery) schematic

HIT Latching and
HIT Encoding Logic



Pixel/Segment
Address

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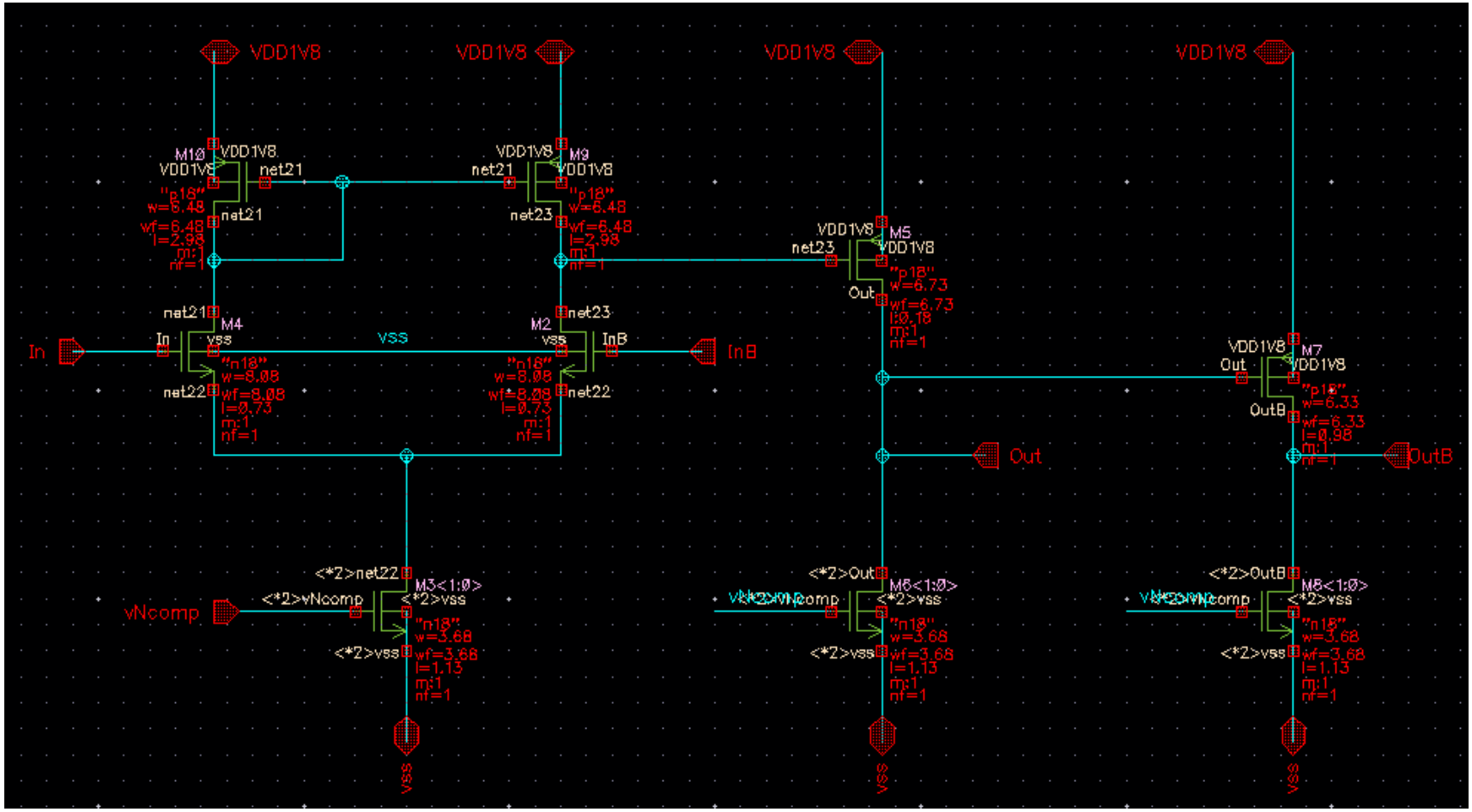
Comparator schematic Initial Trial



Didn’t exactly meet the time-walk requirements of <16ns

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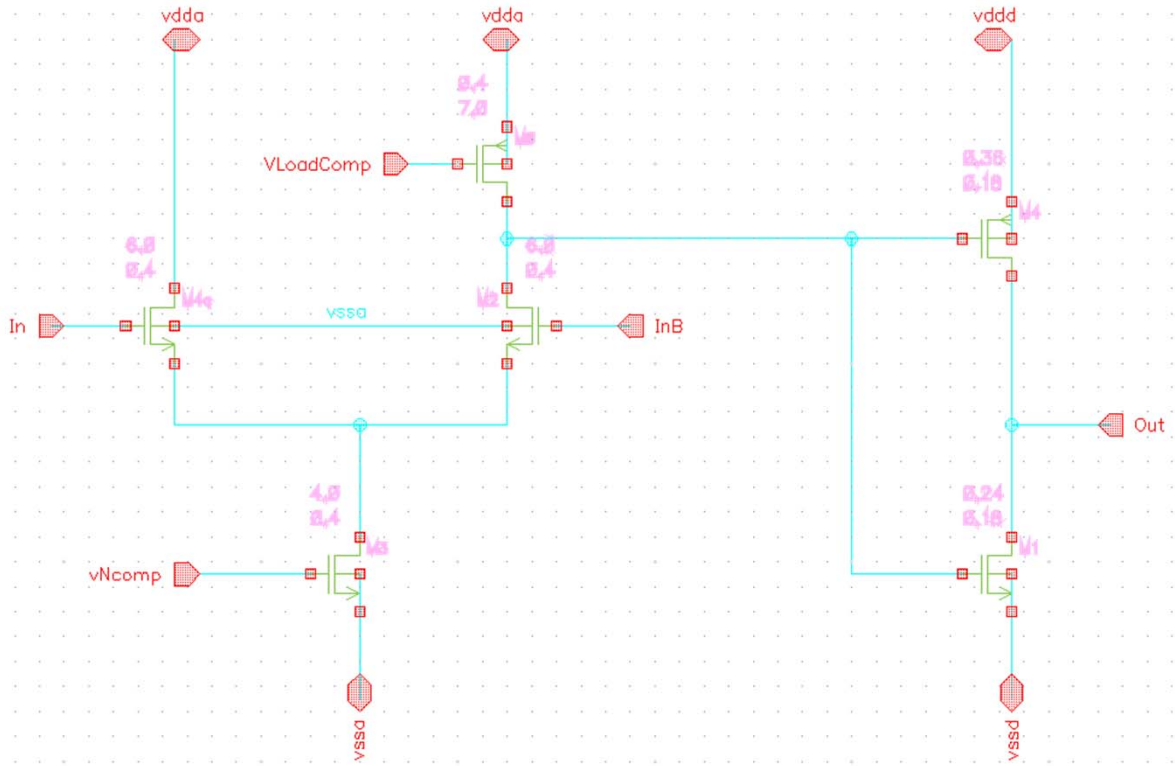
Comparator schematic We liked!



- Same as HV-CHESS, see Herve's review presentation
- Meets time-walk requirements of <16ns, see later
- Power Consumption < 15µW

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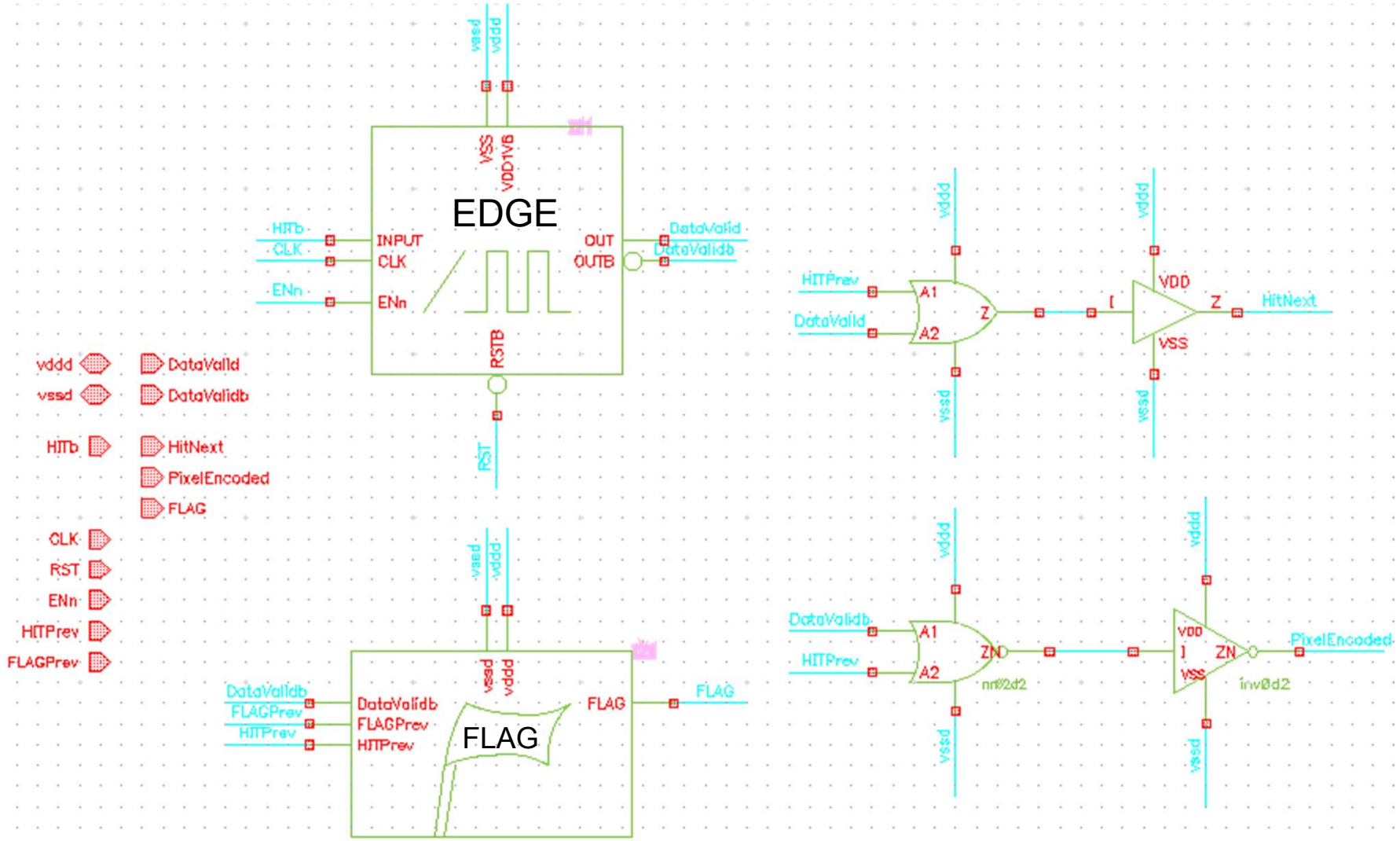
Front-end (periphery) logic schematic



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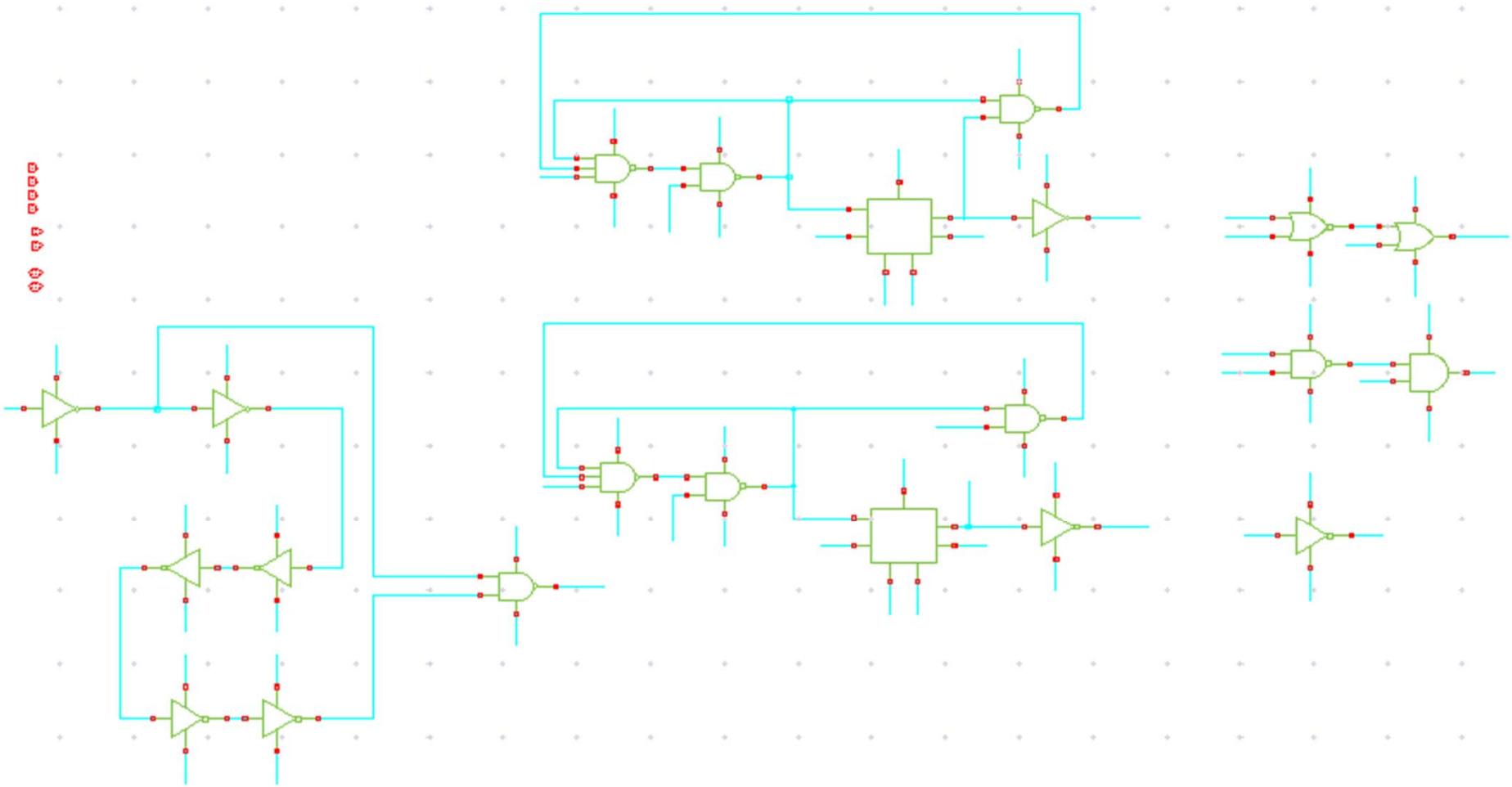
Edge Detector schematic



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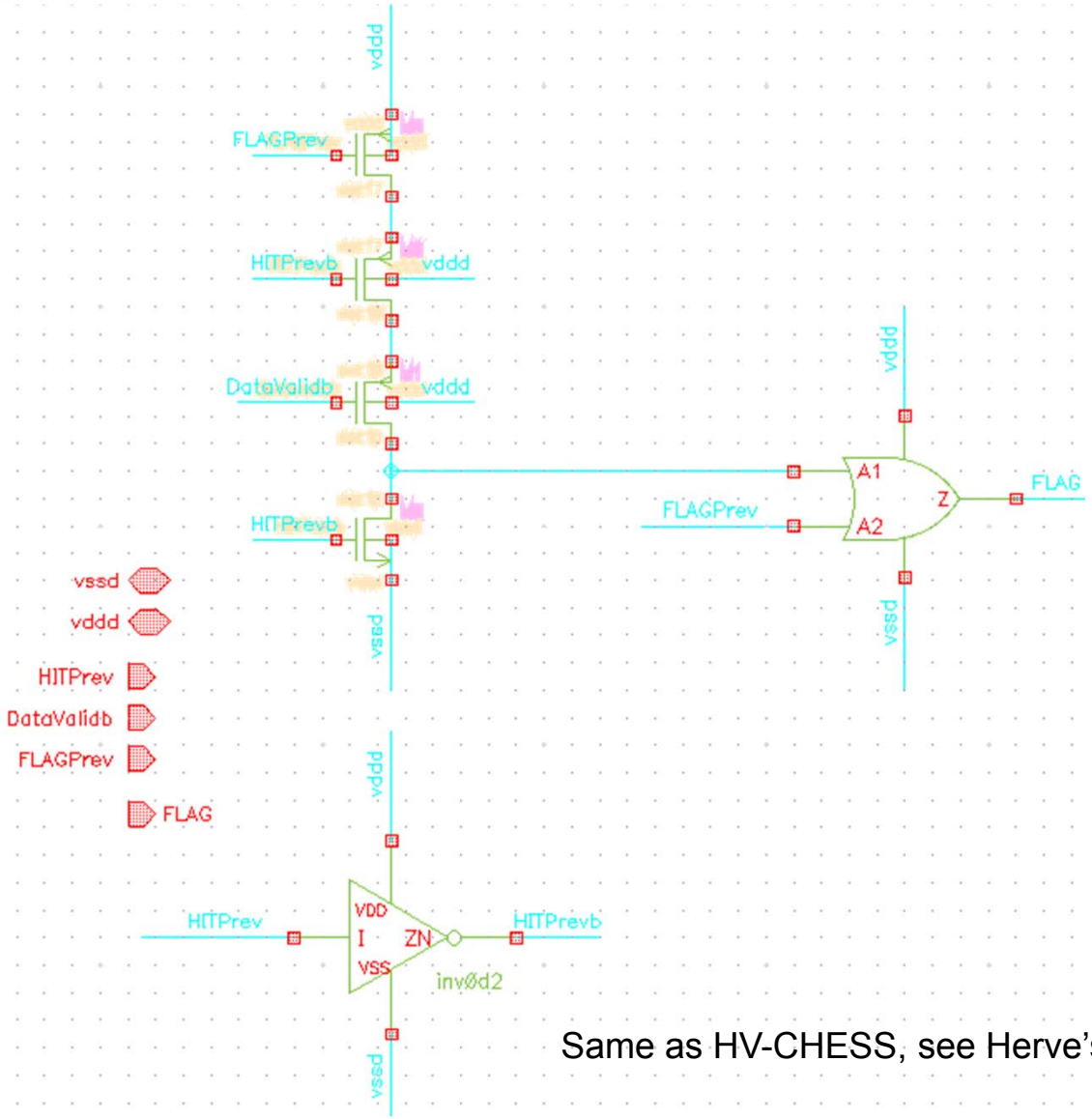
FLAG Logic schematic



Same as HV-CHESS, see Herve's review presentation

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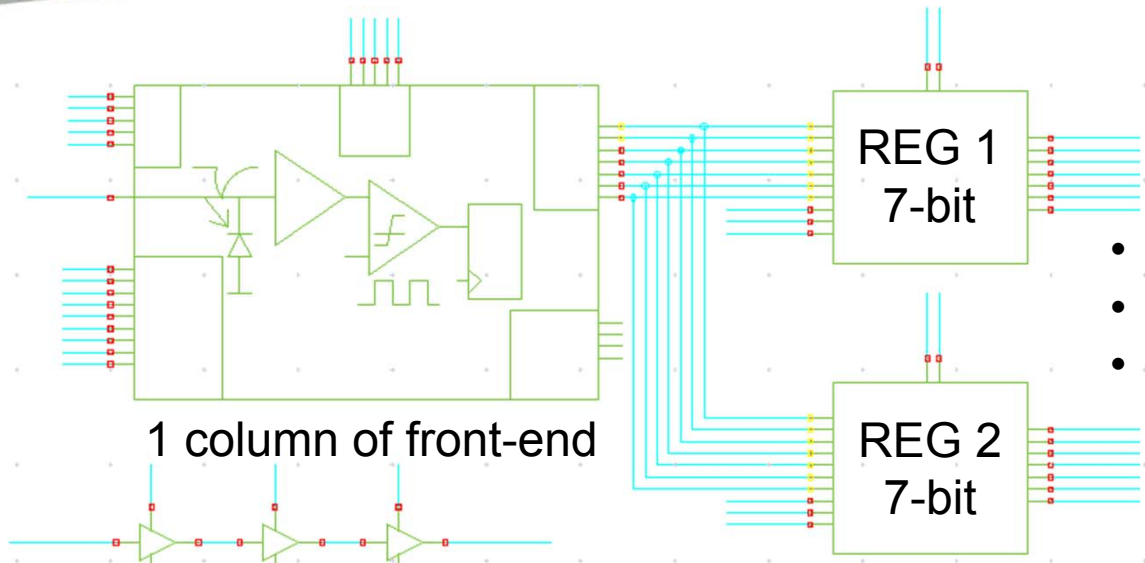
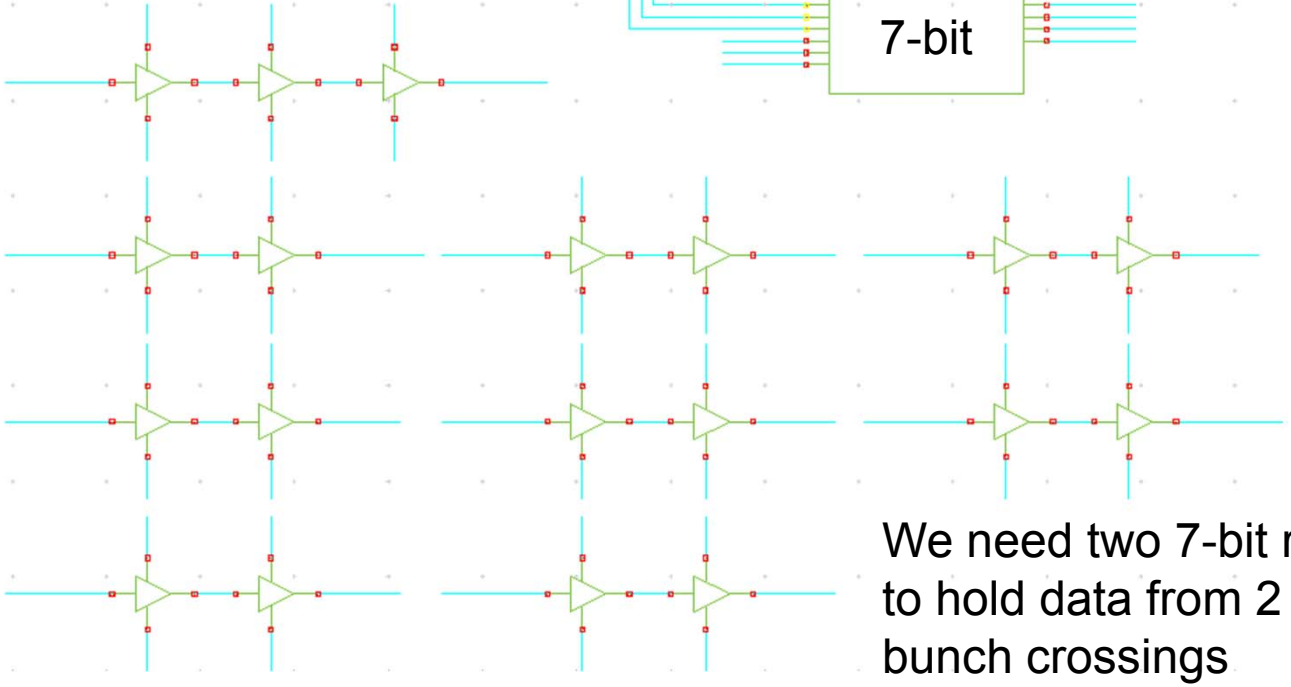
Complete column schematic



1 column of front-end

- 5-bit pixel address
- 1-bit FLAG
- 1-bit to indicate strip was hit



We need two 7-bit registers to hold data from 2 successive bunch crossings

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Pre-Amplifier Spec Achieved

	MIN	MAX	NOM	FAST	SLOW	SF	FS
CG [µV/e] @1000e-	52.31	63.79	57.24	52.31	63.79	55.89	57.24
Trise [ns] (10% to 90%)	9.8	16.03	11.95	9.8	16.03	13.13	11.95
Noise [e-]	47	51	50	51	47	50	50
Phase Margin [º]	70.01	74.42	70.76	70.01	73.31	74.42	70.76
Open Loop Gain [dB]	50.6	58.8	56.96	52.5	58.83	50.59	56.96
Power [µW]	13.44	19.71	16.647	19.71	13.44	15.381	16.648

- Optimised design over all process corners
- Leakage current tolerance up to 10nA
- Overload recovery within 15usec for 1Me- signal

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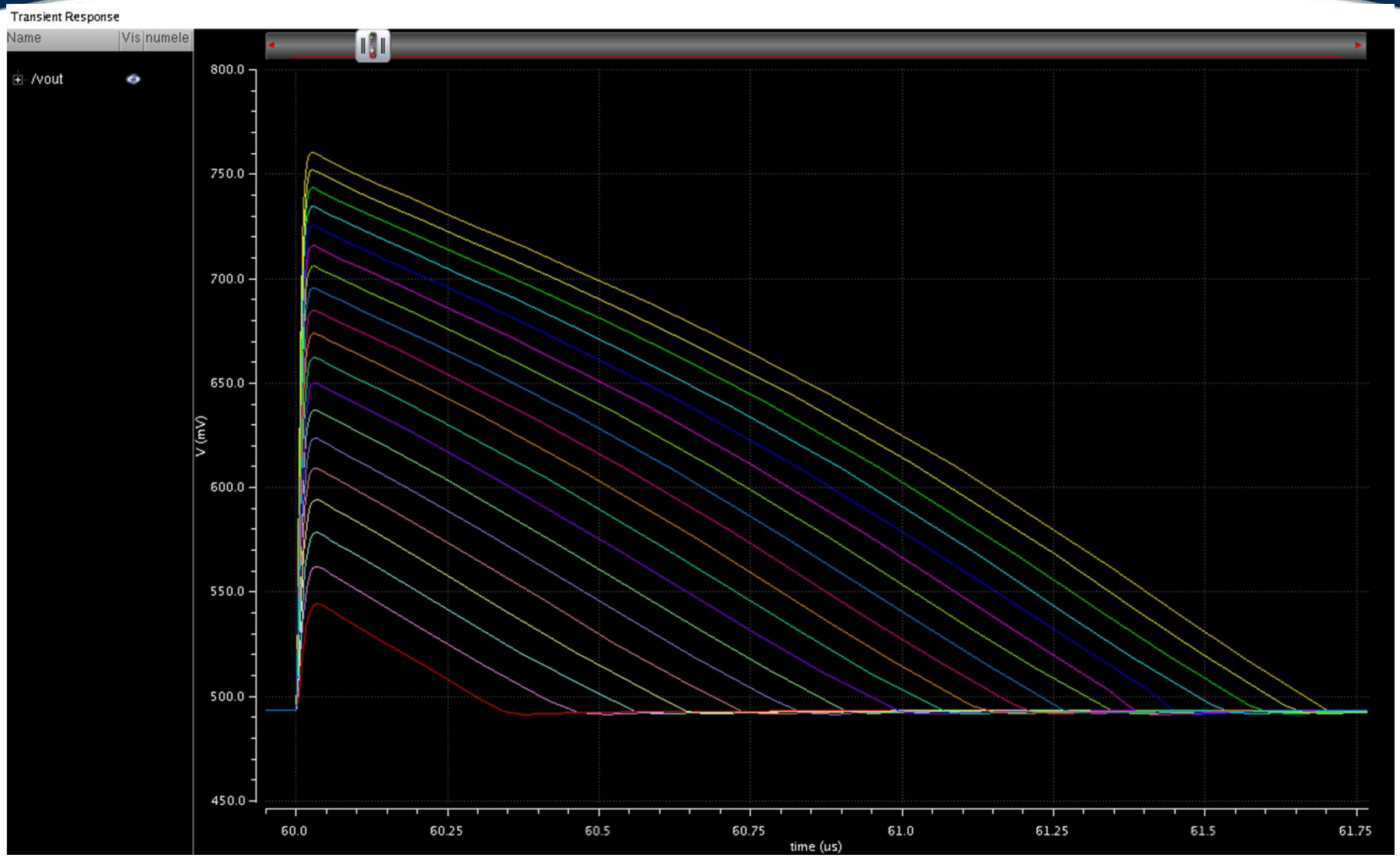
Vout vs Signal (500e- to 5000e-)



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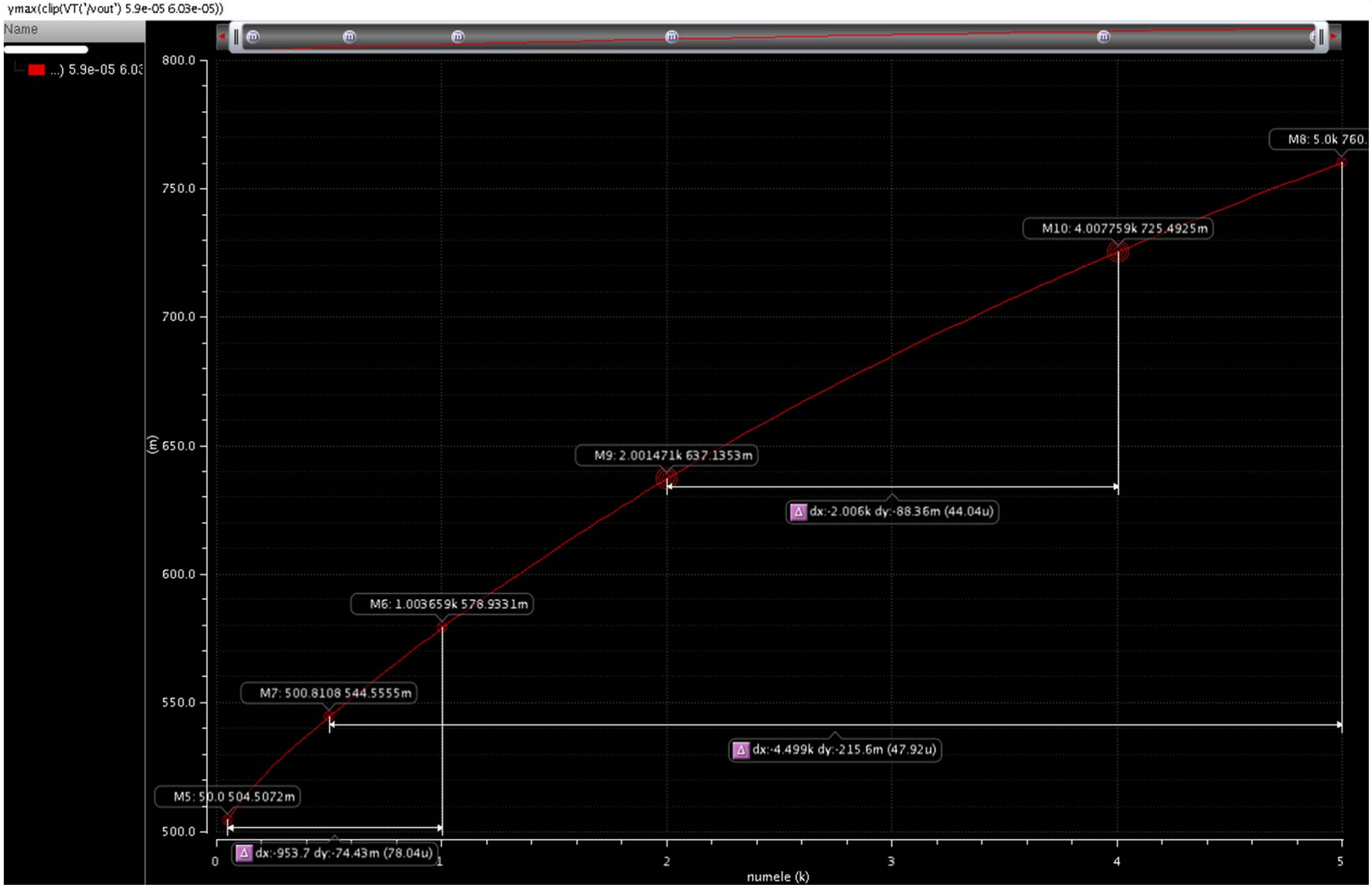
Conversion Gain [uV/e] vs Signal (50e- to 5000e-)



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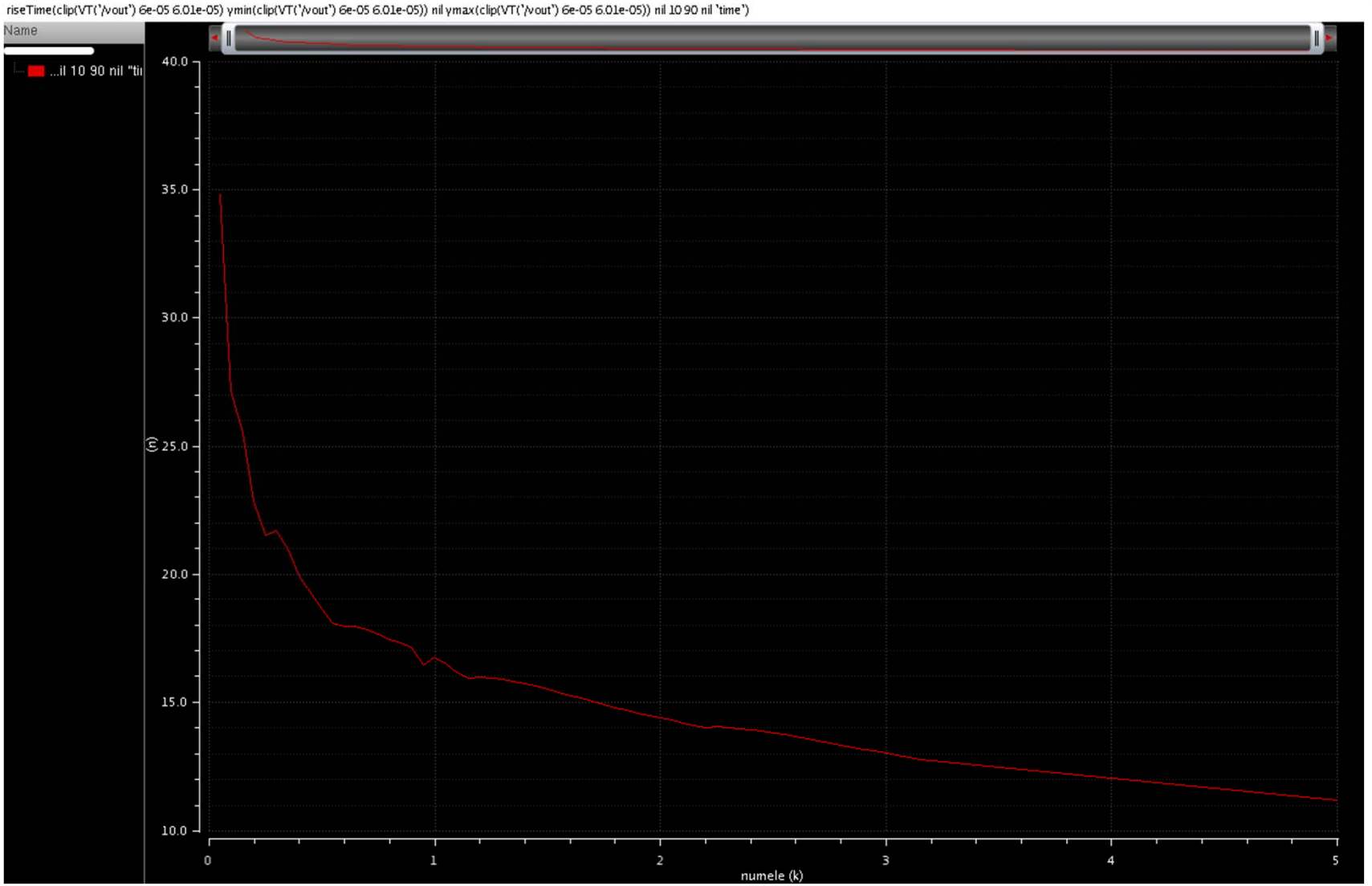
Trise vs Signal (10% to 90%)



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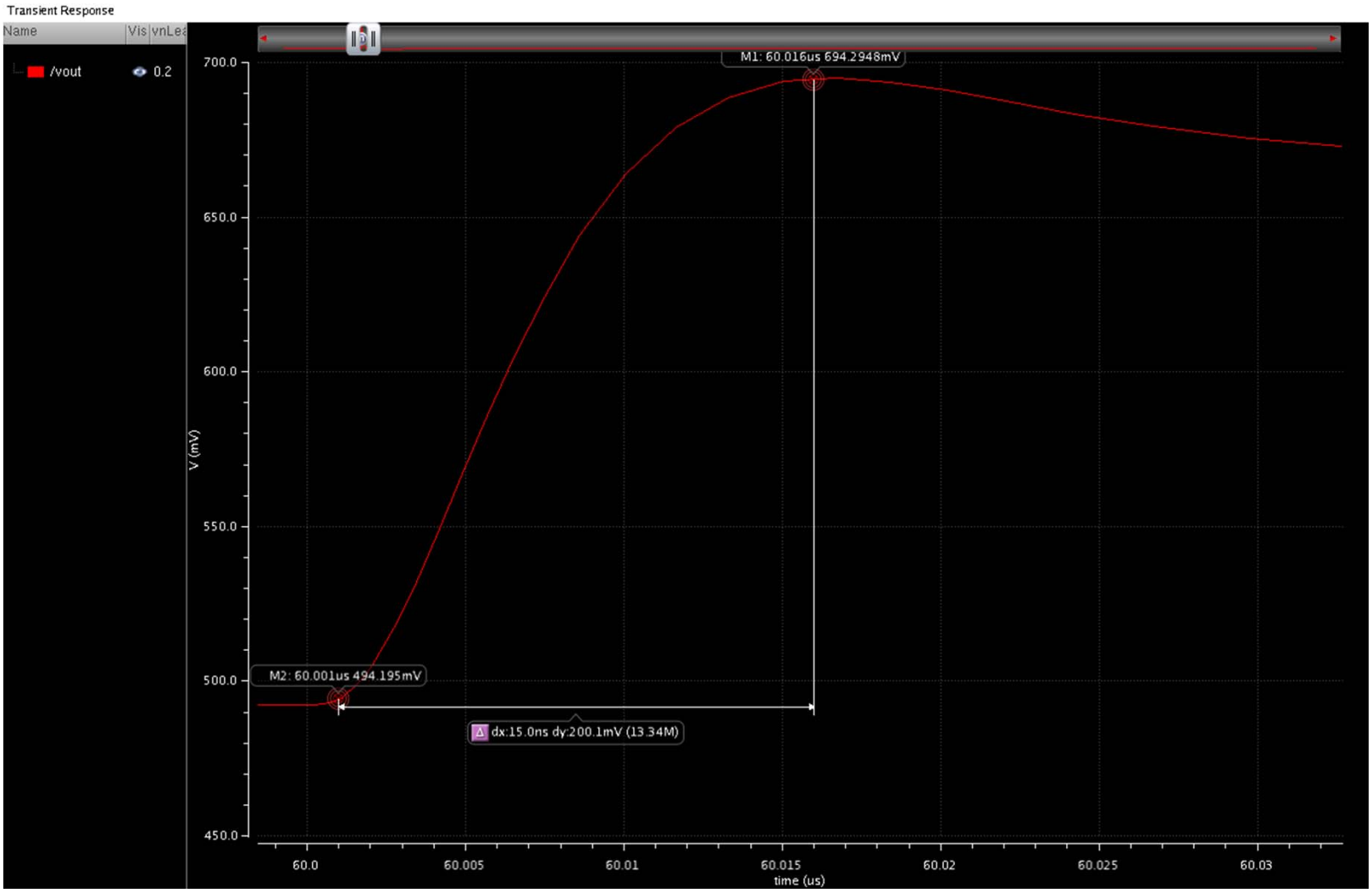
Trise vs Signal (from baseline up to peak)



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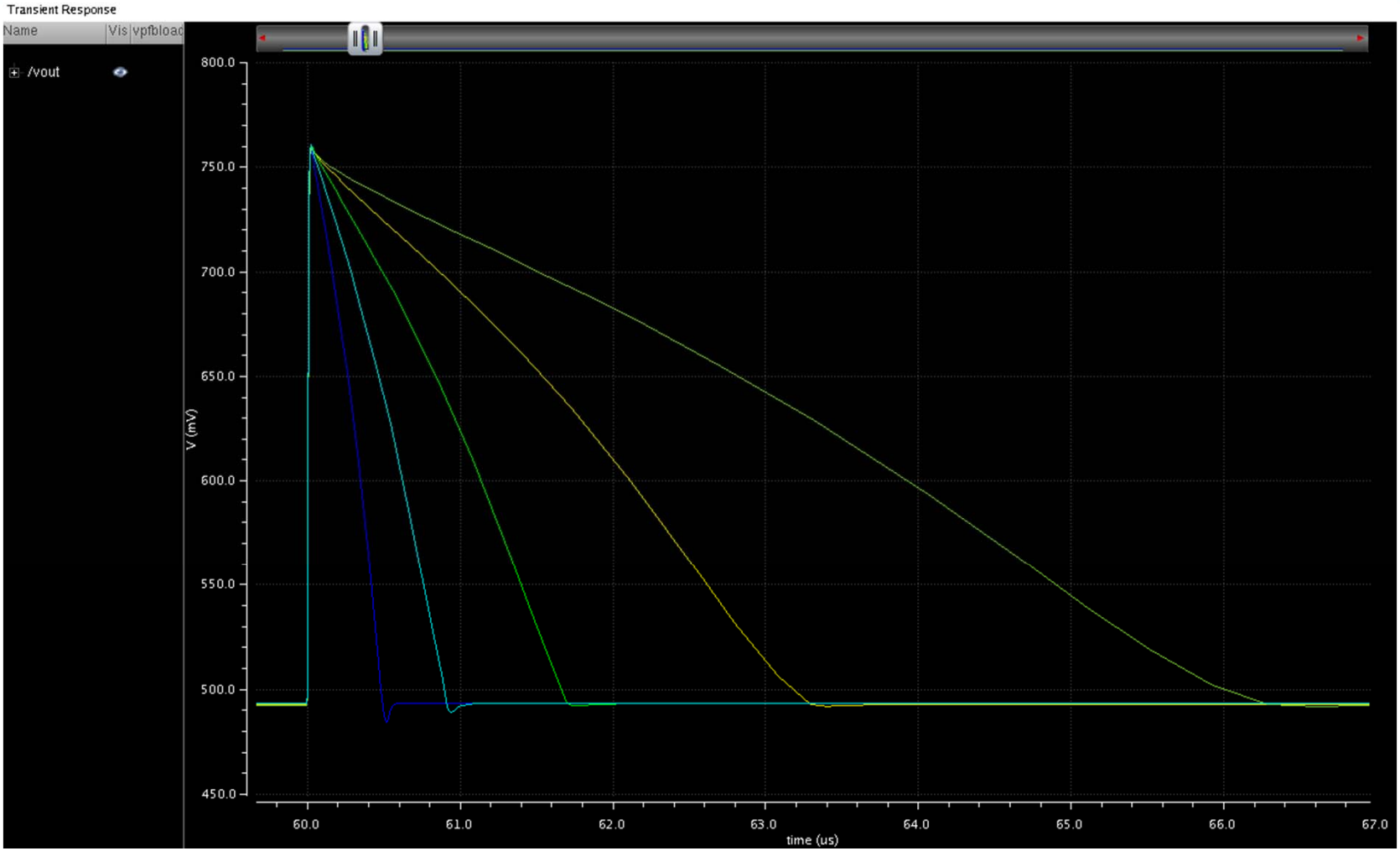
Pre-amp Discharge Control (5Ke-)



Changing vPLoadFBPreAmp by 100mV in steps of 25mV

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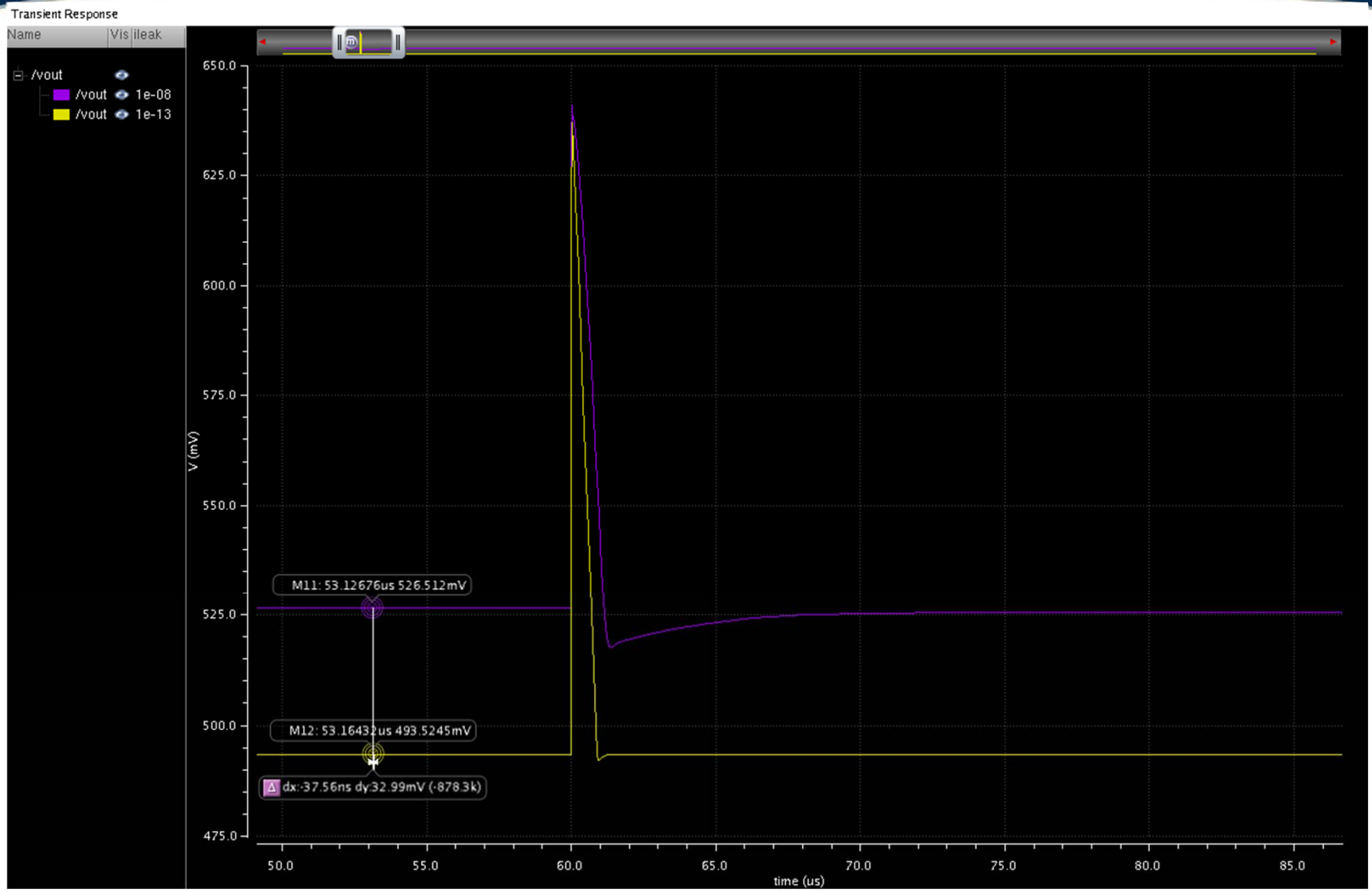
Vout without leakage Compensation (0.1pA to 10nA)



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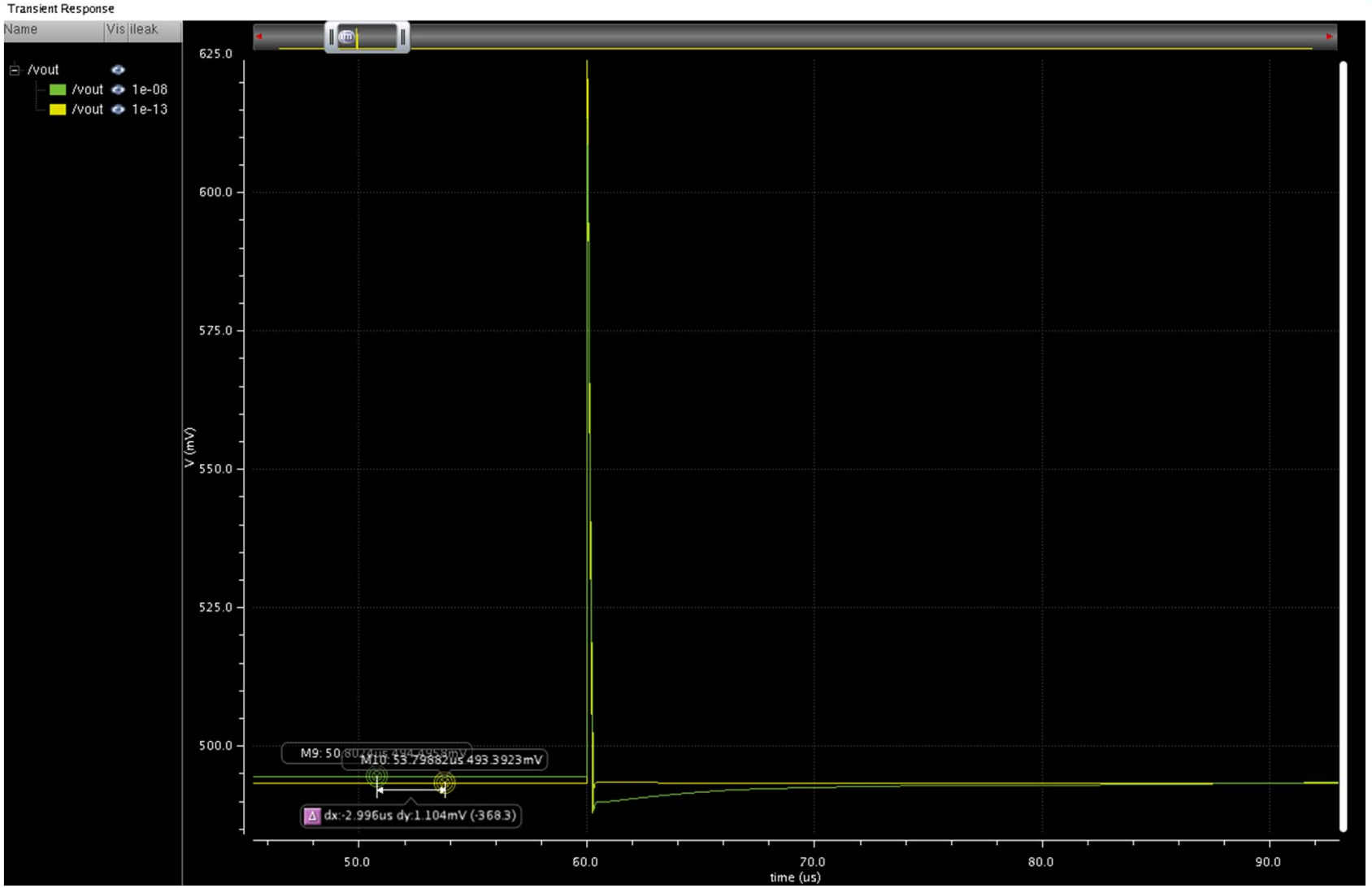
Vout with leakage Compensation (0.1pA to 10nA)



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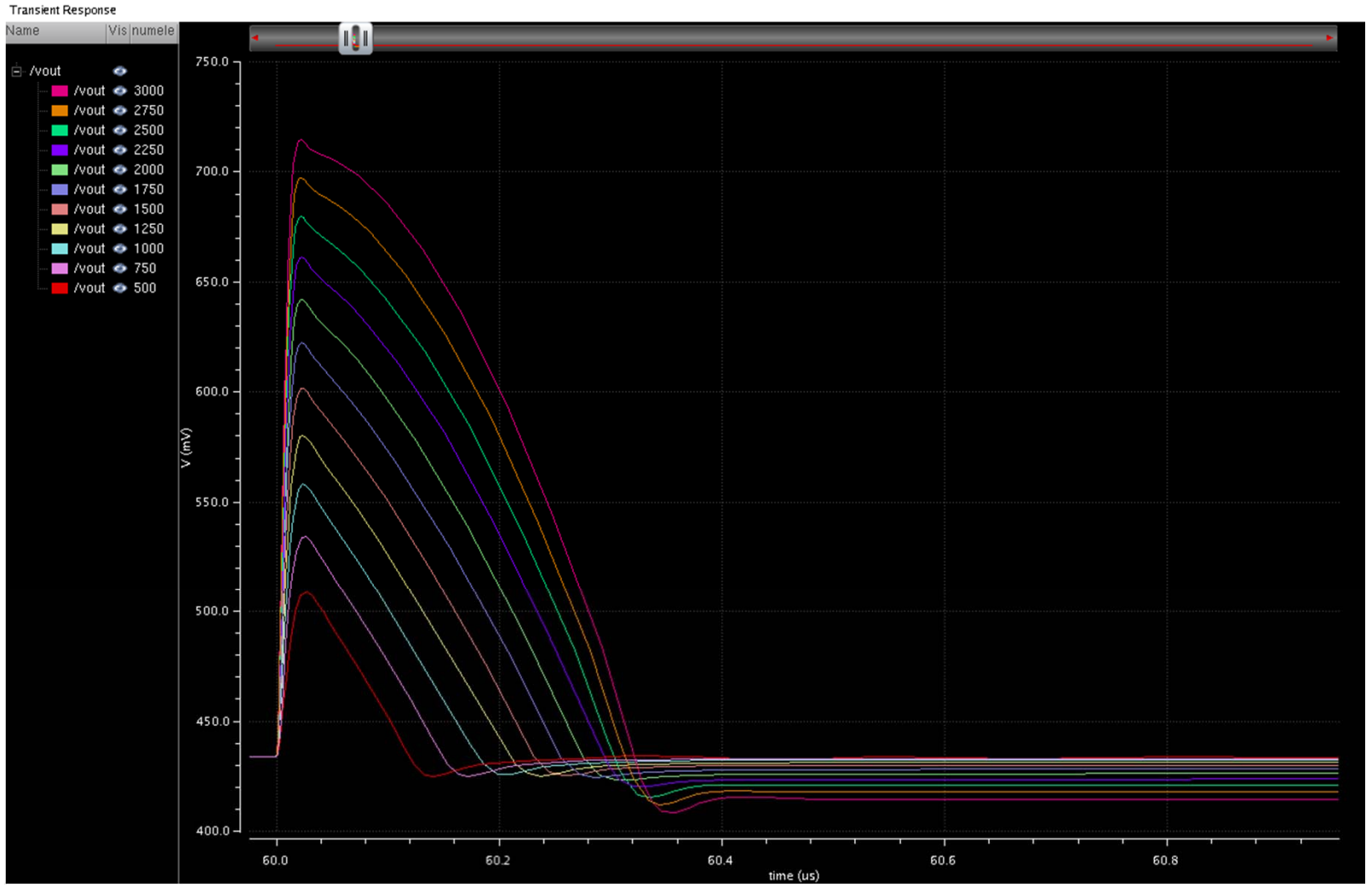
Vout with leakage Compensation @10nA leakage current



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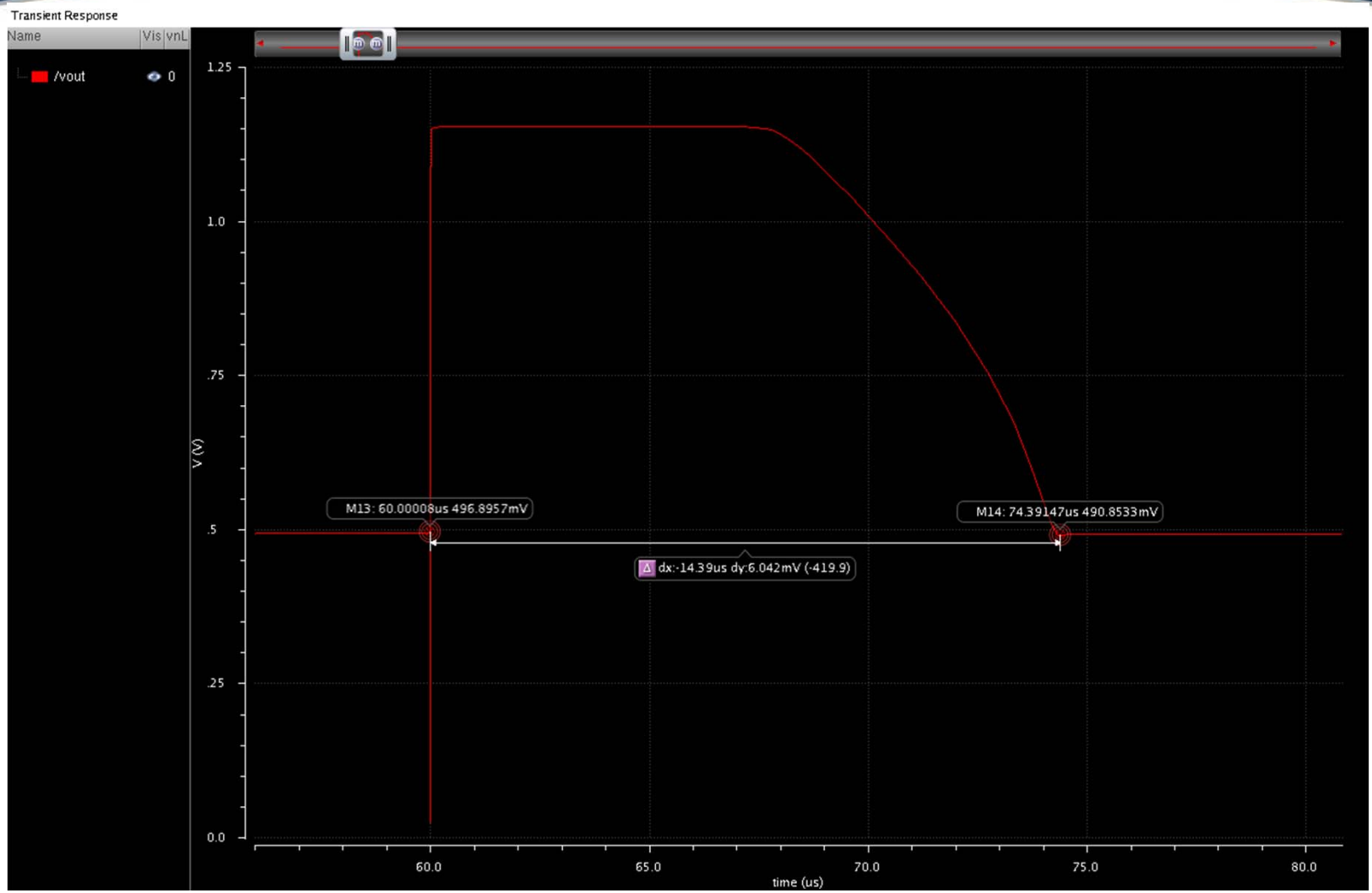
Overload Recovery @1Million e-



Return to base line within 15µs

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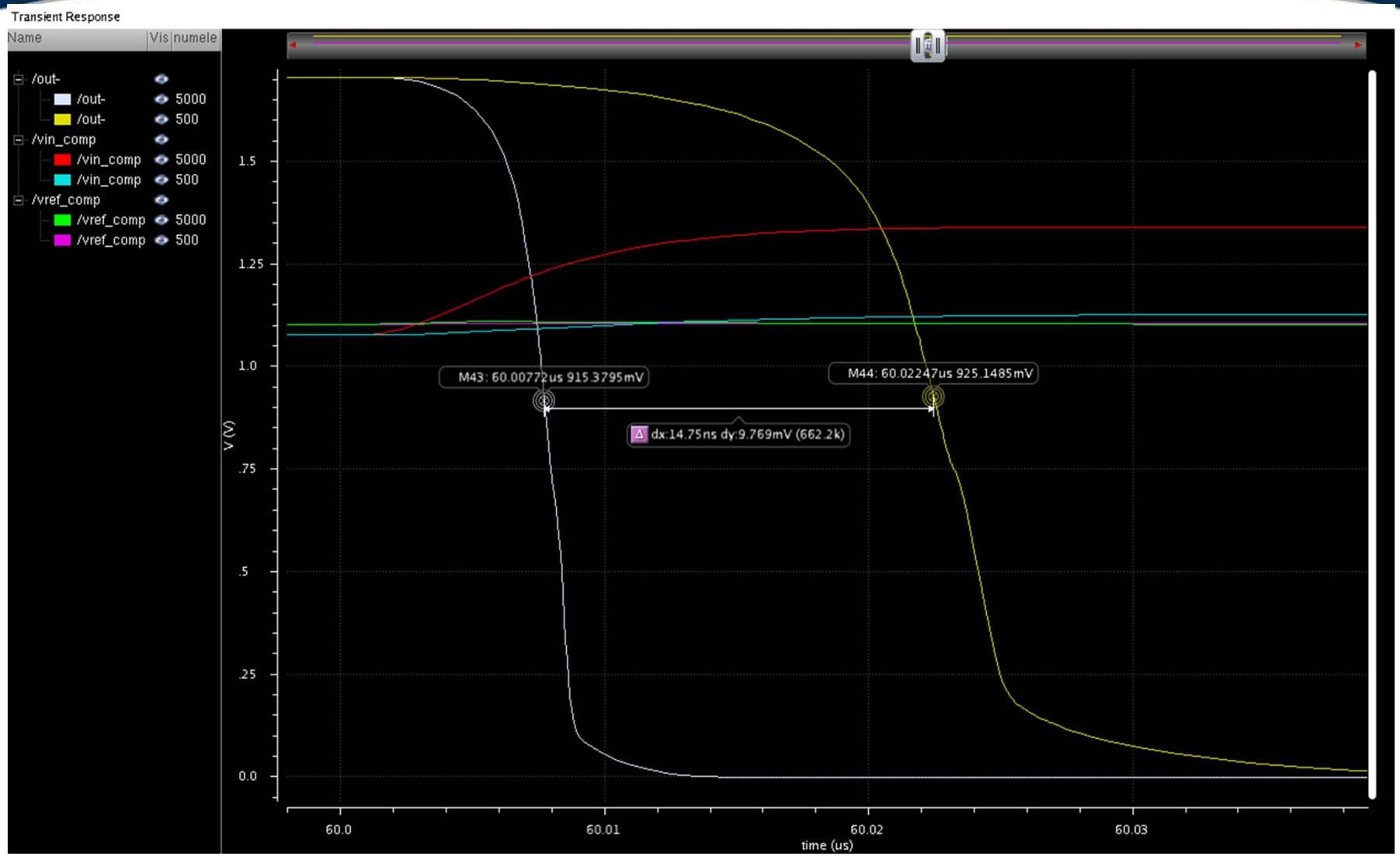
Time-Walk (Threshold @ 275e-)



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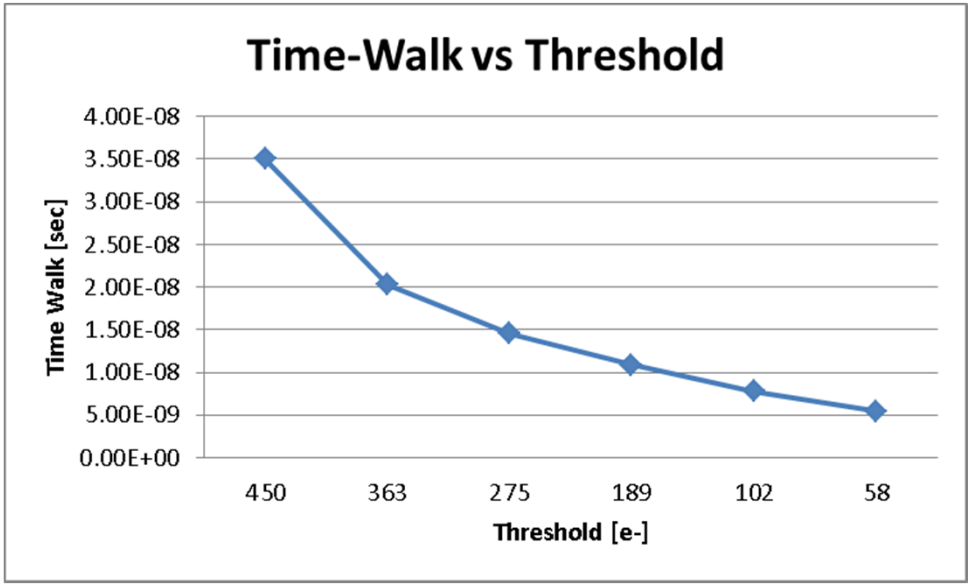
Time-Walk vs Threshold



Minimum Signal: 500 e-
Maximum Signal: 5000 e-

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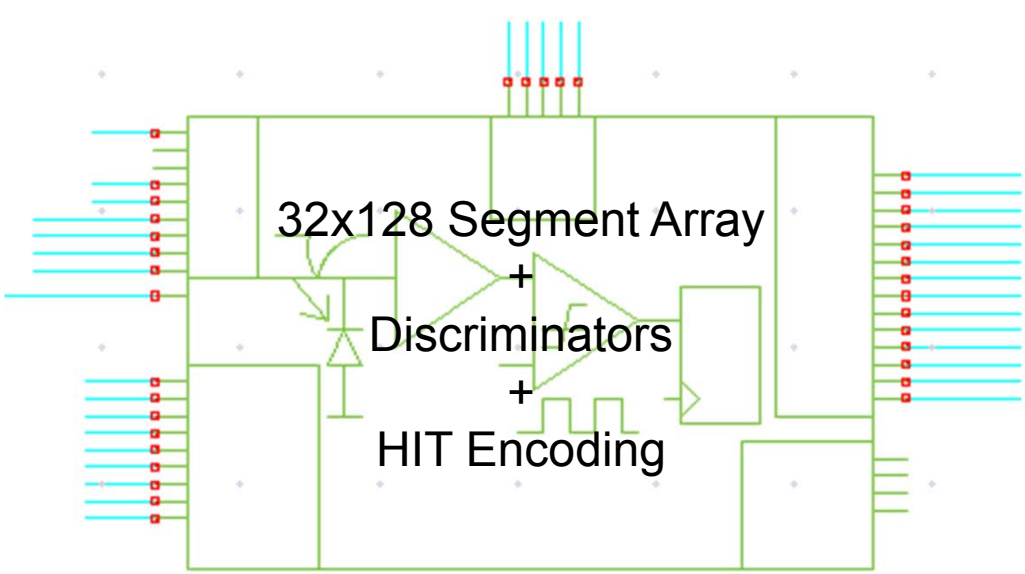
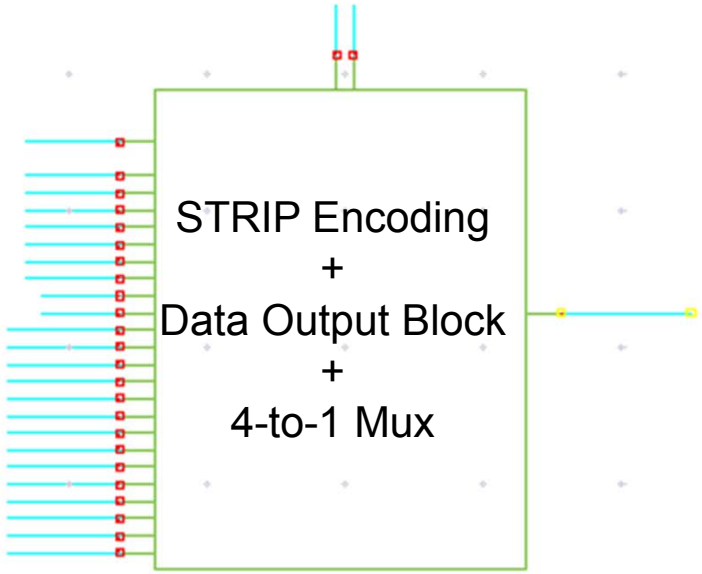
Top-Level Simulation





NOT Simulated in this block:

- Calibration
- Bias Generation
- CONFIG REG/SPI
- PLL
- LVDS

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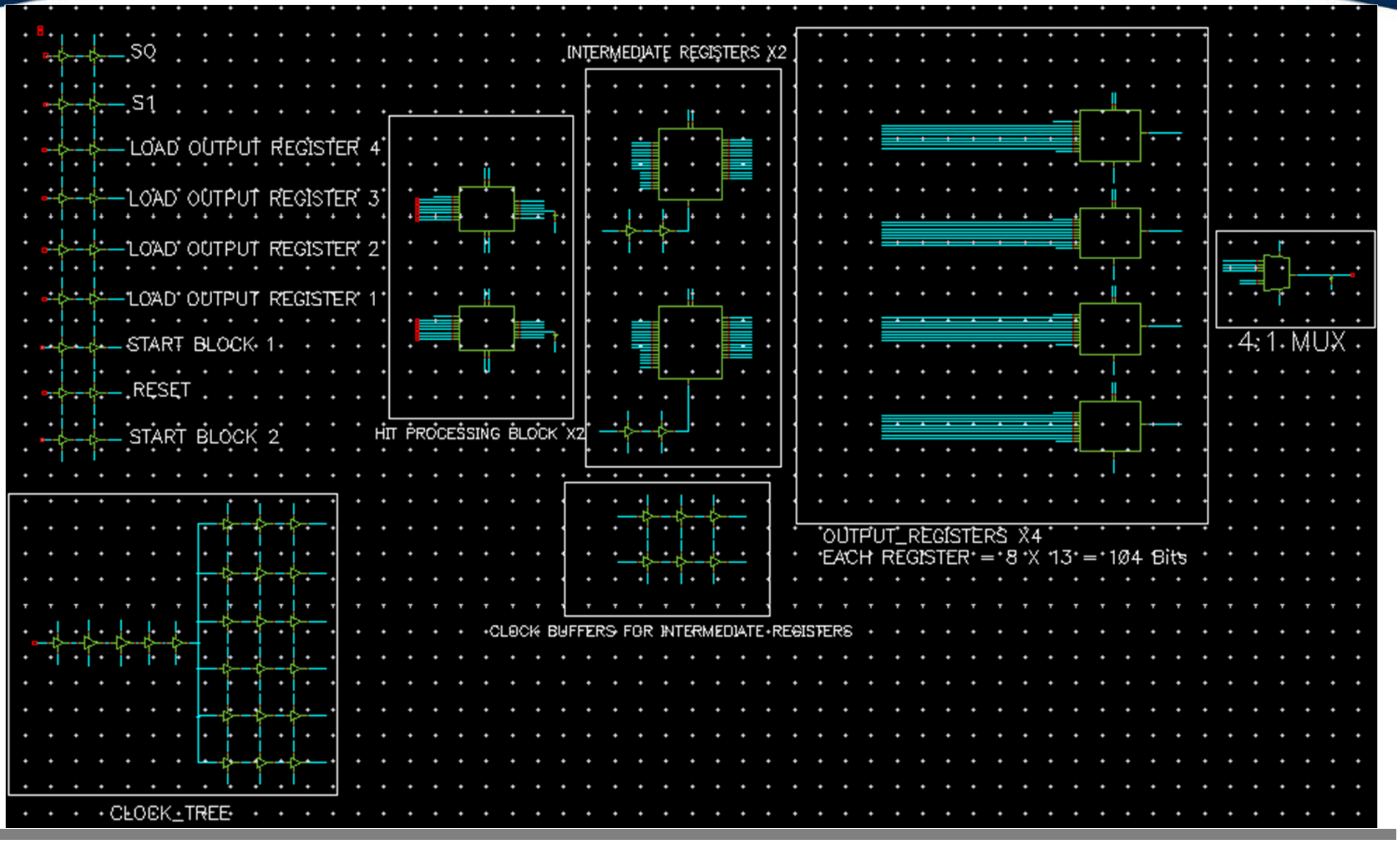
Strip Encoding and HIT Readout Block



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Top-Level Simulation

- We simulated the Top-Level schematic.
- We simulate 3 Strips being hit
- For each strip the last Segment/Pixel was hit
- 7-bit Strip address Gray coded.
- Goal is to read out these 3 hits and output their address inside 2 bunch crossing periods or 50 ns.
- Clock period used in simulation is 320 MHz
- The Hit addresses corresponding to each bunch crossing are then stored and readout through LVDS stages every 25 ns.
- Table below shows the Hit locations and corresponding 7-bit Strip address (Gray coded).

Hits	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0	Strips
1	0	0	0	0	0	0	0	0
2	0	0	0	0	1	1	0	4
3	0	0	0	1	1	0	1	9

Data 4	Data 3	Data 2	Data 1	Data 0	Segment
1	0	0	0	0	32

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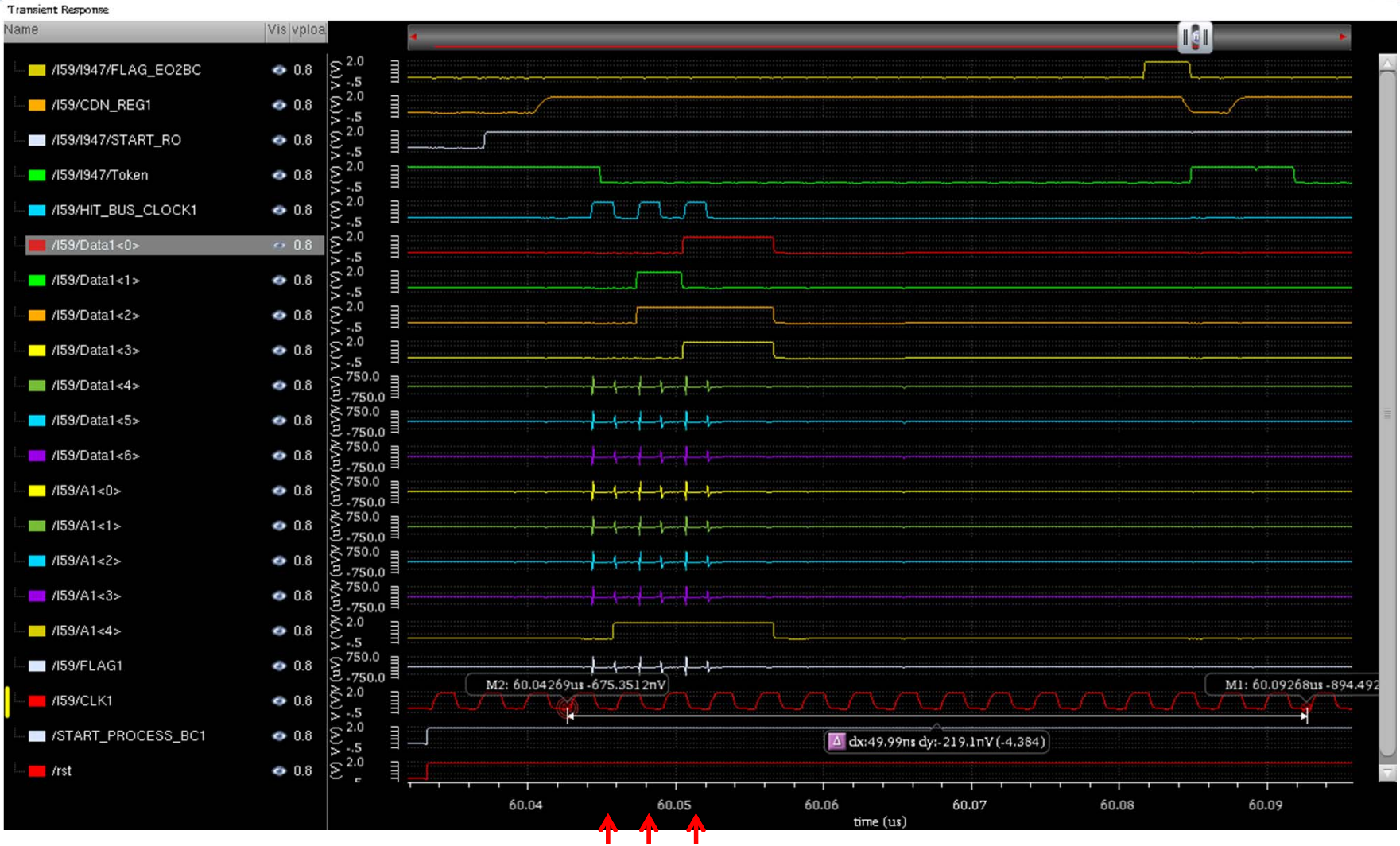
Strip HIT Detect & Address Output



Strip: 0 4 9

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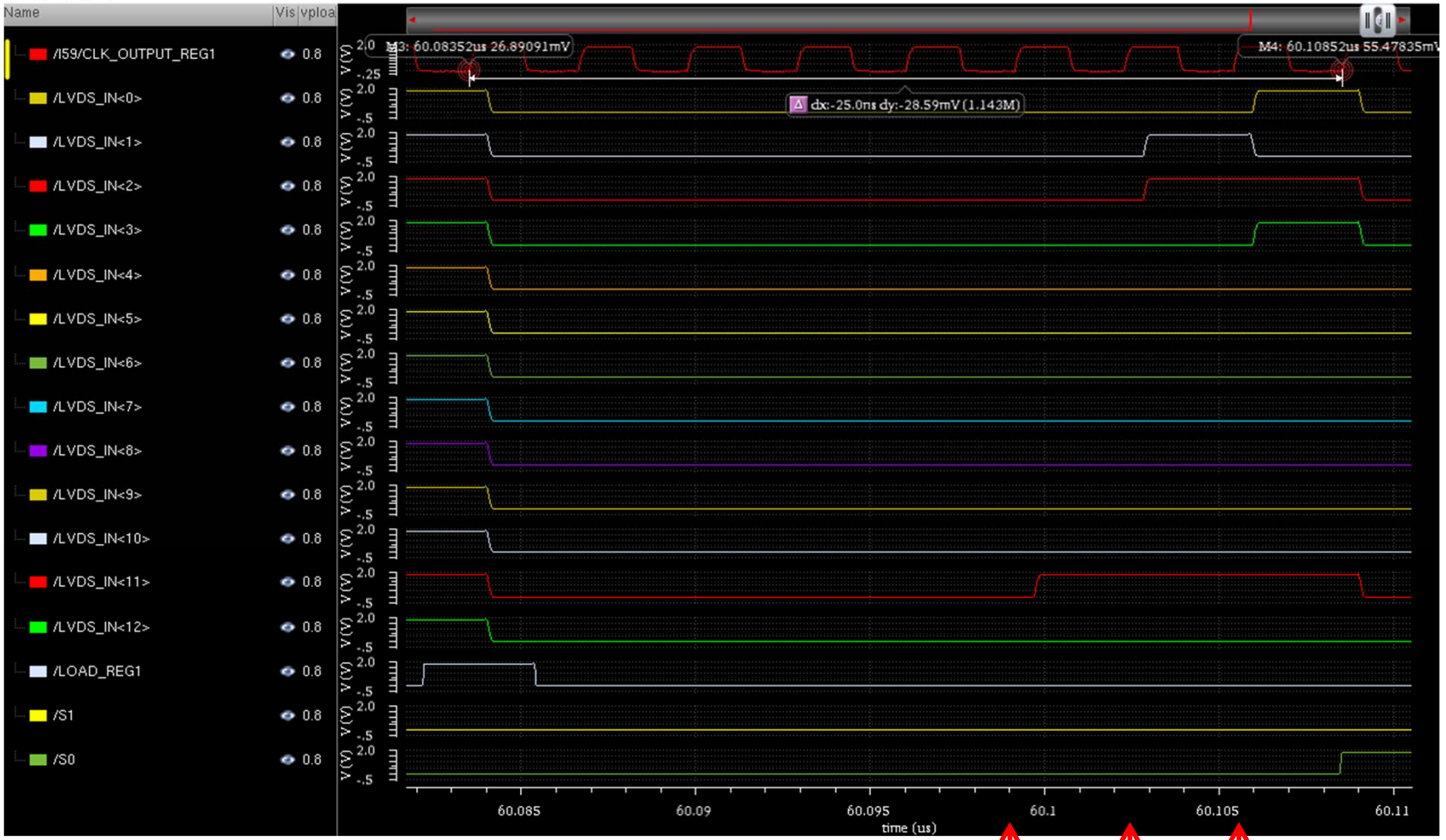
Output to LVDS



Strip: 0 4 9

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Where we are, current status

Block	Schematic	Simulation	Layout	Verification
Pixel/Segment	Partial	Partial	Partial	No
Pre-Amplifier	Done	Done	No	No
Comparator	Done	Done	No	No
Hit Encoding	Done	Done	No	No
Complete Front-end	Done	Done	No	No
Complete Column	Done	Done	No	No
128 Columns	Done	Done	No	No
Strip Encoding	Done	Done	No	No
Data Output	Done	Done	Partial	No
PLL	Done	?	Yes	?
LVDS Rx/Tx	Done	Partial	Partial	No
Calibration	No	No	No	No
Bias DACs	Partial	No	Partial	No
Config Reg/SPI	No	No	No	No
Full Chip	Partial	Partial	No	No

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Final Sensor Additional Blocks

Additional Requirements

On top of the above, the sensor will also require the following features.

- Comparator 4-bit threshold trimming
- Analogue pre-amp channel output for monitoring one channel
- Test Structures (Isolated PreAmps, Passive Pixels, Digital Blocks etc)
- LVDS current control to save power
- Provisions to test CMOS data output transmission