



Science & Technology Facilities Council

Technology

ATLAS CMOS Strip
Regular meeting
01/09/2015

HR-CHESS2 update

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- Almost done with Top-Level schematic simulation, seem to be able to detect and read out up to 8-hits within 1 BX across all process corners from a 32x128 array.
- Plan to start layout of the different blocks early this month, starting with with the digital STRIP encoding block. Still waiting on test results from HR-CHESS1 chip to get an idea of the pixel/segment geometry so hope to start optimisation and layout of the pre-amplifier/analogue front-end for from HR-CHESS2 in early October.
- Plan to organise a Design Review in September, preparing documentation.



1. In the list of spec it was mentioned that the epi thickness is up to $25\mu\text{m}$, is this a strong limit?

No this is not a strong limit, we can increase the thickness to collect more signal.

2. Given your pixel volume are you sure a leakage current tolerance of 10nA is sufficient?

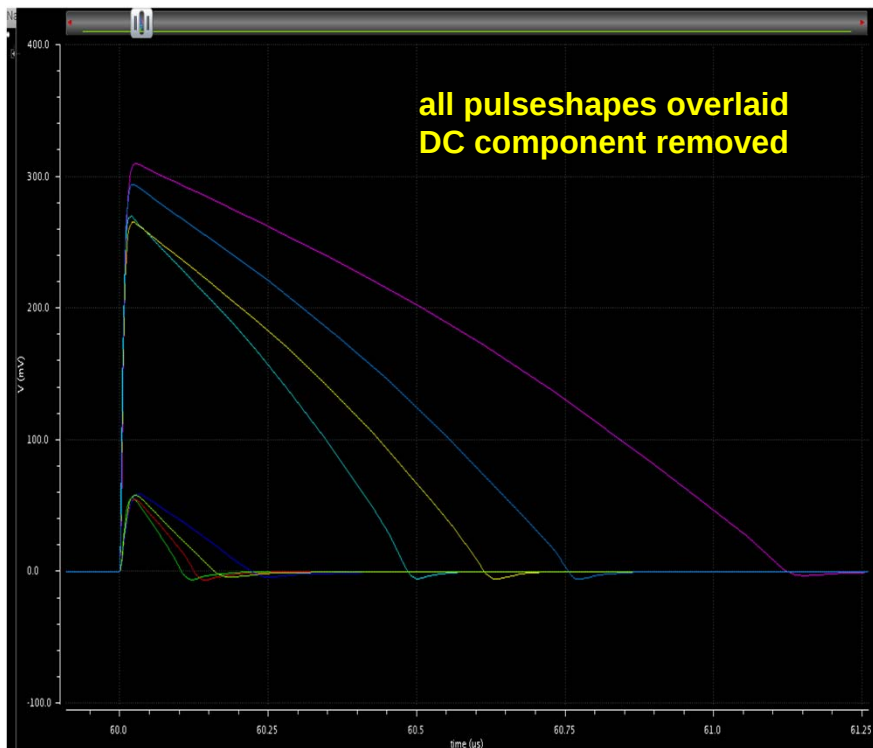
Not completely sure, it is based on what the test engineers measured for similar structures. But the leakage current tolerance of the pre-amplifier increases up to $1\mu\text{A}$ if the temp is decreased to -40°C . See results later.

3. Are you worried about hit-processing in 25ns ?

No. But with the design I have, I can correctly detect max 8-hits if I reserve 2 BX periods for the STRIP ENCODING block. Ultimately I read-out the 8 hits in 25 ns or 1BX. It is a synchronous system and the delay is well characterised for the blocks.

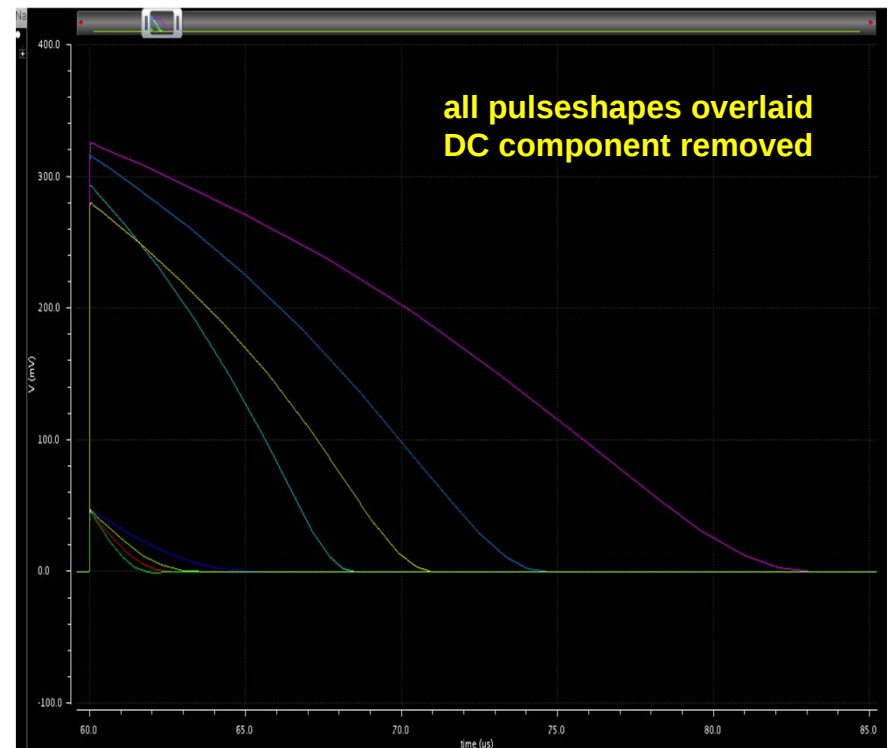


Pre-Amplifier performance



$T = +40^\circ$

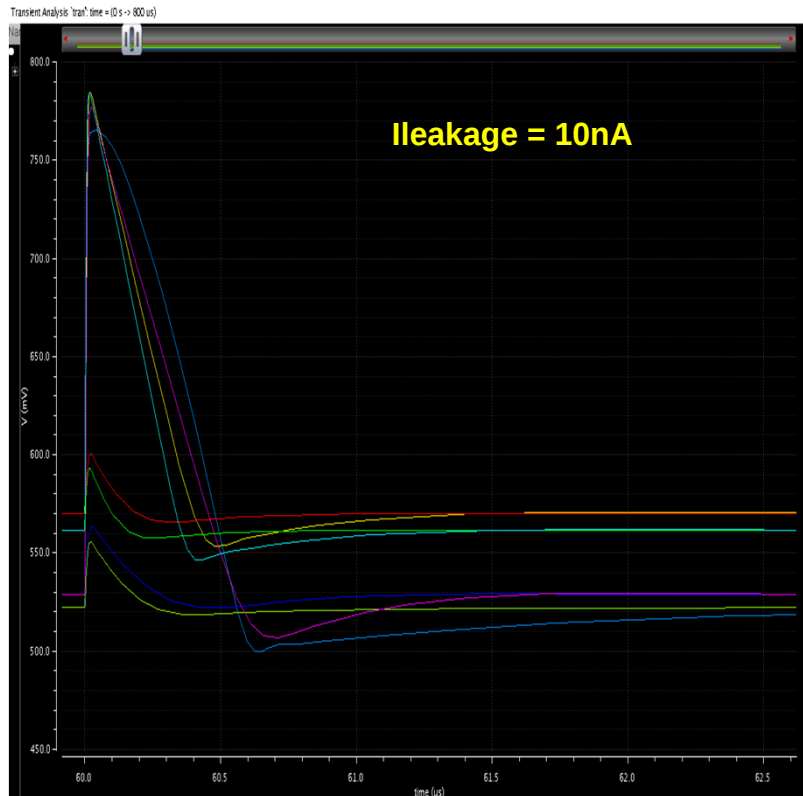
- Signal at Pre-Amp output from 500e⁻ to 5Ke⁻ in 2 steps
- All process corners
- $I_{\text{leakage}} = 0\text{A}$



$T = -40^\circ$

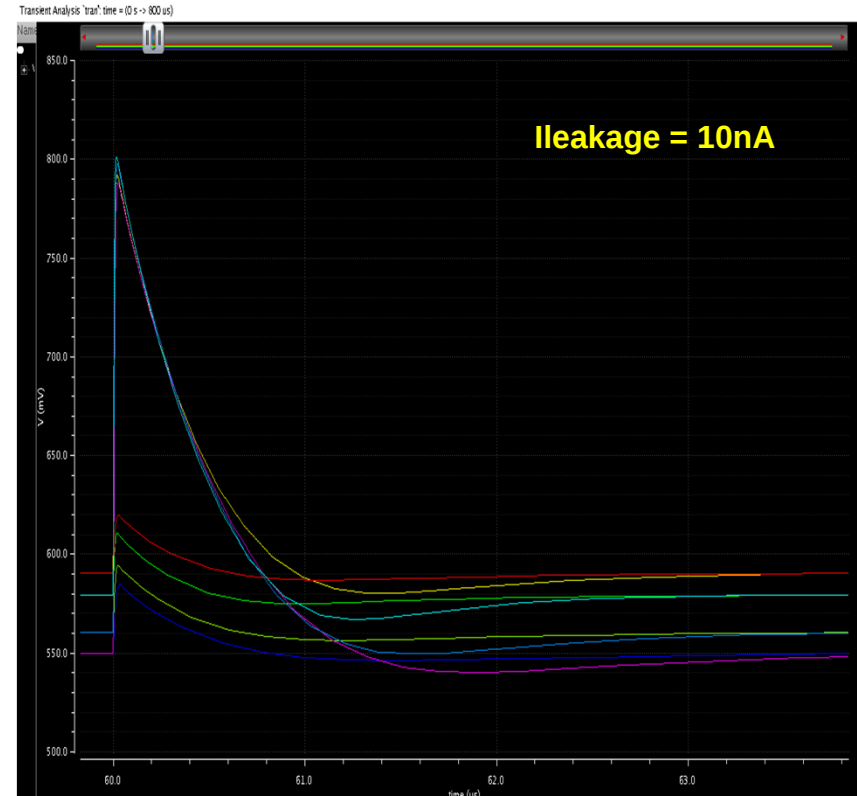


Pre-Amplifier performance with leakage current



T = +40°

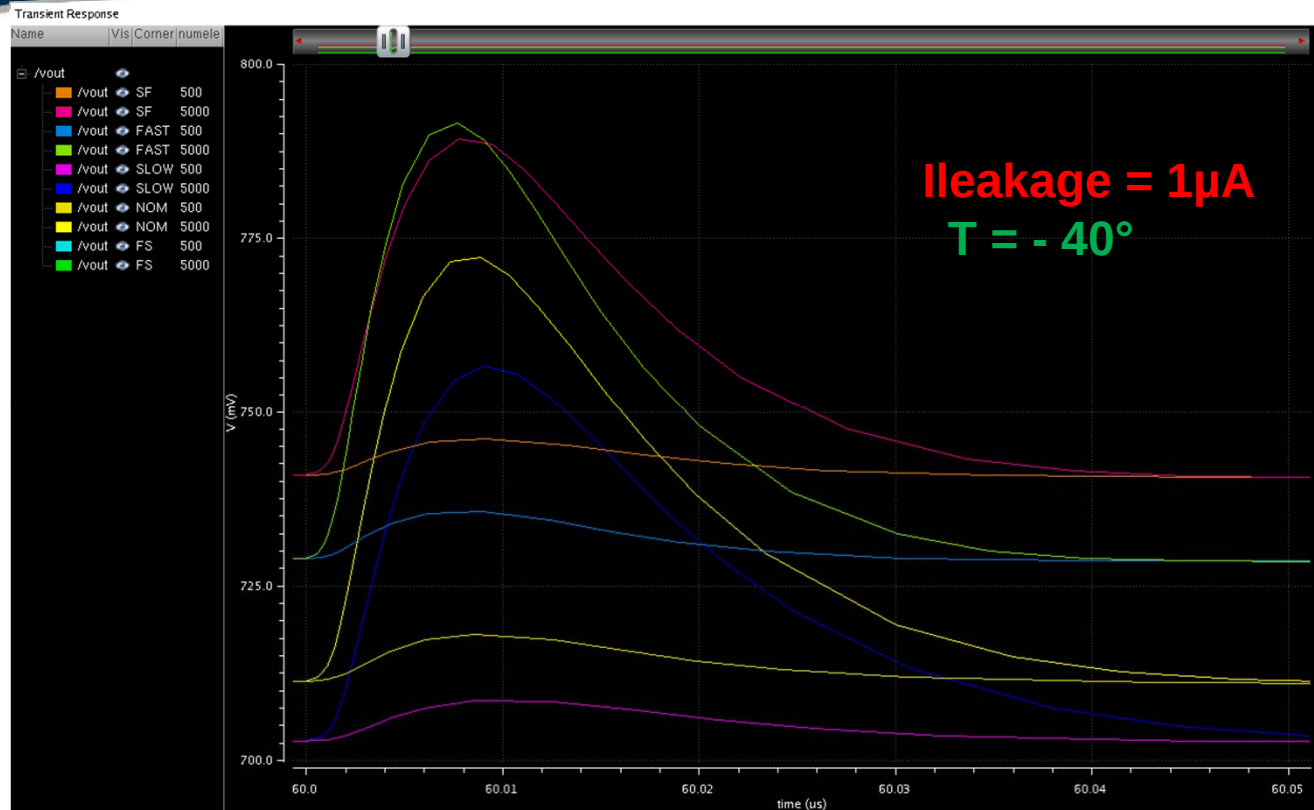
- Signal at Pre-Amp output from 500e- to 5Ke- in 2 steps
- All process corners



T = -40°



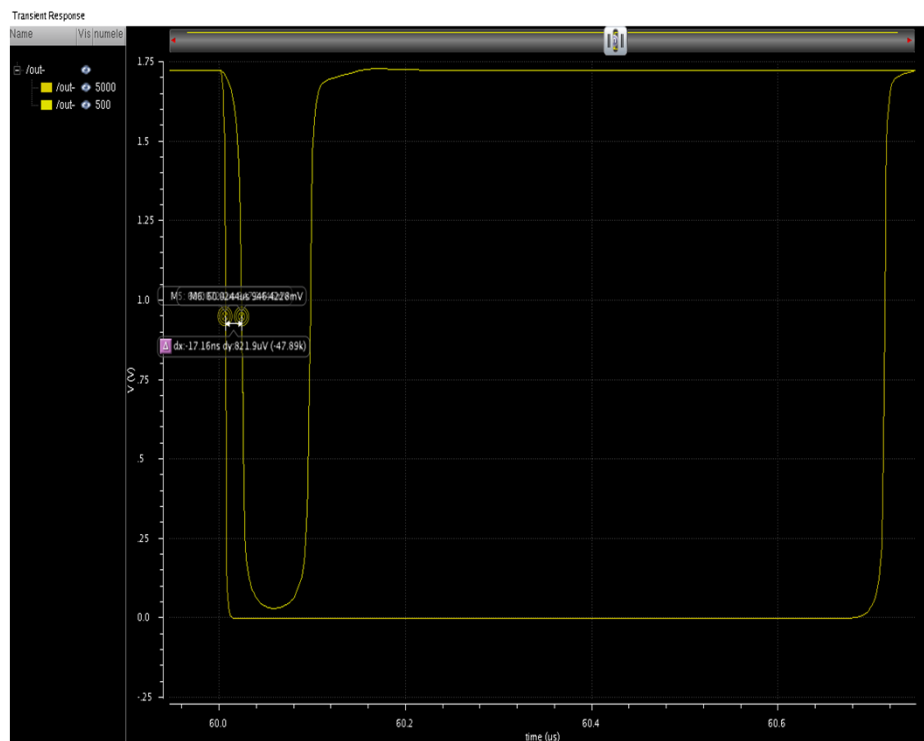
Pre-Amplifier performance with leakage current



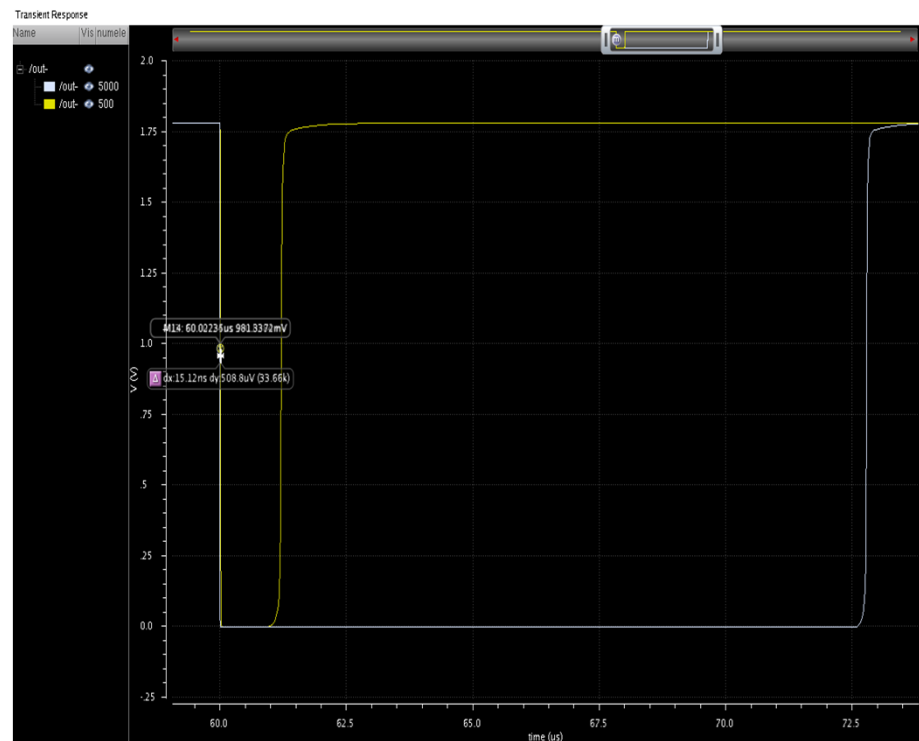
- Signal at Pre-Amp output from 500e- to 5Ke- in 2 steps
- All process corners
- *Gain drops significantly*



Time-Walk at different Temp Nominal Corner

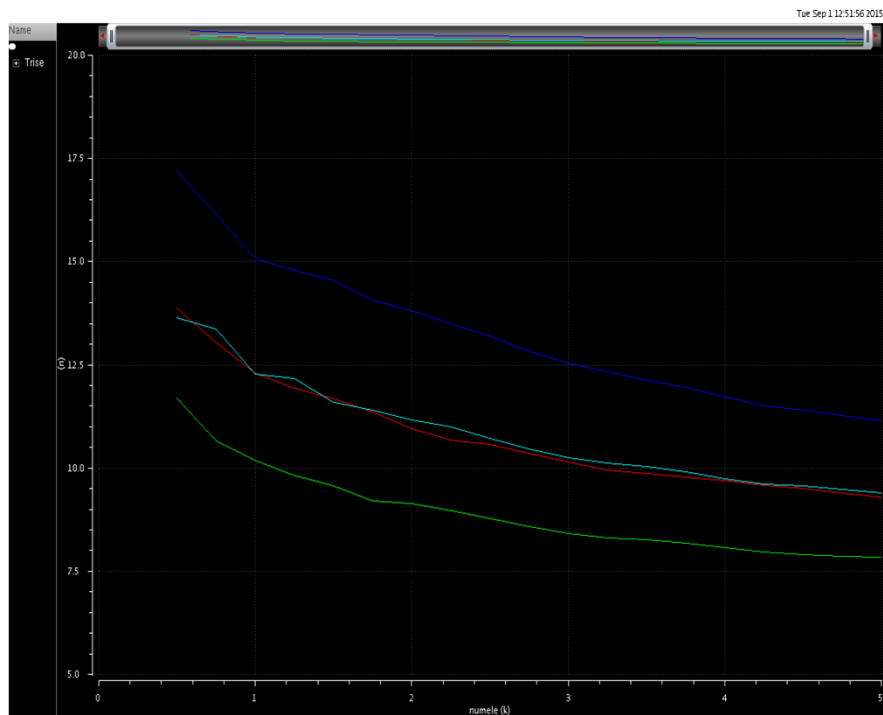


T = +40°
Time-Walk = 17ns

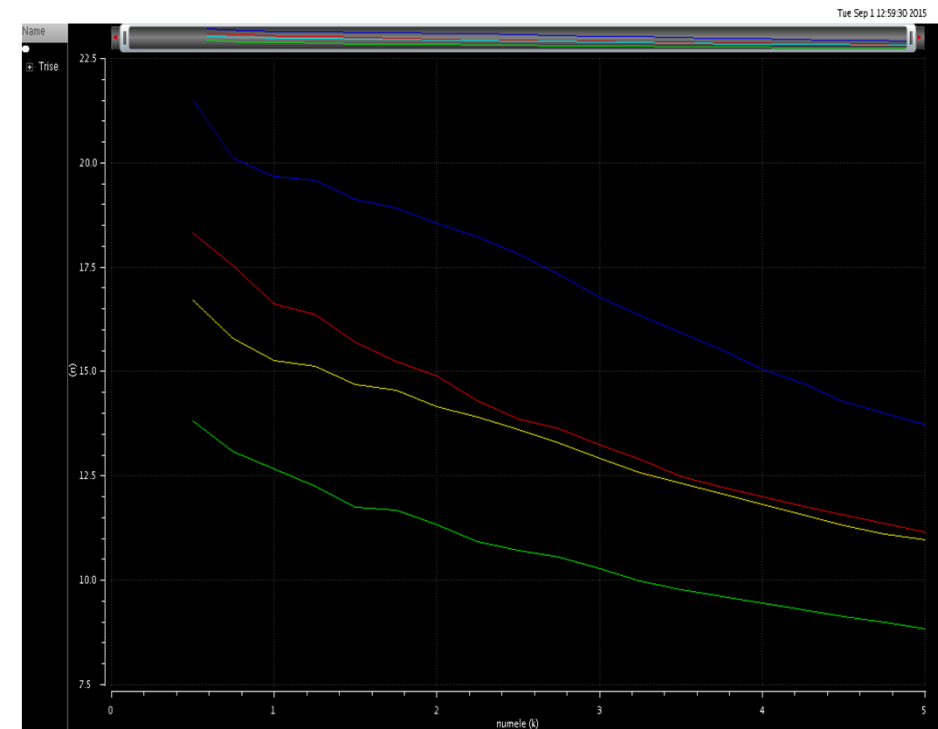


T = -40°
Time-Walk = 15ns

- Comparator output for 500e- and 5Ke- with threshold set at 275e-
- ~1ns charge injection time



$T = +40^\circ$

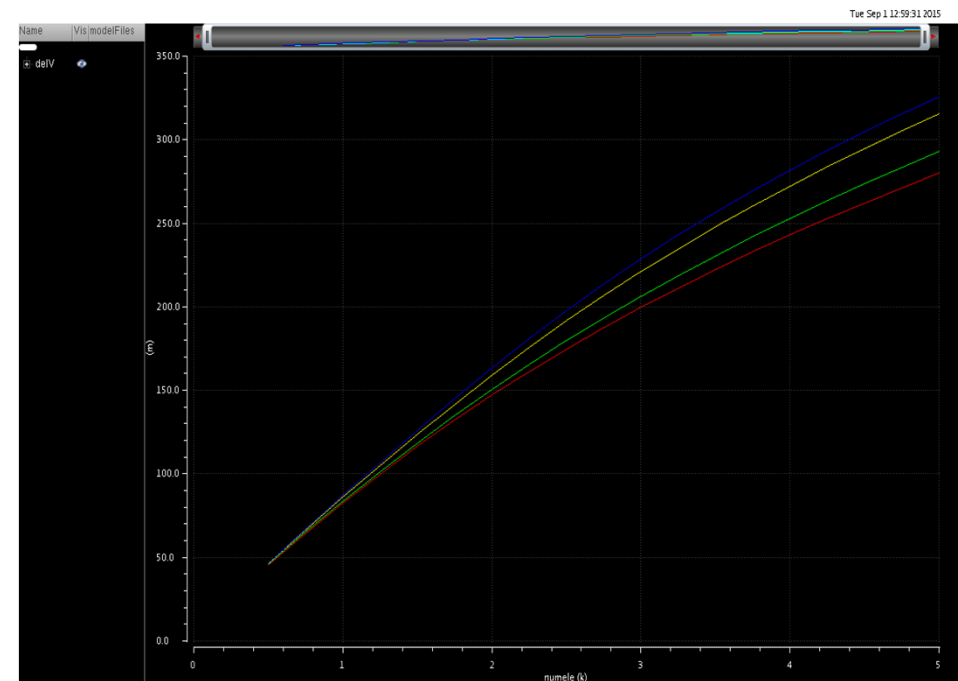
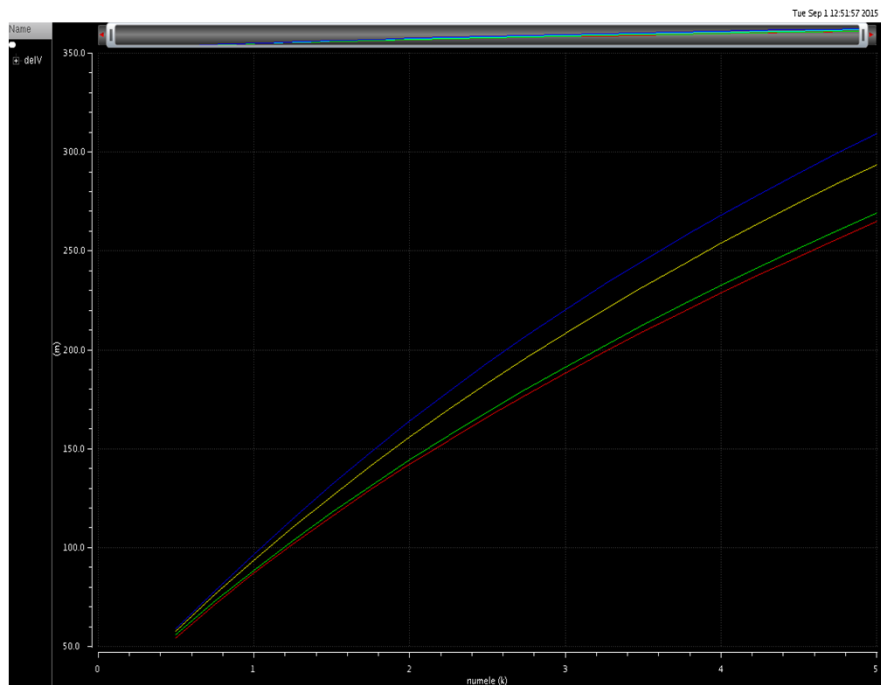


$T = -40^\circ$

- Signal at Pre-Amp output from 500e- to 5Ke- in 250e- steps
- All process corners (NOM, FAST, SLOW, SF, FS)
- I_{leakage} = 0A
- *Trise increases as Temp decrease*



Output pulse amplitude vs signal



$T = +40^\circ$

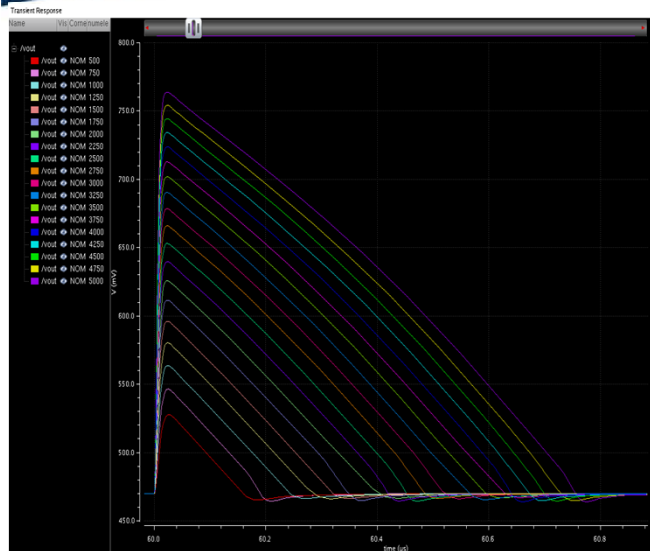
$T = -40^\circ$

- Signal at Pre-Amp output from 500e- to 5Ke- in 250e- steps
- All process corners (NOM, FAST, SLOW, SF, FS)
- *No significant change in gain*



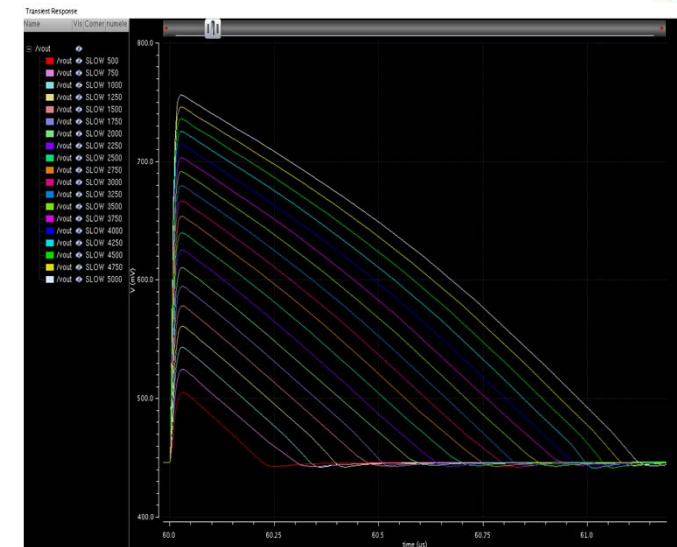
Output pulseshapes vs signal

Temp = +40°



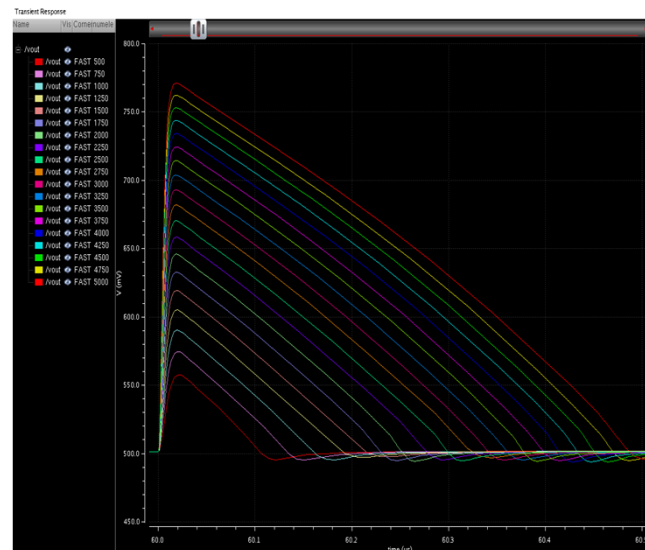
NOM

FAST



SLOW

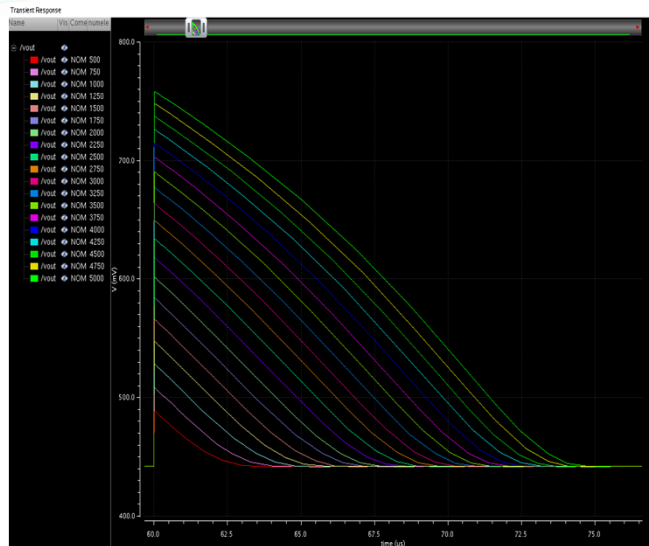
Signal at Pre-Amp output from
500e- to 5Ke- in 250e- steps
Ileakage = 0A





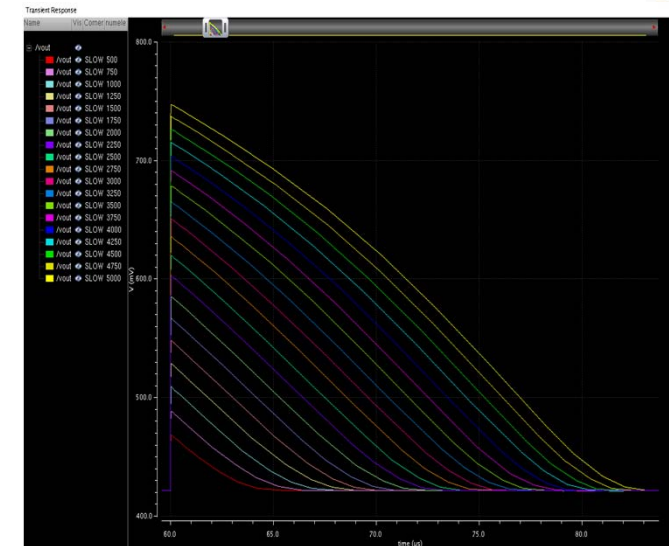
Output pulseshapes vs signal

Temp = -40°



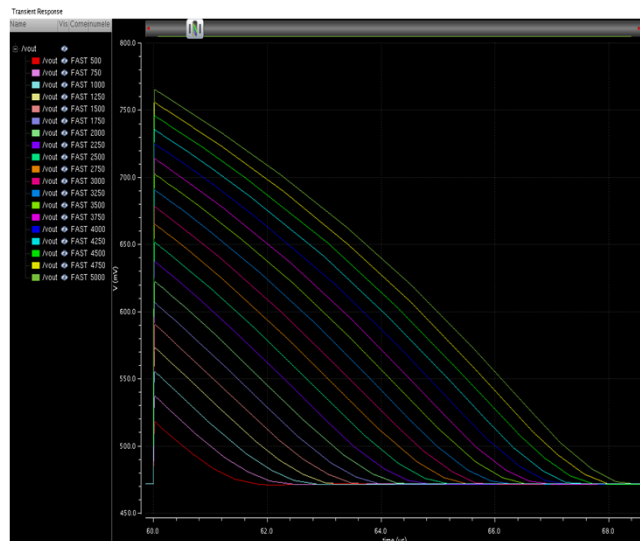
NOM

FAST



SLOW

Signal at Pre-Amp output from
500e- to 5Ke- in 250e- steps
leakage = 0A





- The pre-amplifier seems to be robust across all process corners and temperature extremes

Leakage current: up to 10nA, also looked at 1uA

Temperature: -40°C to +40°C

All functional process corners

- Need to simulate time-walk across all process corners