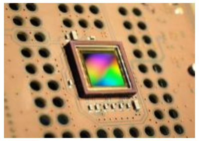

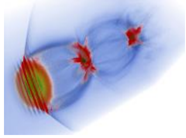

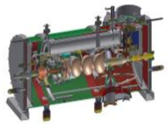

ASICs in HGF – An Overview

Ulrich Trunk

2nd Anual Meeting of the Matter and Technologies Programme
Karlsruhe, 08-10 March 2016

ASIC activities - Outline

Cum Grano Salis…..

ASIC Projects are usually 10..20FTEa and thus take about 5..10 years to complete. This is usually longer than a PoF period. Due to such long term commitments, don't expect things to change too fast! (except for new projects and developments)

Common Technology (TSMC 65nm CMOS) Activities

- TSMC 65nm common Framework
- VULCAN → Talk by Andre Kruth
- SFB Scalability of Quantum Information Processing

Legacy Projects

- Digital SiPM Readout (130nm IBM/GF CMOS) → Talk by Inge Diehl
- GET4 TDC (180nm UMC CMOS)
- HitDetection Transient Recorder (180nm UMC CMOS)
- PhotonV1 Hybrid Pixel Detector Readout (180nm UMC CMOS)
- DSSC Hybrid Pixel Detector Readout (130nm IBM/GF CMOS)
- AGIPD Hybrid Pixel Detector Readout (130nm IBM/GF CMOS)

Projects coordinated by HGF Centres (not covered in this talk)

- Percival CMOS Imager (180nm TowerJazz - RAL) → Talk by Alessandro Marras
- STS-XYTER (180nm UMC CMOS – AGH Krakau)

TSMC 65nm Process Options and available Tools.

Environment

- Linux Version
  - Red Hat (SL6, CentOS)
  - Debian (Ubuntu) optional
- Modules
  - Allows loading and unloading of environments
  - Concurrent use of different tools and versions
  - Used by Cadence support

TSMC 65nm Design Kit & Foundry Access

- Source:
  - CERN (Allows sharing of designs among collaborators – other NDAs do not)
  - Europractice (these are still available for ordering…)
  - Mosis
- Options
  - As CERN kit (LP RF 1P9M silicide lowK…)
  - HV

Schematic Entry and Layout

- Cadence 6.x (OA)
- Current (2015) Europractice release

Digital Flow

- Cadence RC & Encounter (Europractice releases)

Simulation

- Analogue
  - Spectre
  - Ultrasim
  - H-Spice
- Digital
  - Encounter
  - Incisive
  - MMSIM
- We do not need to specify this! Not needed for design exchange. Analogue Artist allows to change simulator in state files

Verification

- Mentor Calibre (latest Europractice release) – sign-off
- Cadence Assura
- Cadence PVE (if deck available)

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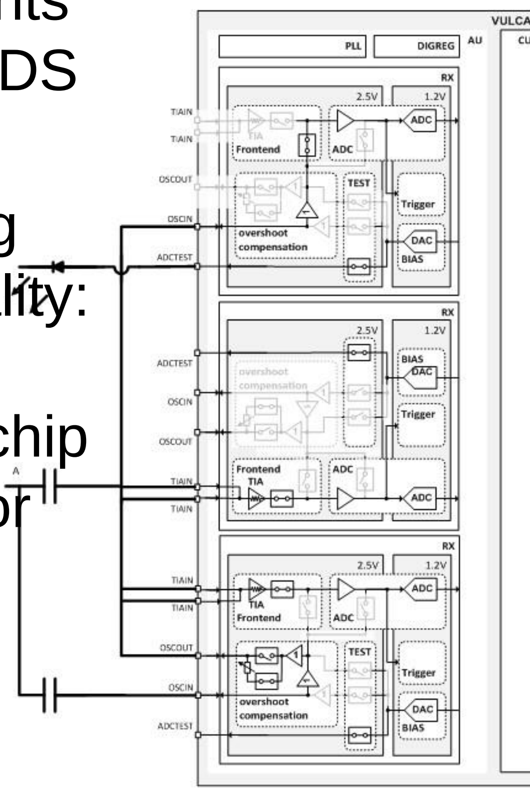
FZJ ZEA-2 ASIC Design Activities 2015 -2016

Matter and Technology 2nd Annual Meeting @ KIT

March 08th 2016 | Dr. Andre Kruth

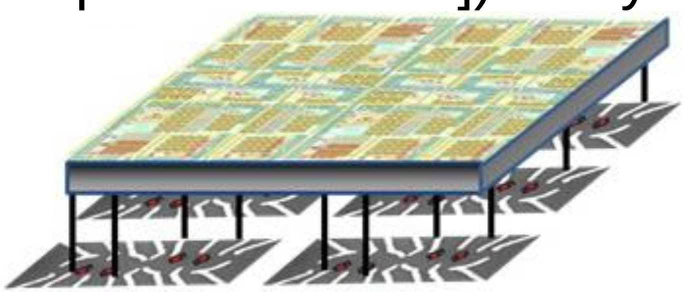
VULCAN – RX Analog to Digital Unit

- Software-defined receiver for charge input detectors (e.g. PMT RX) with a high linearity mode or three parallel receive chains with 1GS/s ADCs
- First demonstrator with individual components (4GHz VCO, ADC, Front-end amplifiers, LVDS interface) taped-out June 2015
- First prototype of full receive chain including digital data processing (additional functionality: data reduction, error correction, calibration, build-in self-tests, PLL, JTAG-Interface for chip configuration, digital to analog converters for reference voltage generation) planned for June 2016

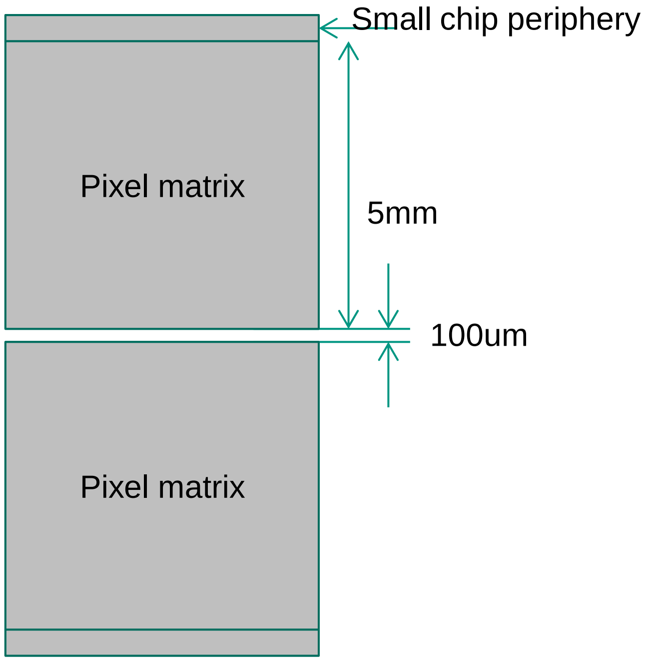


SFB Scalability of Quantum Information Processing

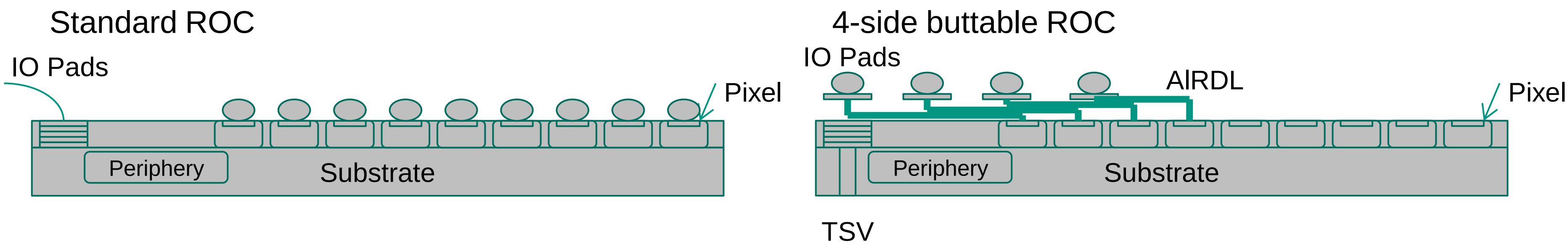
- Application for DFG common research center (SFB) headed by RWTH Aachen in collaboration with FZJ
- Goal: Pave the way for a quantum information processor
- SFB review took place Dec. 2015 – funding decision expected for May 2016, SFB potential start July 2016
- Task for ZEA-2: System and concept development for an electrical low-power scalable qubit operation unit (static bias, RF manipulation, [read-out of quantum states]) in cryogenic environment



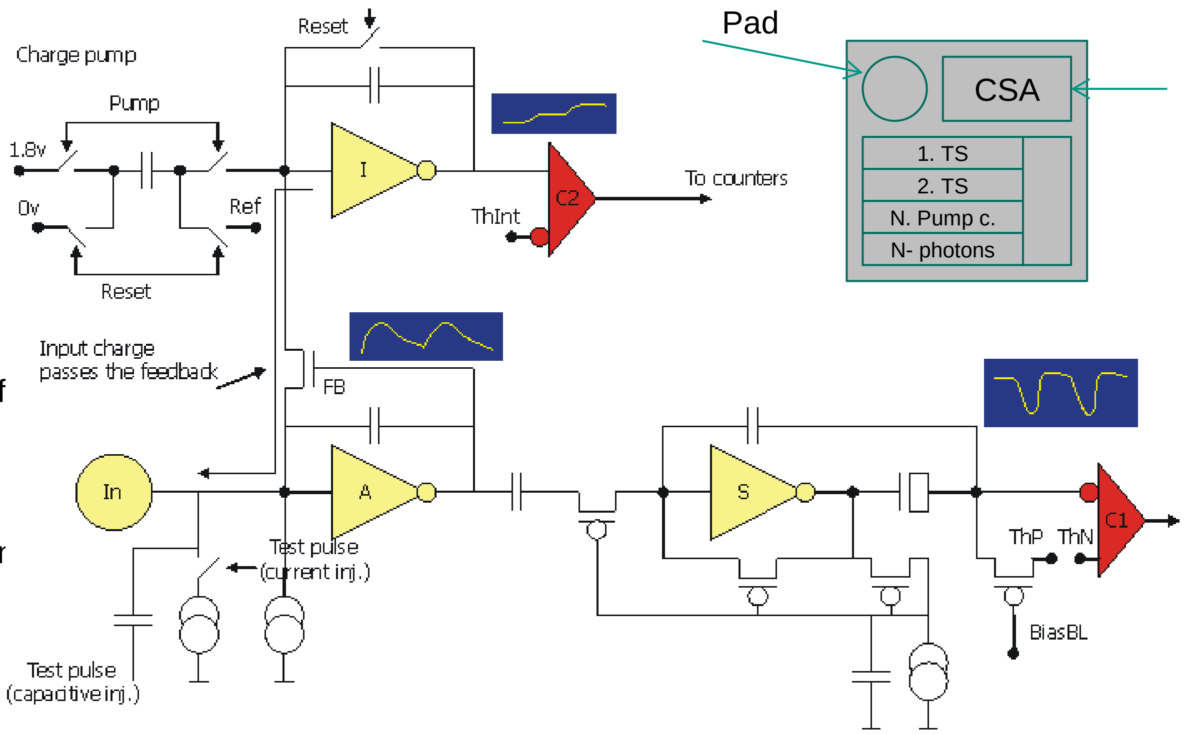
- PhotonV1 pixel readout ASIC – submitted in November ‘15 as engineering run in UMC 180nm MMRF process. The chips have been produced, will be tested soon. The run has been shared between several projects and institutes (Belle, EDET, PETA, SPADIC, MPI, HLL, Heidelberg, KIT)
- The wafers produced by UMC will be post-processed by adding an extra aluminum redistribution layer (AlRDL) and SnAg bumps
- Several wafers will be produced without bumps/AlRDL, leaving the possibility for different post processing
- The chip size is 5m x 5m and there are two chips placed at the reticle



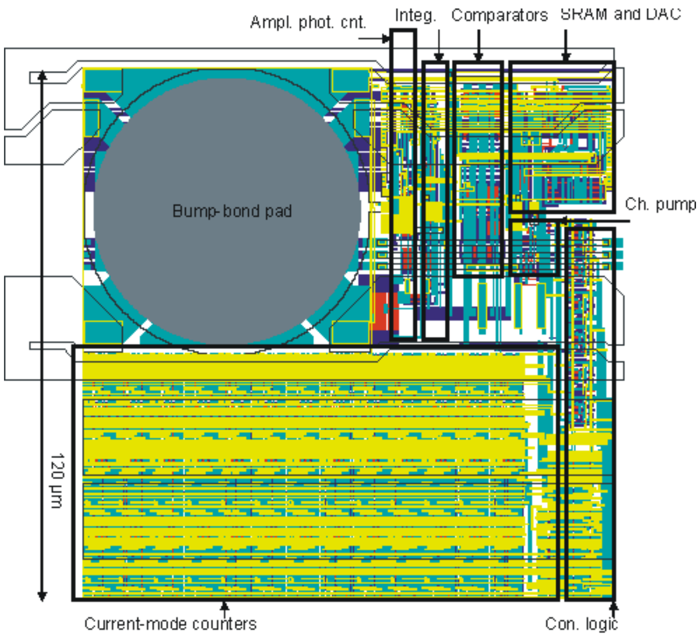
- When AlRDL is used, one of the chips is 4-side buttable
- The power and IO pads are implemented in the way that they can be easily accessed using through-silicon vias (TSV). The TSVs could be produced e.g. by Fraunhofer IZM institute in Berlin



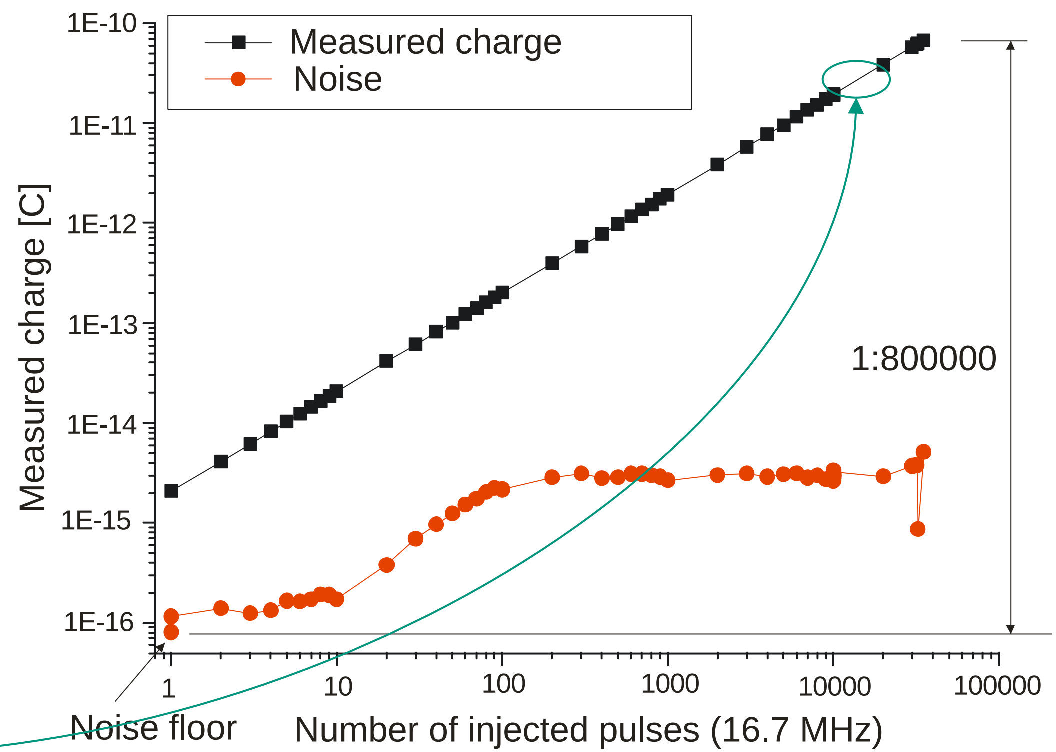
- The PhotonV1 chip contains a pixel matrix of 34 x 34 pixels. The pixel size is 150 µm x 150 µm. The pixel electronics allows simultaneous **counting of photon signals** and **integration of total charge** generated by the sensor. The integrator is a special high dynamic range integrator
- The use of two-fold measurements – number of particles and charge integral are determined – can have many benefits.
- Increased dynamic range: Photon counters usually work better for low photon flux and integrators for high intensities
- In the overlap region where both counting and integrating work, it is possible to determine the average photon energy. This can be used to improve the image quality in the case of medical imaging
- In the case of application in FEL, the high dynamic integrator can allow the detection of the number of photons in an x-ray pulse
- Every pixel contains a low-noise charge sensitive amplifier CSA, a 13-bit counter counts the photon pulses
- The charge pulses bypass the CSA (thanks to novel feedback circuit) and are received to the integrator
- When integrator signal exceeds a certain threshold a reference charge packet is subtracted from the input
- The time difference between the first and last subtraction is measured and the number of subtractions is counted
- Such a two-dimensional quantization allows a high dynamic range



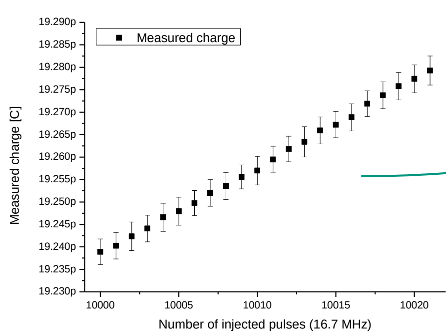
- To decrease crosstalk, the pixel logic has been implemented using differential current mode logic cells
- Continuous readout (both integrating and counting part) should be possible. The readout of one frame in ~ 20µs should be possible according to simulations



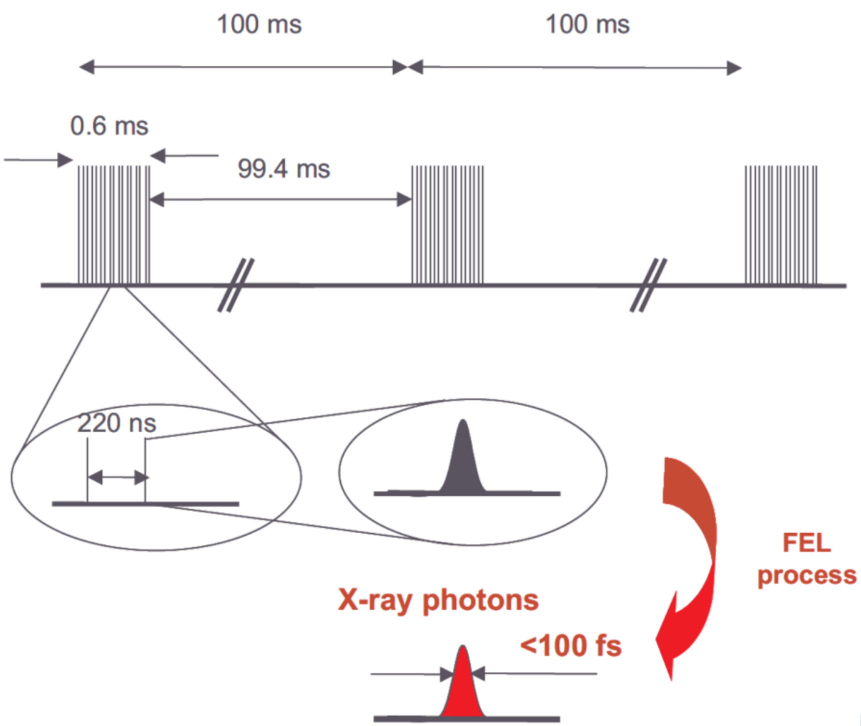
- Measurements with a smaller prototype



Integration time: 2.5ms.

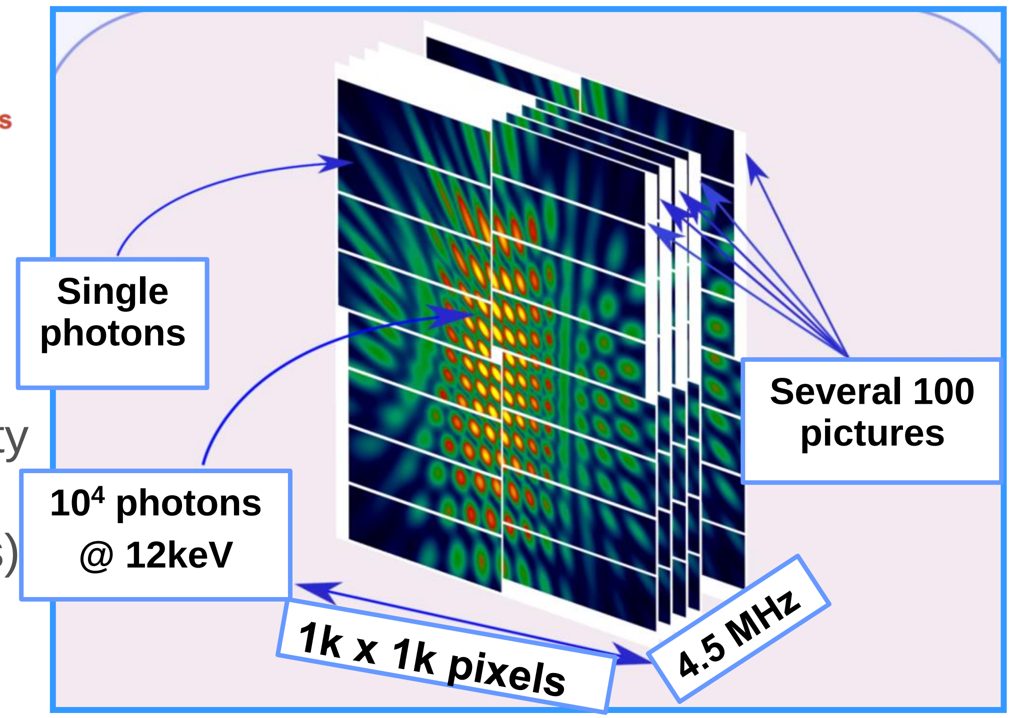


Detector challenges of



Photon density at XFEL is too high for photon counting detectors.

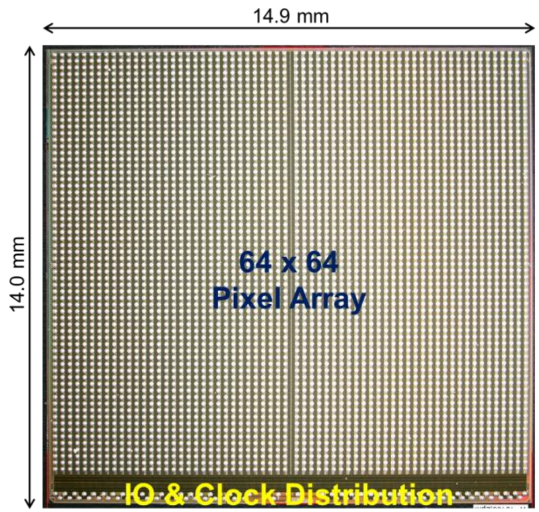
Development of an integrating hybrid pixel detector:



Key features of the European XFEL

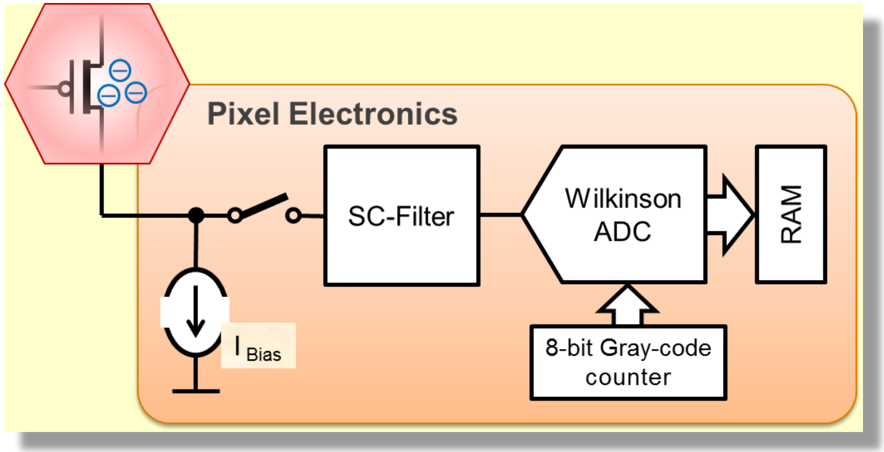
- Very high peak brilliance and intensity (>10^{13} pht/pulse)
- Highly coherent fast pulses (< 100 fs)
- 4.5 MHz pulse repetiton rate
- 2700 pulses per train

DSSC-Readout ASIC.



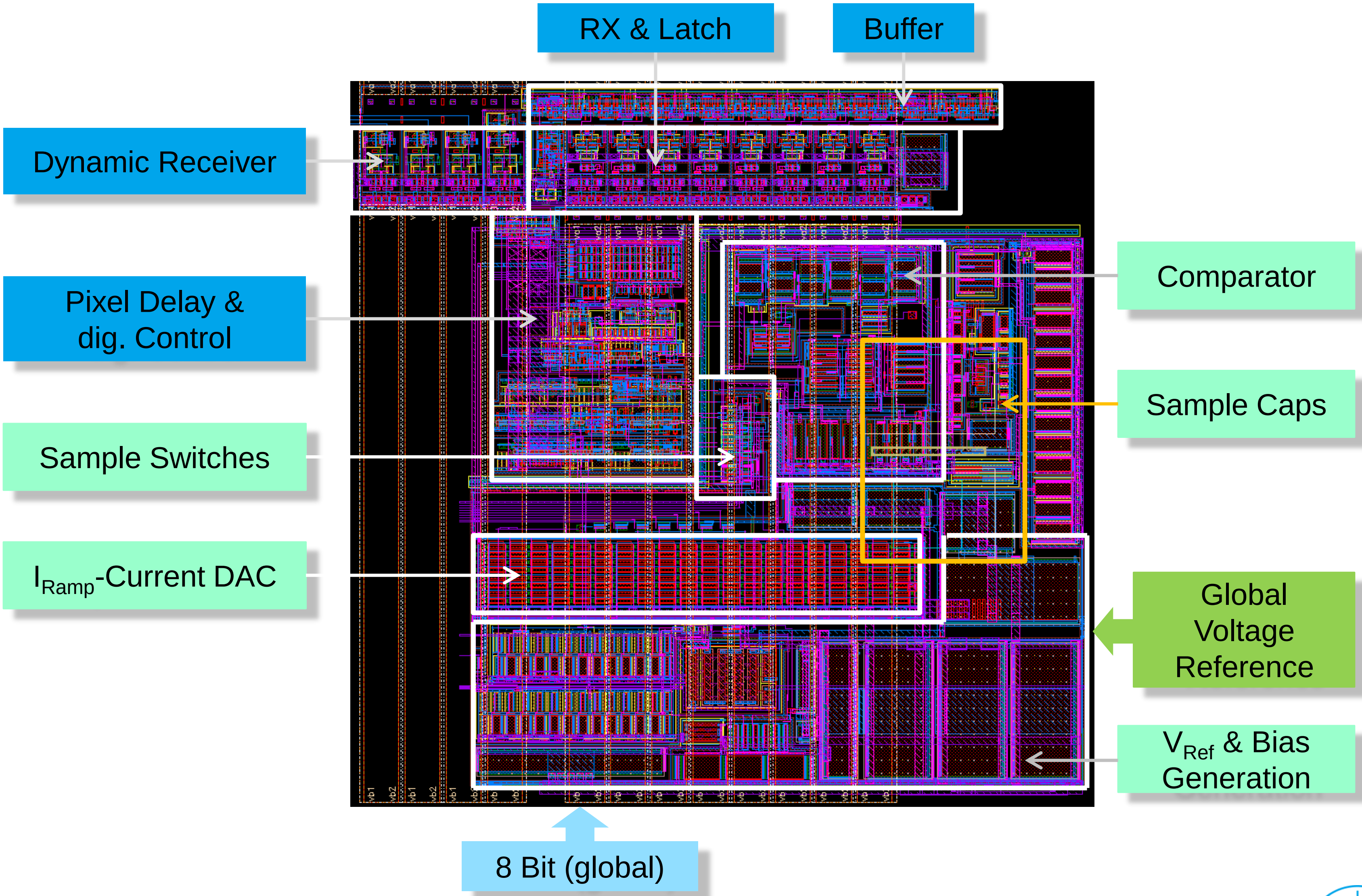
Collaboration

- Politecnico di Milano
  Front End / Filter Design
- Universita di Bergamo
  LVDS Pads / Injection Circuitry
- University of Heidelberg
  SRAM, Integration & Chip Control
- DESY-FEC Hamburg
  ADC Design



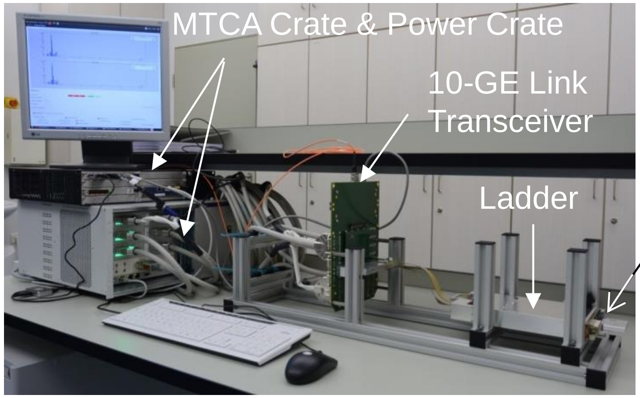
- IBM 130-nm CMOS
- 4096 Pixels
- 220 x 230 μm^2 Pixel Size
- Current Readout of DEPFET
- Trapezoidal Filter
- 8-bit Single-Slope ADC
- 5-MHz Frame Rate
- SRAM for 800 Frames

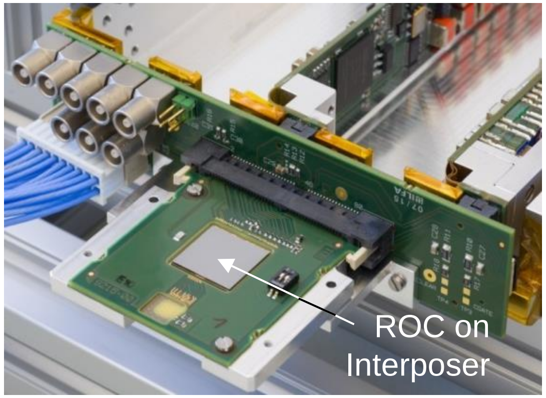
DSSC-Readout ASIC.



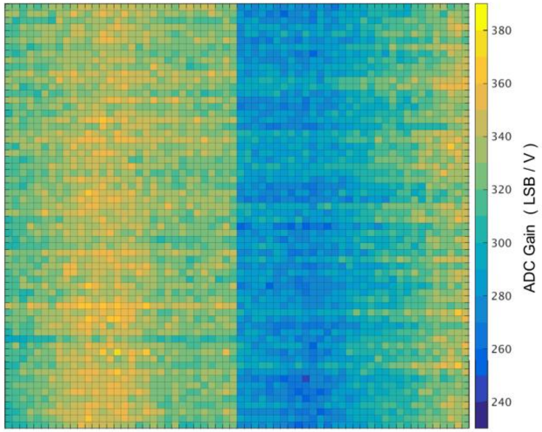
DSSC-Readout ASIC.

Ladder Camera

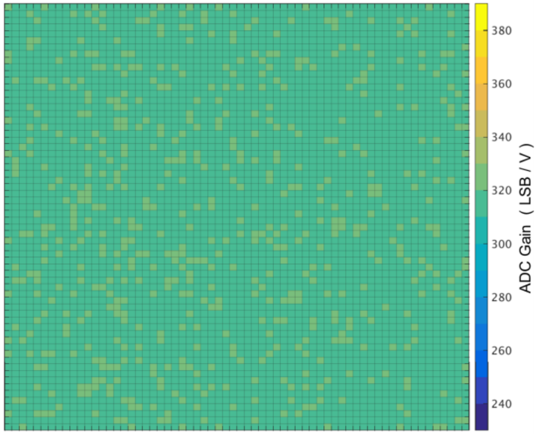




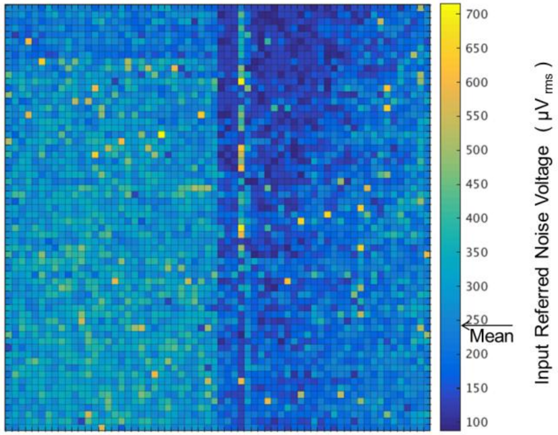
Dark Images @ 5-MHz Frame Rate



before gain trimming

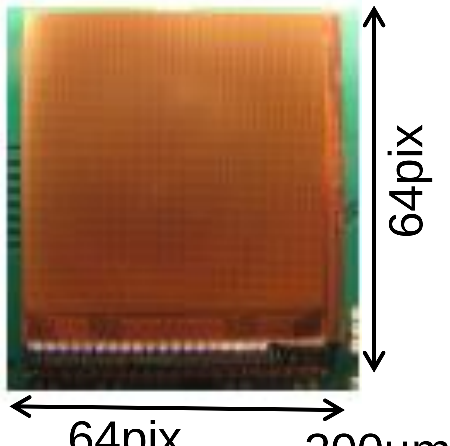


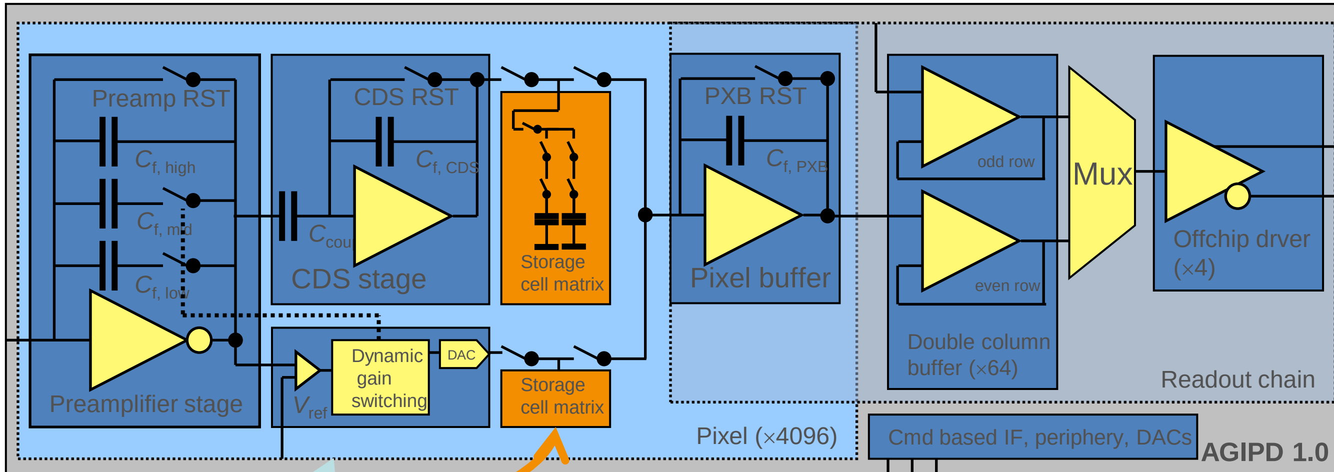
after gain trimming

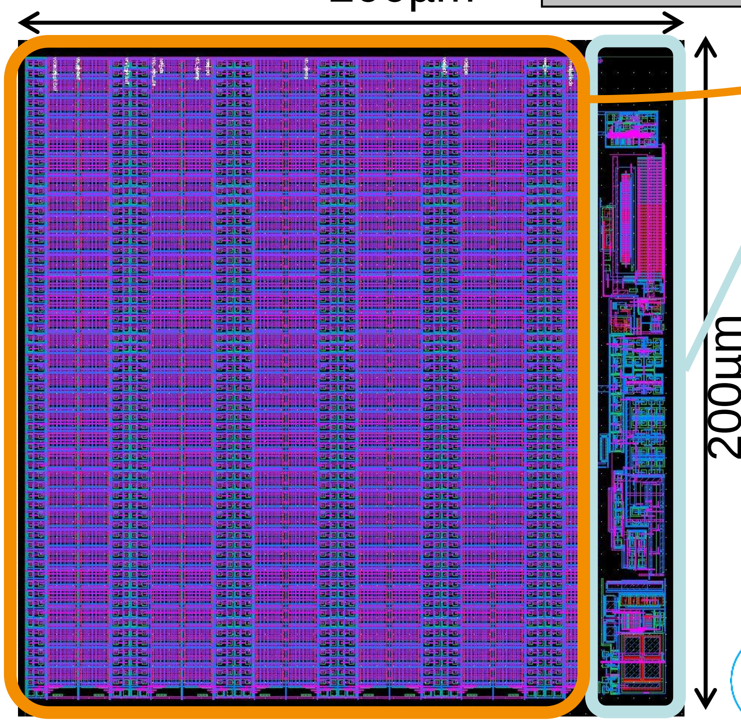


Mean in LSB: ~8 %

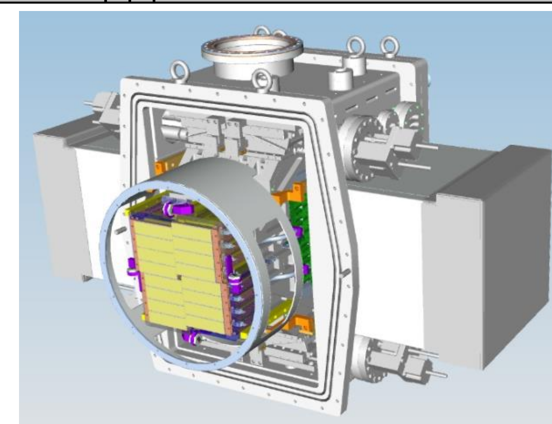
AGIPD –
Adaptive Gain Integrating Pixel Detector





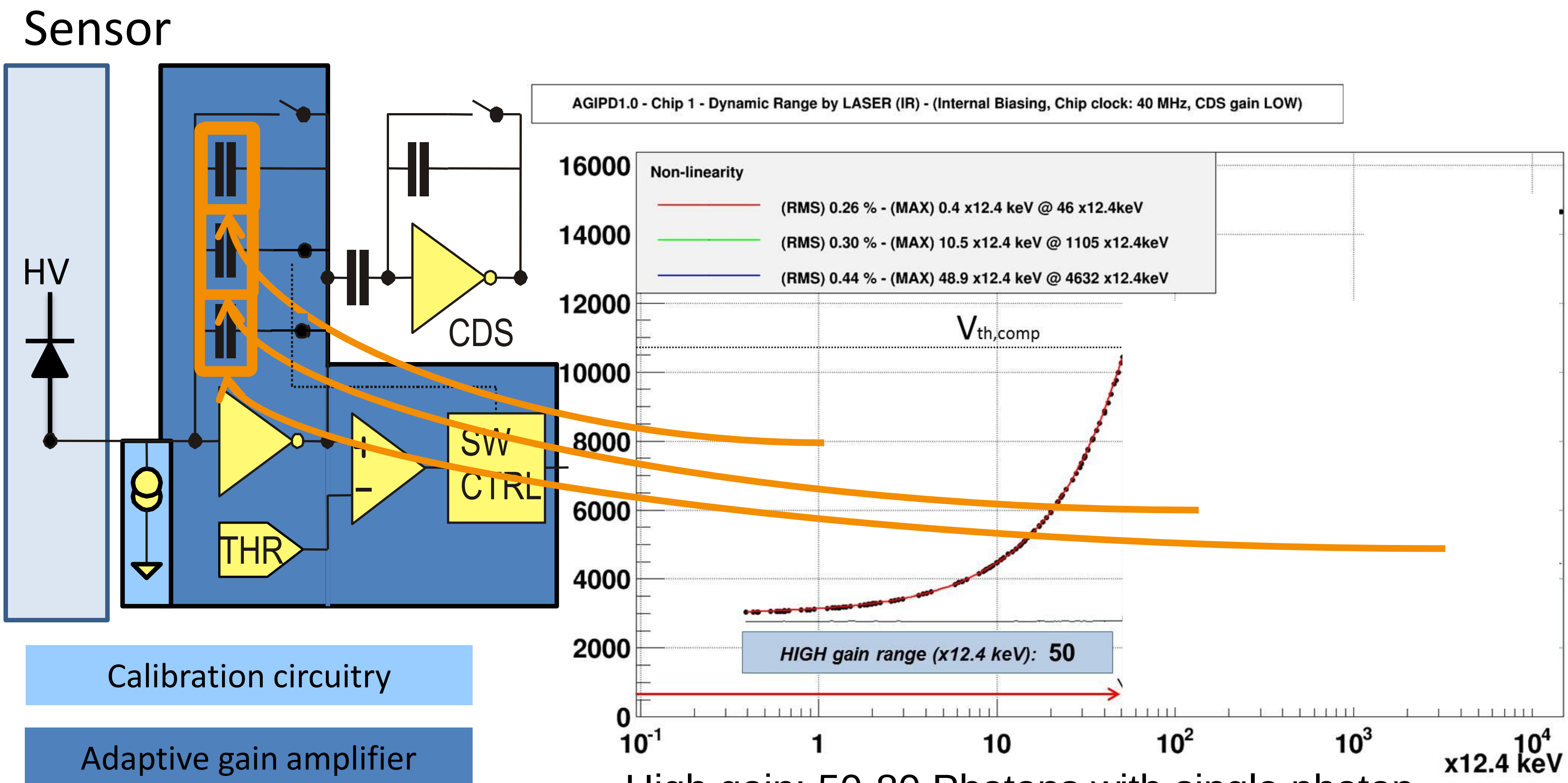


- IBM/GF 130nm
- 64 × 64 pixels
- 200 × 200 µm² pixels
- 352 storage cells + veto capabilities.
- 4.5 MHz frame rate
- Dynamic range from
  - ≈300 e⁻ (0.1 photon of 12.4keV) to
  - ≈33 10⁶ e⁻ (10⁴ photons of 12.4keV)
- Radiation hard design



DESY PAUL SCHERRER INSTITUT PSI Universität Hamburg universität bonn

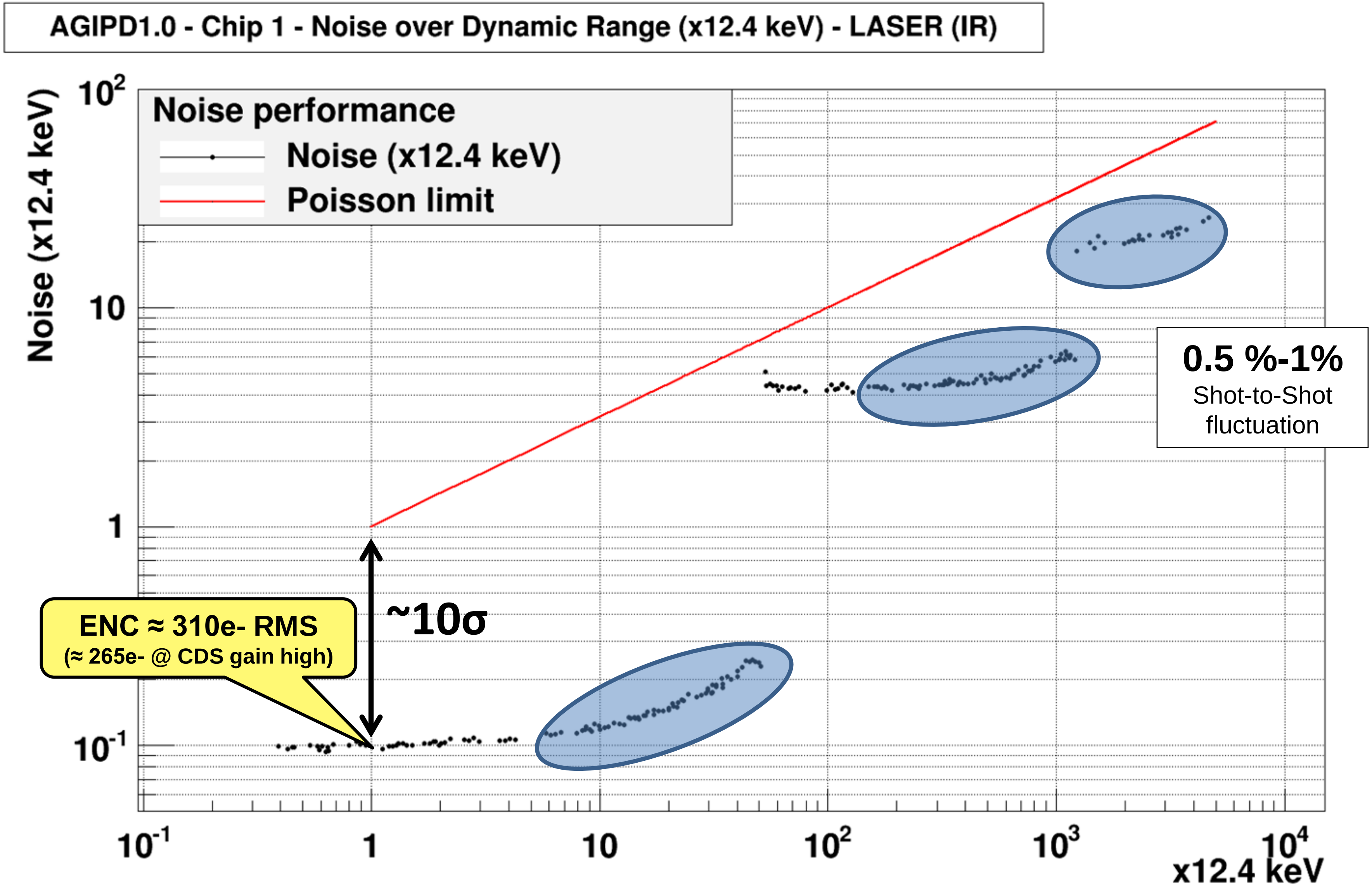
Adaptive gain switching



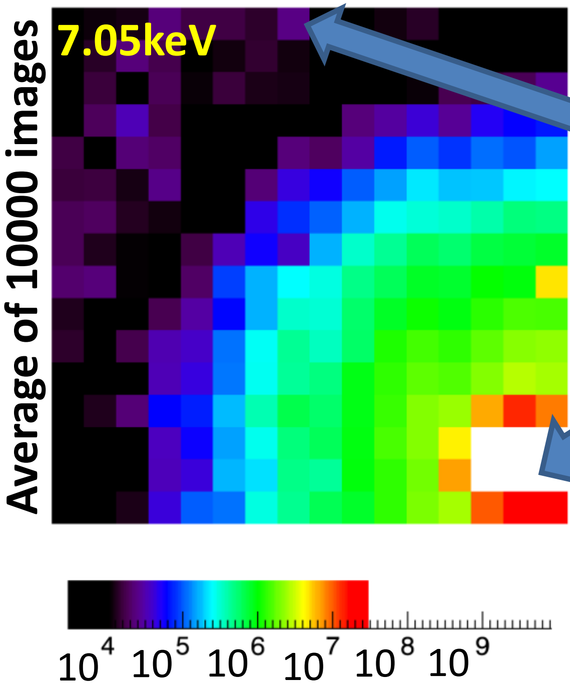
High gain: 50-80 Photons with single photon sensitivity.

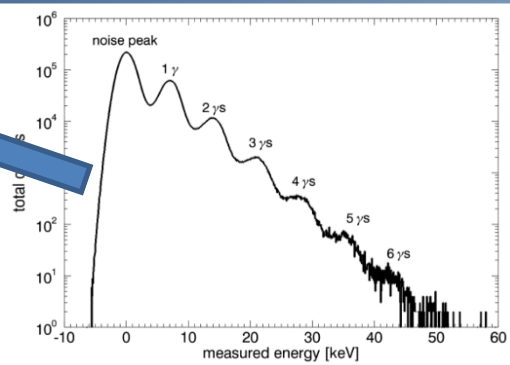
Low gain: 5000 photons with linear gain +5000 photons with 1% nonlinearity.

AGIPD Detector noise

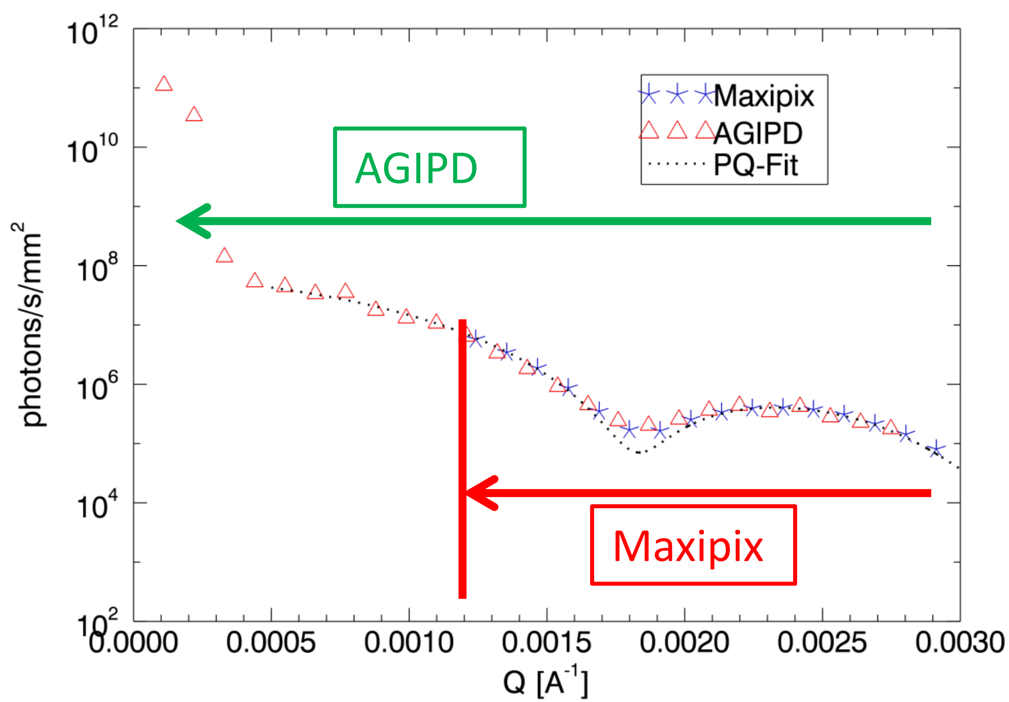


AGIPD Dynamic Range: Small angle scattering of colloidal particles





Direct beam (10^{11} Ph/s)



J inst PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: March 11, 2013
ACCEPTED: May 22, 2013
PUBLISHED: June 12, 2013

Performance tests of an AGIPD 0.4 assembly at the beamline P10 of PETRA III

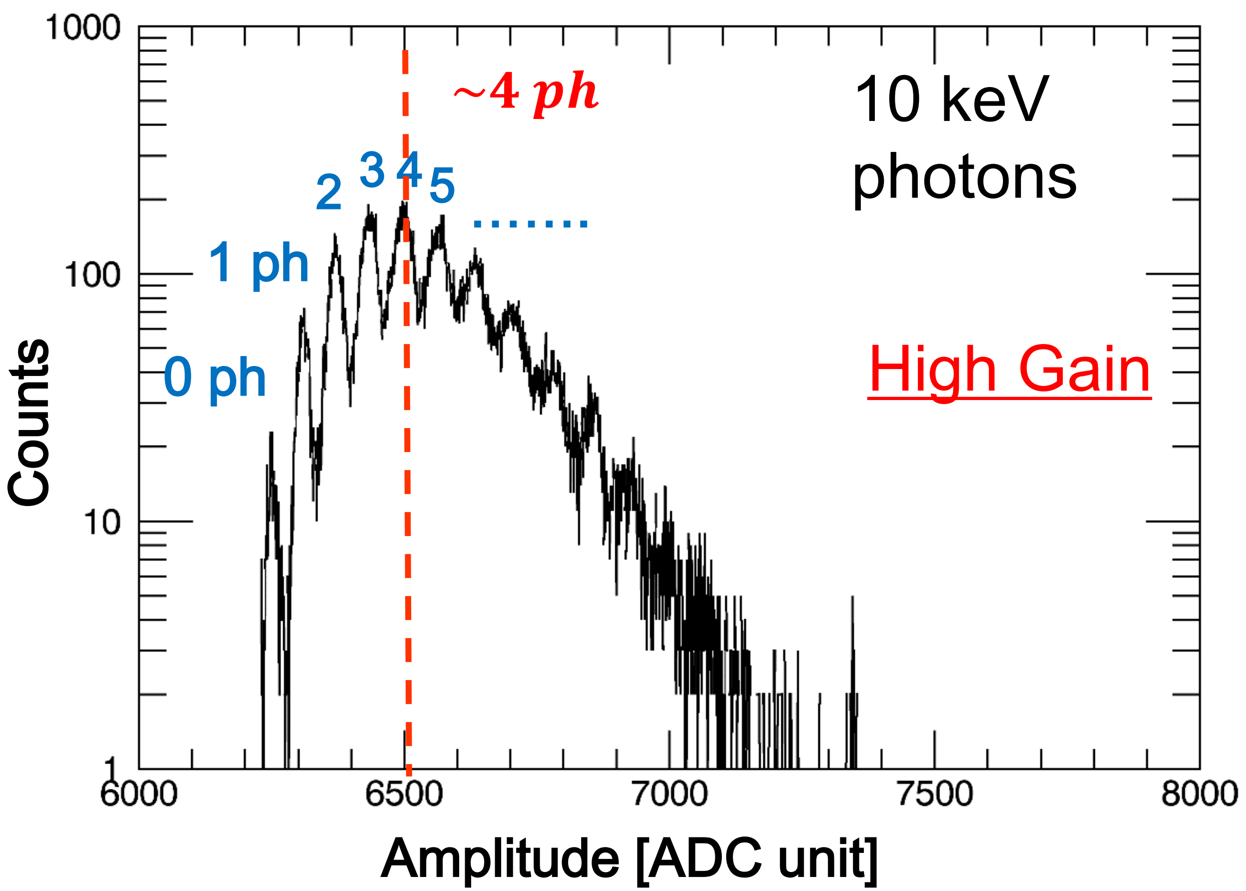
J. Becker[a,1] A. Marras,[a] A. Klyuev,[a] F. Westermeier,[a] U. Trunk[a] and H. Graafsma[a,b]

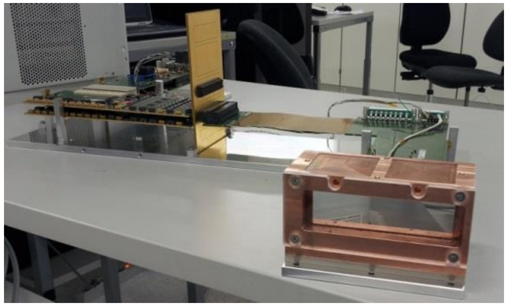
[a] Deutsches Elektronen-Synchrotron (DESY), Notkestr. 85, 22607 Hamburg, Germany
[b] Mid Sweden University, Holmgatan 10, S-85170 Sundsvall, Sweden

Single photon sensitivity of the AGIPD FEM

- Beam focussed on a single pixel (by means of K-B Mirrors)
- Beam attenuated with aluminum foils

@6.5 MHz!
(@10 keV)





6.5Mhz frame rate at APS

Result from laser mea

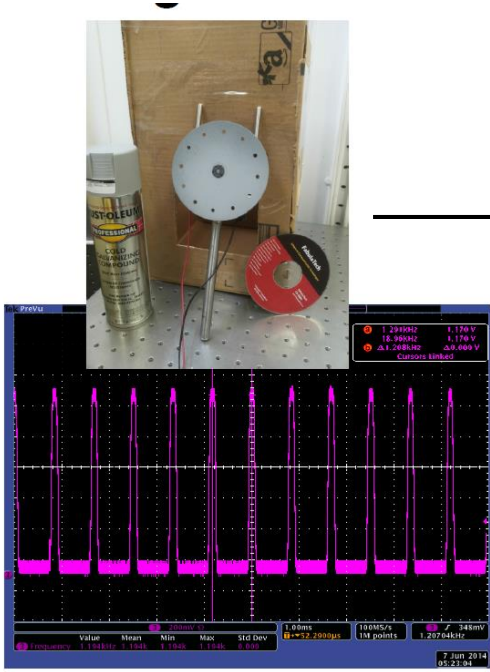
Single bunch imaging – a challenge to find processes fast enough

Experimental setup

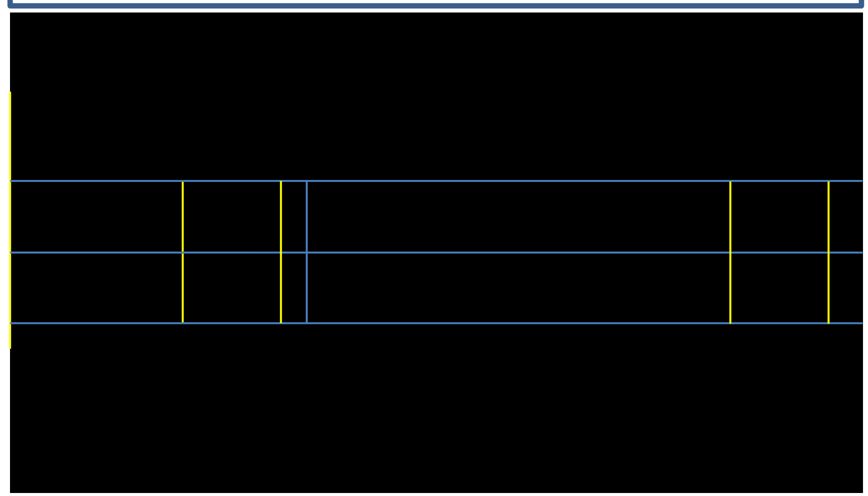
- Drilled equidistant holes into a DVD
- DVD painted with zinc to increase absorption
- Mounted DVD on a fast electric motor
- Measurement of hole to hole frequency
- with diode and oscilloscope: 1.208kHz

Calculation for burst imaging

- APS bunch spacing: t = 154ns
- Number of pixels crossed during burst of 352 images: ≈ 8
- Pixel size: 200µm



V_{disc}, AGIPD = 29.51m/s
≈ V_{disc}, Laser = 29.83m/s



Thanks to Robert Bradfort and Antonino Miceli *et al.* from APS

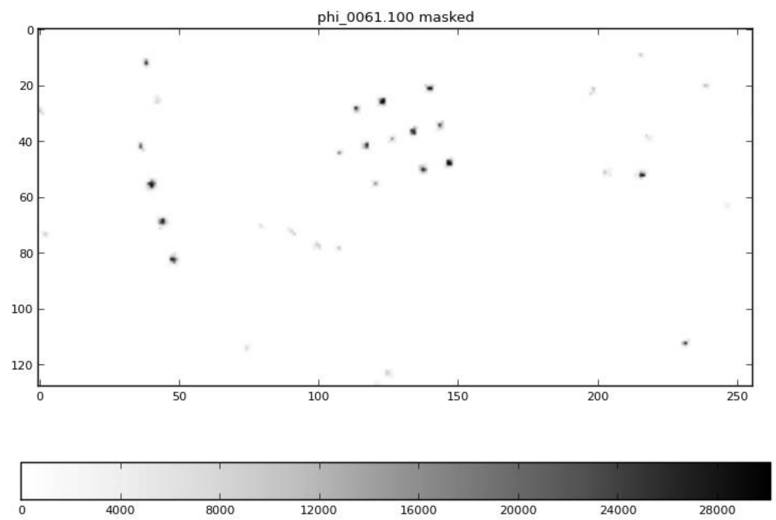
Single bunch imaging is possible even at a repetition rate of 6.5MHz!!

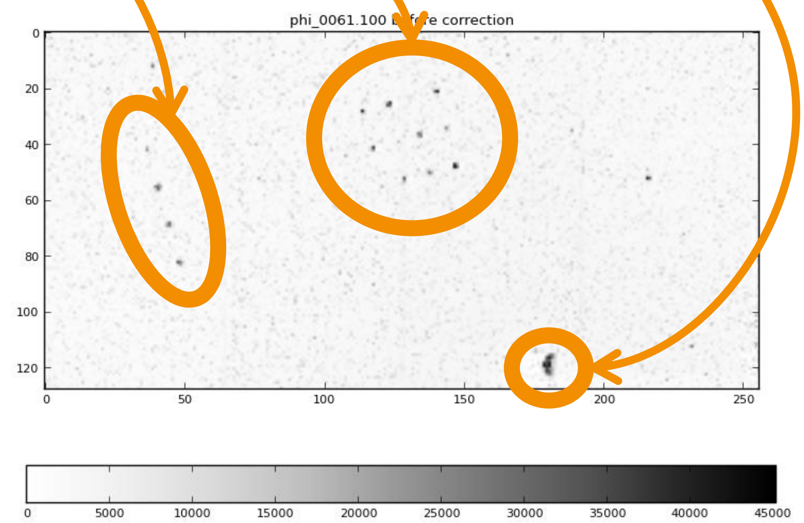
Protein crystallography at P11

The experiment:

- Structure of Trypsin will be resolved from AGIPD data and compared to previously obtained results from Pilatus 6M.
- Bursts of 352 images were recorded for each orientation
- Eγ=12.4 keV
- Clearly visible diffraction patterns
- “Half Moon” shaped image of the part of the direct beam missing the beam stop
- Right image is before, left one after correction

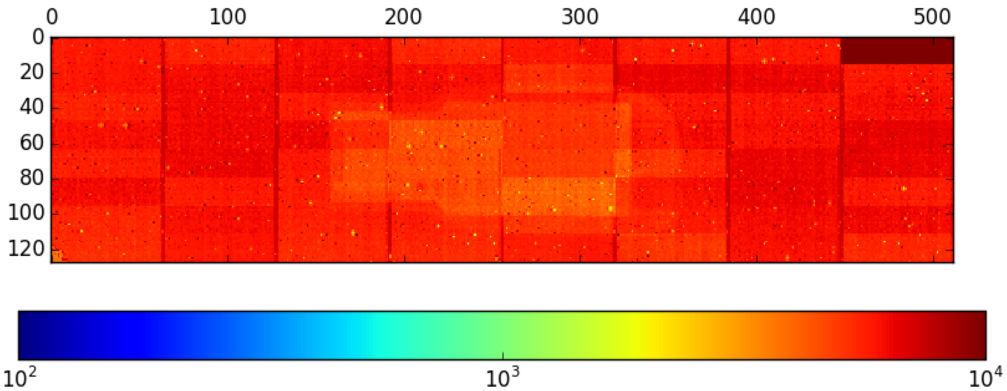
Trypsin





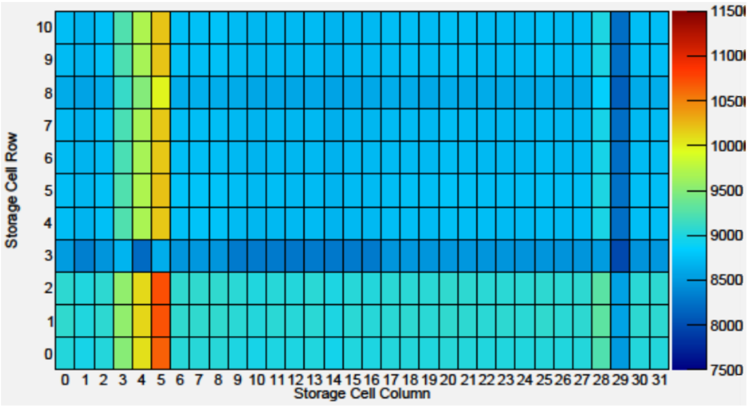
X-ray of a pendrive

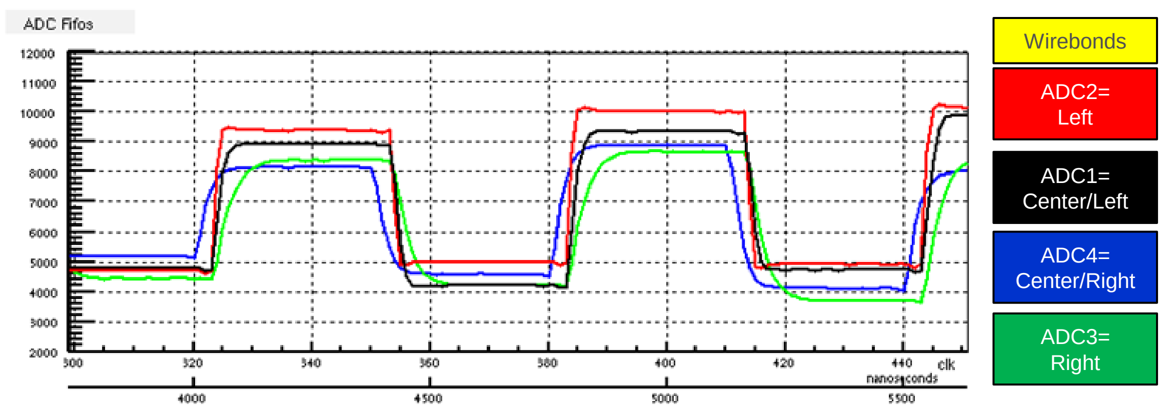
Mean of 30000 frames
50µs integration time per frame

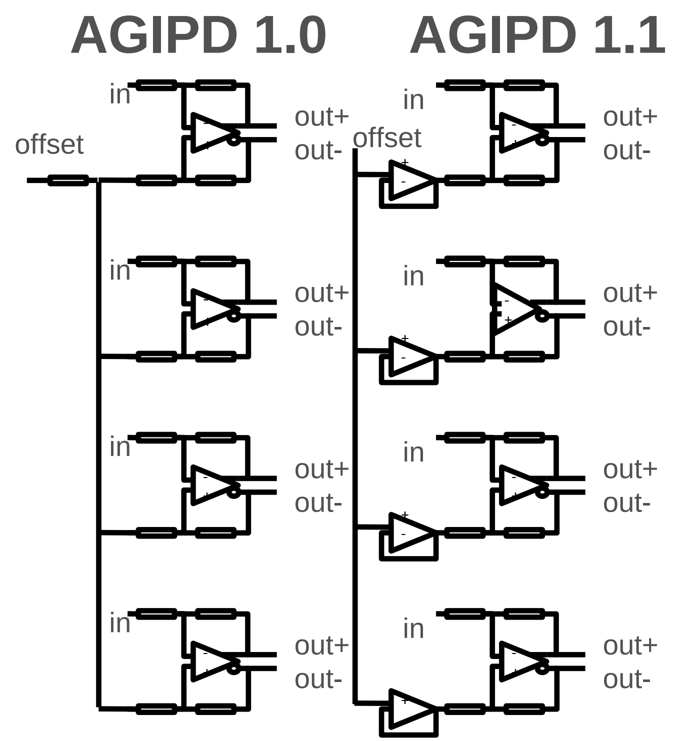


AGIPD 1.1

- An improved version of the AGIPD readout ASIC has been submitted for manufacturing in December 2015. It will have
  - Faster readout speed (33MHz) due to reduced parasitics
  - Less crosstalk inside the pixel and between readout lines
  - Easier calibration due to improved calibration circuits and less crosstalk
  - Minor other improvements, e.g. gain encoding in fixed gain mode
- It has been received back from fab Feb. 26th







Summary

- Single photon sensitivity
- Dynamic range of up to 10^4 Photons at 12keV
- Frame rates of up to 6.5MHz possible

- Improved AGIPD 1.1 received from fab last week (Feb. 26th)
- Delivery of AGIPD 1M to the European XFEL by mid of 2016.
- AGIPD 1M systems will be located at the XFEL beam lines SPB/SFX and MID
- SFX station at XFEL will use an AGIPD 4M system

	AGIPD
Pixel	64 x 64
Pixel size	200 x 200 μm^2
Storage cells	352
Chip size	13.1 x 14.8 mm^2
Dynamic range	1 to >$1 \cdot 10^4$ x 12.4 keV
Frame rate	>4.5 MHz (burst)
Noise (rms)	<265 e^- ENC
energy range(keV)	<6-15 keV
Non-linearity	<<1 %
Protection measure	Diode
Dead time	Triggered (EU-XFEL)
Vetoing scheme	yes
Technology	IBM 130nm

Conclusions.

Due to such long term commitments, don't expect things to change too fast!

(except for new projects and developments)

FZJ will tape out their 3rd TSMC 65nm Silicon!

- VULCAN is currently under development

KIT has developed the universal readout 'Photon V1' in UMC 180 nm

- KIT submitted **13** chips on **8** runs in AMS 0.35µm, AMS 180nm HV and UMC 180nm
- will also move to TSMC 65nm with some projects

DESY has taped out ASICS for several projects in IBM/GF 130 nm

- will move to 65nm based on a per-project evaluation

GSI will not move to TSMC 65nm in the near future

- Due to long-term projects in other processes

We agreed on an common toolset

- CERN-provided design kit
  - For sharing and NDA reasons
- Cadence 6.x (OA) based design flow
  - Little obstacles for a common design repository

We started an Offer and whish list

- For bartering designs and test environments

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