# Achievements and Perspectives of CMOS Pixel Sensors for HIGH-PRECISION Vertexing & Tracking Devices

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KIT / 10 March 2016

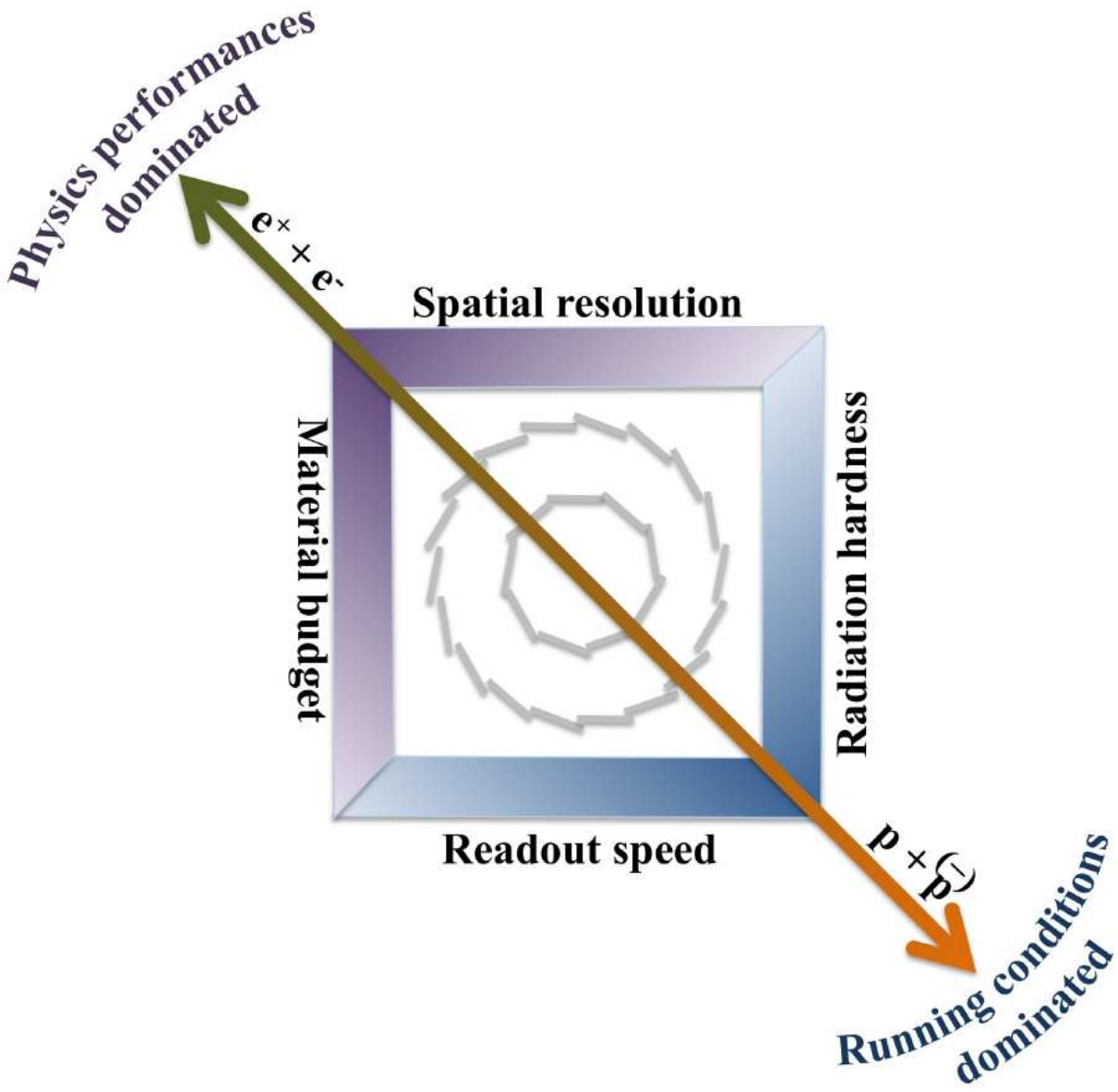
## *Contents*


- *Primordial motivations & main features of CMOS sensors*
- *1st architecture developped - state of the art*
  - MIMOSA-26 (EUDET chip applications) $\longmapsto$ MIMOSA-28 (STAR-PXL)
- *Extension towards more demanding experiments*
  - ALICE-ITS & -MFT
  - CBM-MVD
  - ILC
- *Perspectives for HEP + X-Ray imaging & forthcoming challenges*
  - read-out speed & rad. tolerance
  - architectures & emerging CMOS technologies
- *Conclusion*


**SOURCES : Talks at CPIX-14 + VERTEX-14/15 + FEE-14 + TWEPP-13/14/15 + LHCC/ALICE + VCI-2016**

**SLIDES : M.Deveaux, D. Doehring, L.Greiner, Ch.Hu-Guo, M.Keil, M.Mager, L.Musa, F.Morel, F.Reidt, W.Snoeys, G. Aglieri, ...**

# Motivation for High Precision CMOS Sensors



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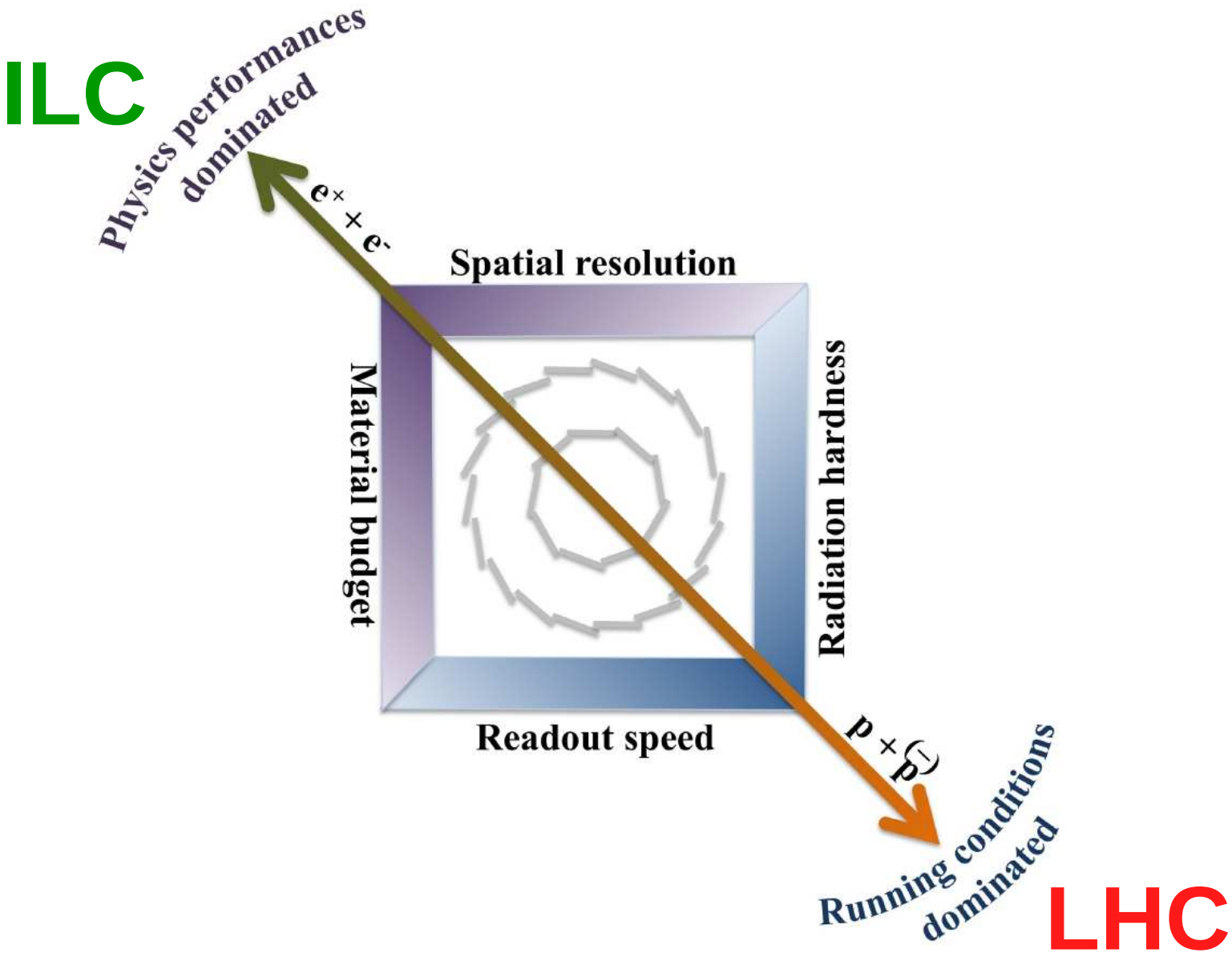

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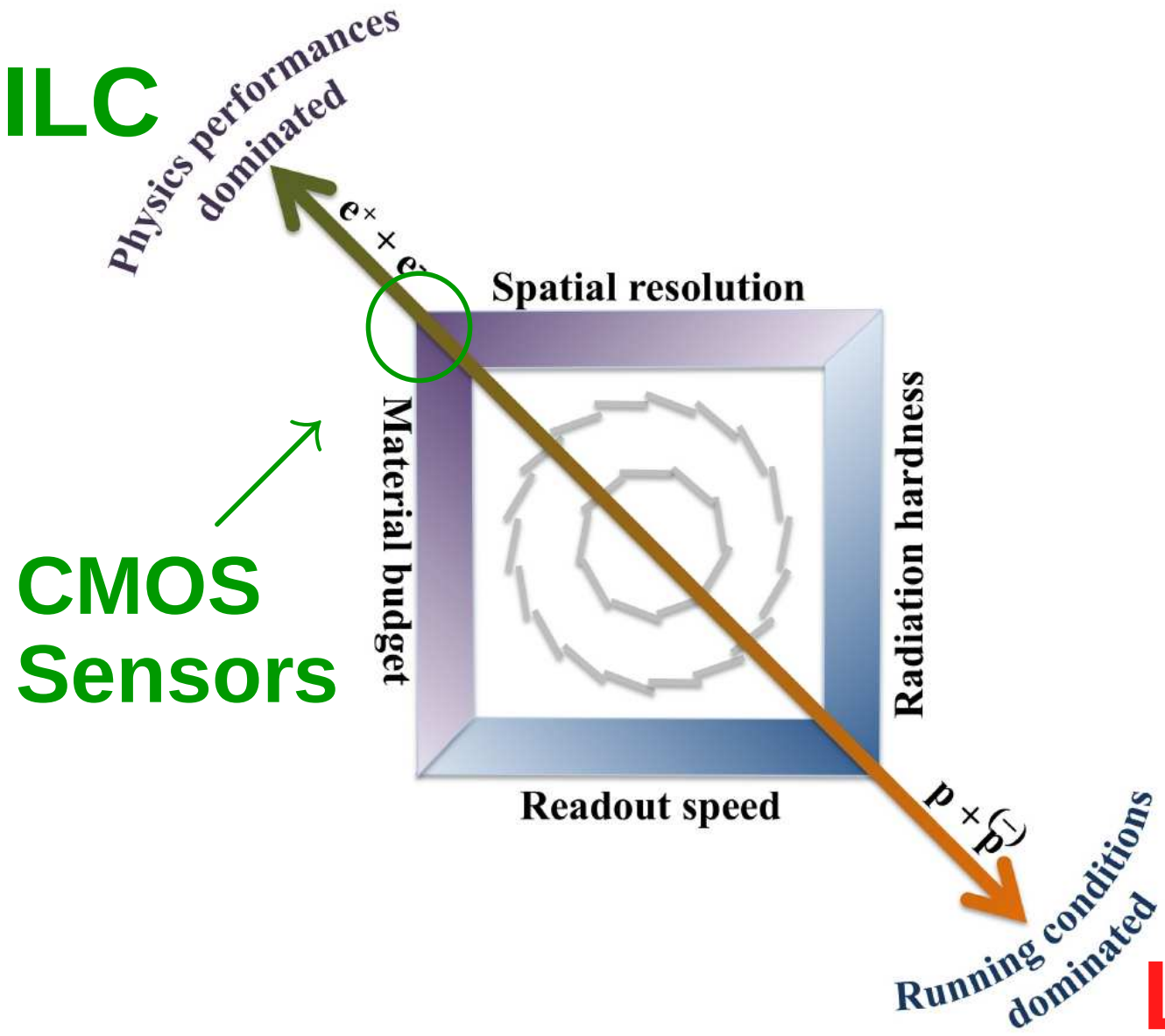

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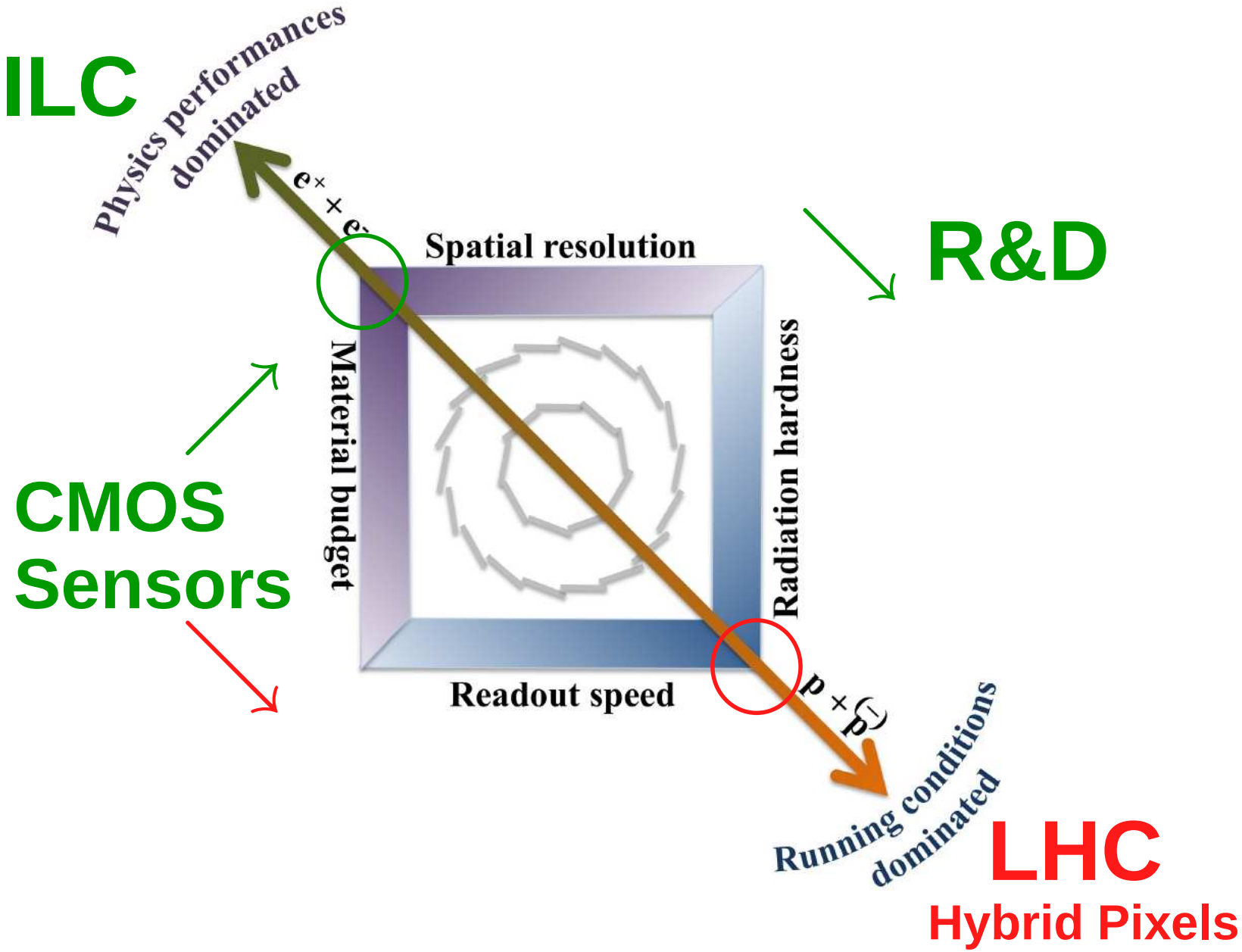
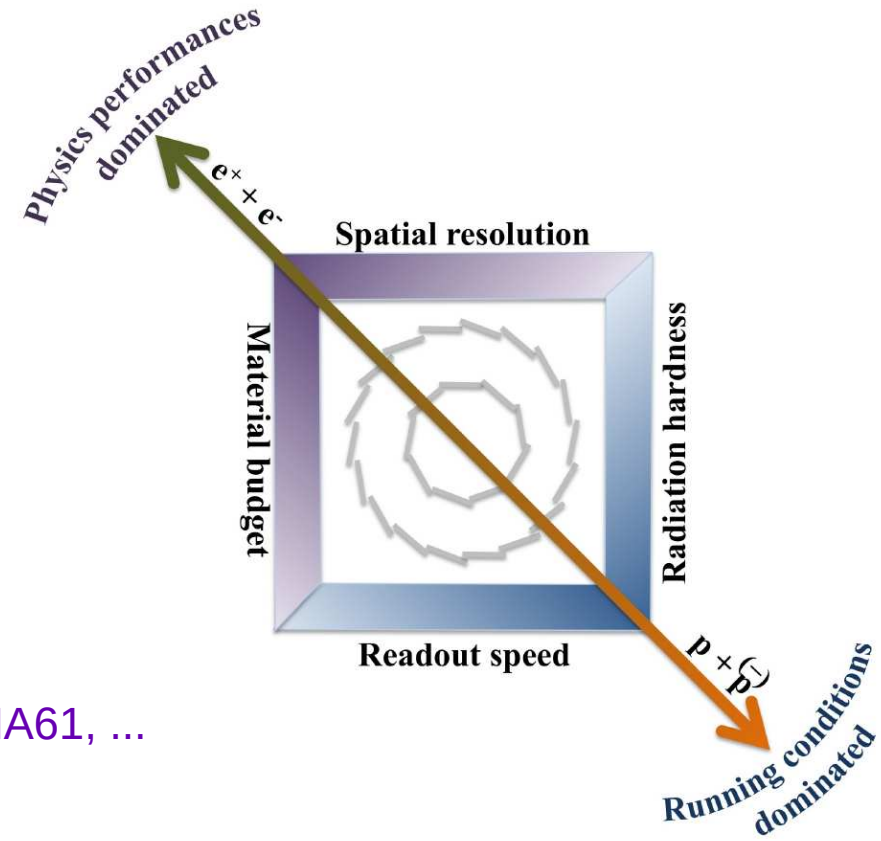


# Motivation for Developing CMOS Sensors

**Quadrature of the Vertex Detector**




- **CPS development triggered by need of**
  **very high granularity & low material budget**

- **Applications exhibit much milder running conditions than pp/LHC**

  ⇒ **Relaxed speed & radiation tolerance specifications**

- **Increasing panel of existing, foreseen or potential application domains :**
  - **Heavy Ion Collisions :** STAR-PXL, ALICE-ITS, CBM-MVD, NA61, ...
  - **$e^+e^-$ collisions :** ILC, BES-3, ...
  - **Non-collider experiments :** FIRST, NA63, Mu3e, PANDA, ...
  - **High precision beam telescopes** adapted to medium/low energy electron beams :

    ↪ few $\mu m$ resolution achievable on DUT with EUDET-BT (DESY), **BTF-BT (Frascati)**, ...

# Charged Particle Detection with THIN & HIGHLY GRANULAR Sensors

- DISPLACED VERTEX RECONSTRUCTION AND CHARACTERISATION :
  - reconstruction of collision point
  - reconstruction of D-meson and $\tau$-lepton vertices
  - reconstruction of b-quark decays in (top-quark) jets
  - determination of displaced vertex electrical charge
  - etc.

- ROLE IN THE TRACKING :
  - track seeding (depending on main tracker)
  - low $P_t$ track reconstruction
  - track momentum determination (in particular low $P_t$)
  - fake tracks mitigation ($E_{miss}$ determination)

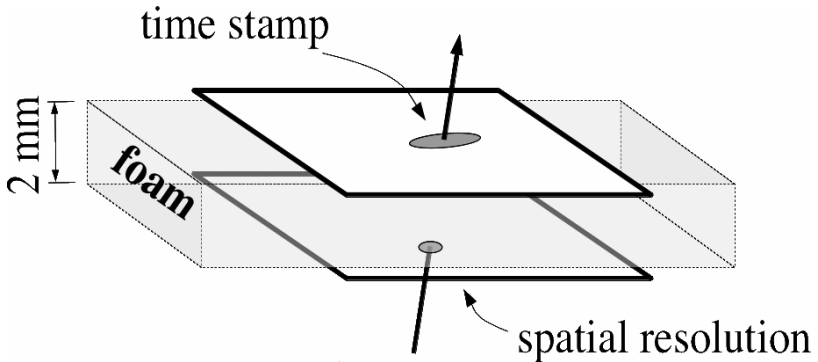
# Example of Application : ILC Vertex Detector

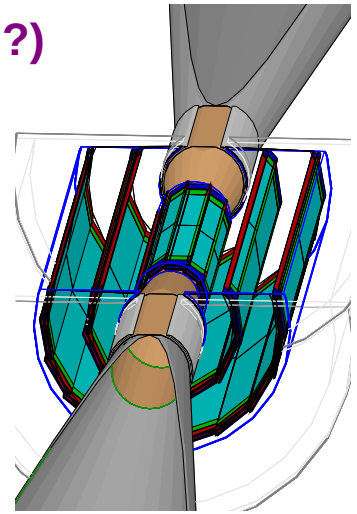
- **Goal :** $\sigma_{sp} \lesssim 3\ \mu m$ **in both directions with** $\lesssim$ **0.15 % X$_0$ / layer (2-sided layers ?)**
- **Comparison between ILC-VXD:**

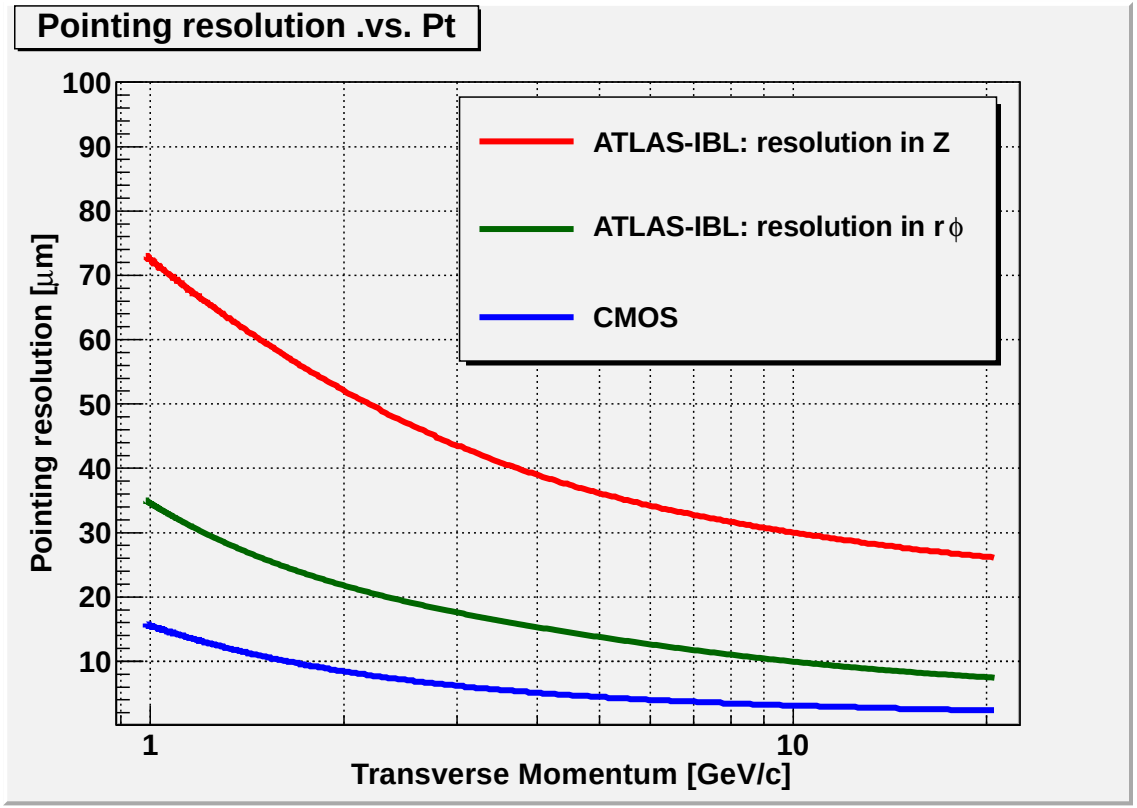
  $\sigma_{sp}$ **= 3x3** $\mu m^2$ **& 0.15 % X$_0$**

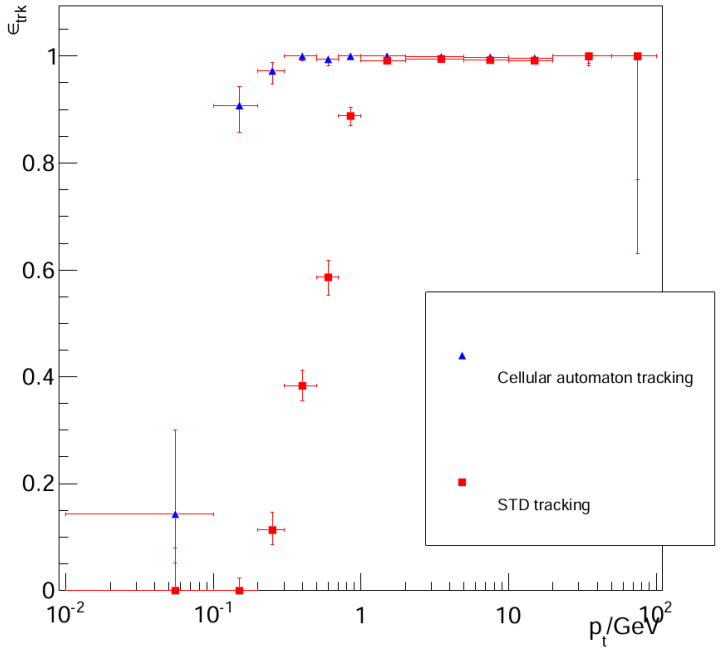
  **and ATLAS-IBL pixels:**

  $\sigma_{sp}$ **= 14x70** $\mu m^2$ **& 1.0 % X$_0$**





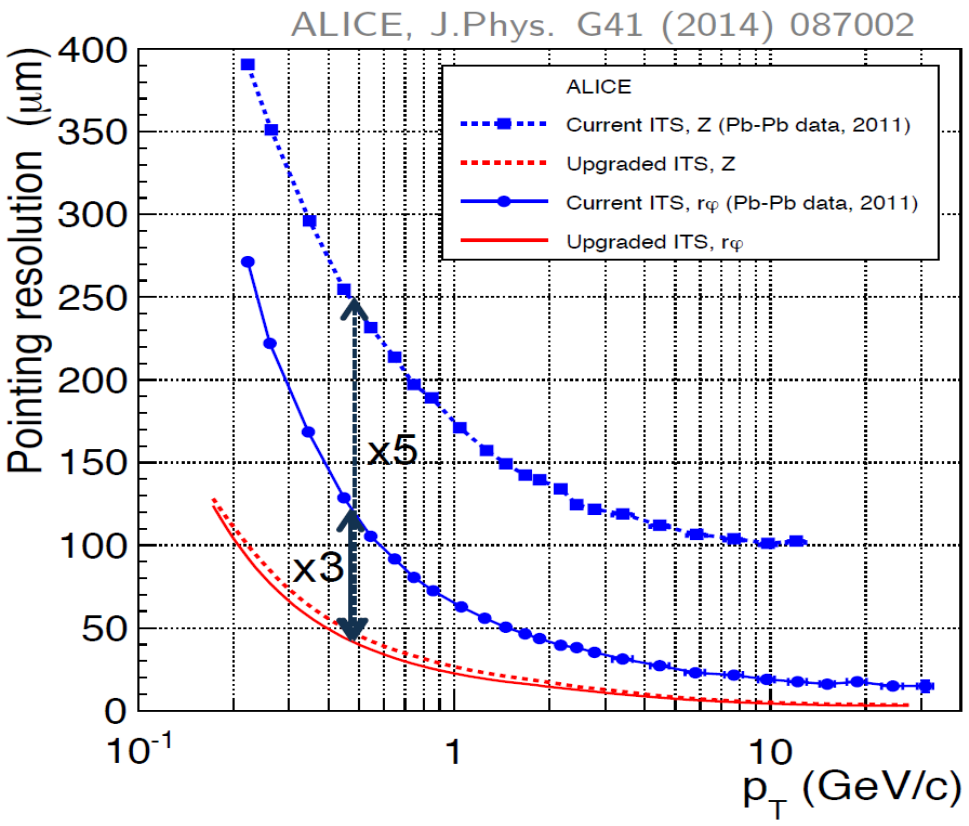



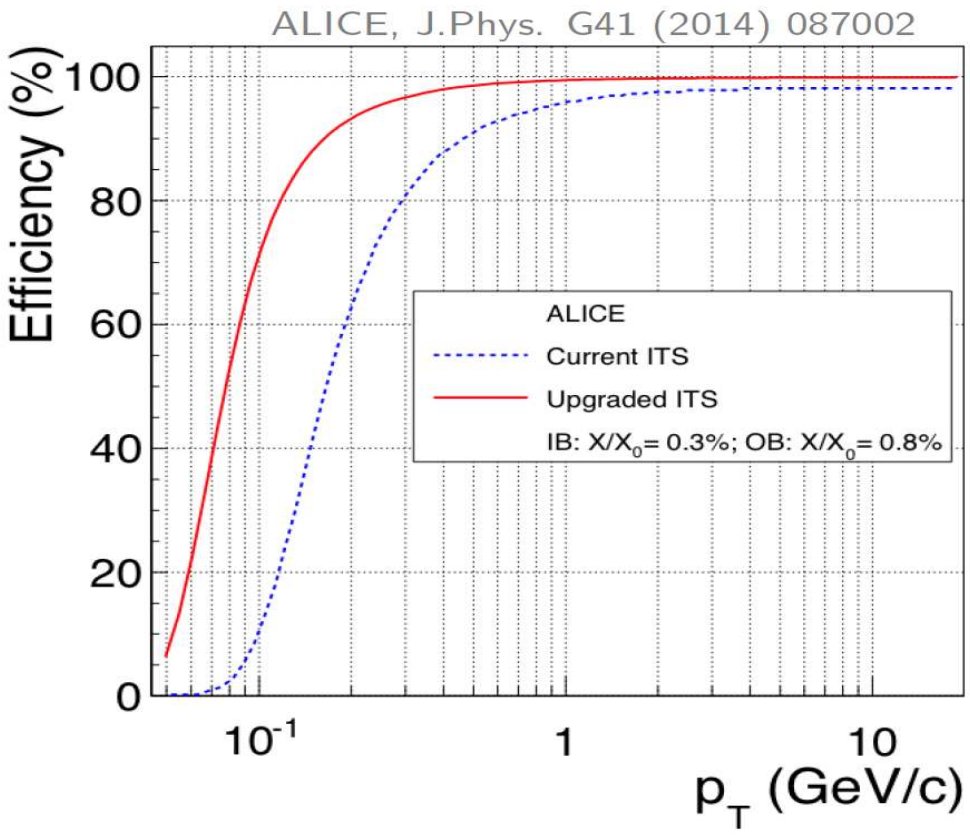
# Example of Application : Upgrade of ALICE-ITS

- **ALICE Inner Tracking System (ITS) foreseen to be replaced during LS2/LHC**

  ↪ higher luminosity (≡ collision rate), improved charm tagging

- **Expected improvement in pointing resolution and tracking efficiency**



# Long Term R&D

- *R&D activity of CPS initiated in 1999 for future subatomic physics experiments*
- *First contact for STAR PXL took place in Year 2000 during the workshop Vertex-2000*

VERTEX 2000
9th International Workshop on Vertex Detectors
Sleeping Bear Dunes
National Lakeshore, Michigan, U.S.A.
September 10-15, 2000

**First Announcement**

**Submission of Proceedings**

**Referees**

**Registration**

**Workshop Program**

**Presen**

**Pictur**

**Comm**

**Accom**

**Travel**

**Attend**

**Attendee Arrival Information**

A new Inner Vertex Detector for STAR

H. Wieman
Vertex 2000

MONOLITHIC ACTIVE PIXEL SENSORS FOR A LINEAR COLLIDER

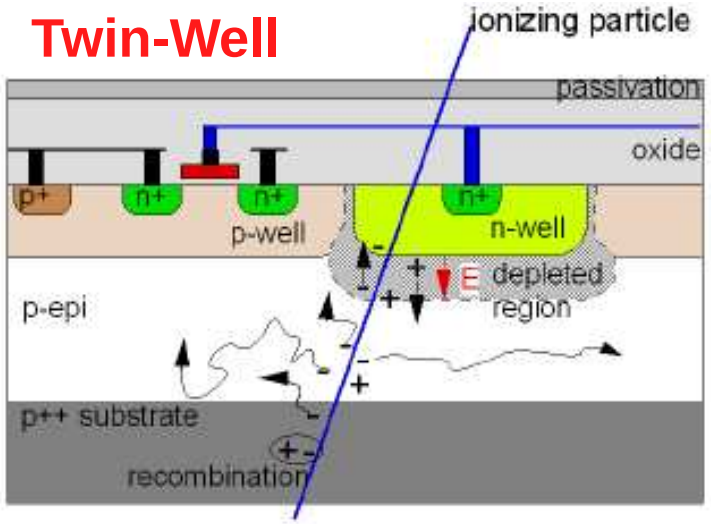
(Marc WINTER - IReS (Strasbourg))
on behalf of IReS+LEPSI coll.

- Physics Motivations
- Principle of Operation of M.A.P.S.
- Characteristics of 1st MAPS prototype
- Beam test Results (preliminary)
- Outlook

# CMOS Pixel Sensors: Main Features

- **Prominent features of CMOS pixel sensors :**
  - high granularity $\Rightarrow$ excellent (micronic) spatial resolution
  - signal generated in (very) thin (15-40 $\mu m$) epitaxial layer
    - $\hookrightarrow$ resistivity may be $\gg$ 1 k$\Omega \cdot cm$
  - signal processing $\mu$-circuits integrated on sensor substrate
    - $\Rightarrow$ impact on downstream electronics and syst. integration ($\Rightarrow$ cost)

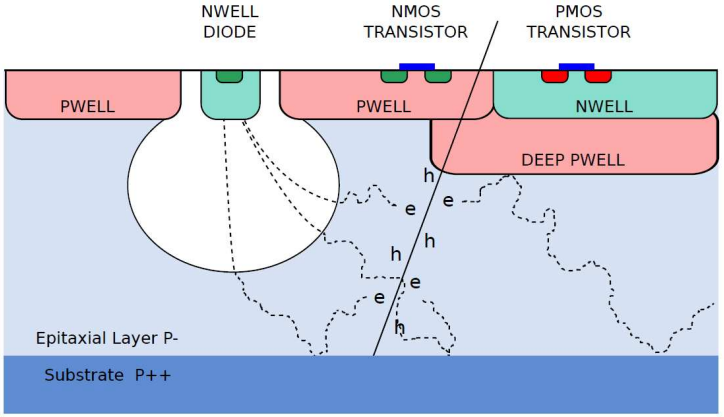
**Twin-Well**




- **CMOS pixel sensor technology has the highest potential :**

  $\Rightarrow$ R&D largely consists in trying to exploit potential at best with accessible industrial processes

  $\hookrightarrow$ manufacturing param. not optimised for particle detection: wafer/EPI characteristics, feature size, N(ML), ...

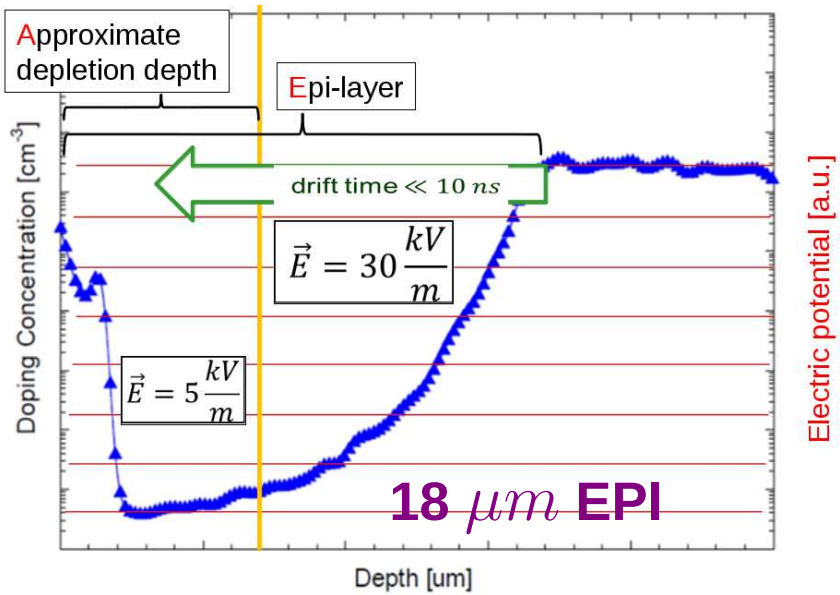


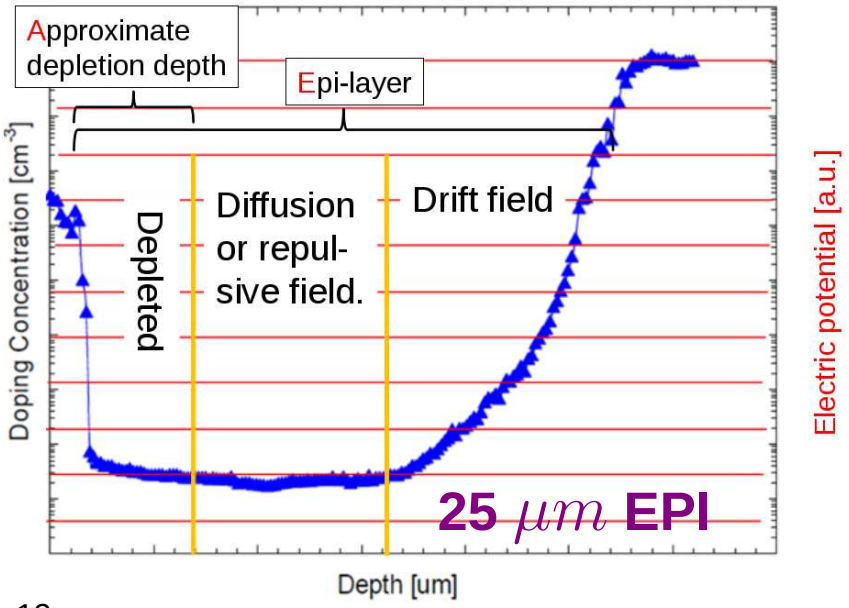

**Quadruple-Well**

- **Read-out architectures :**
  - 1st generation : rolling shutter (synchronous) with analog pixel output (end-of-column discri.)
  - 2nd generation : rolling shutter (synchronous) with in-pixel discrimination
  - 3rd generation : data driven (asynchronous) with in-pixel discrimination
  - ...

# Role of the Epitaxial Layer

- **Main influences :**
  - $Q_{signal} \sim$ EPI thickness and doping profile
  - $\epsilon_{det}$ depends on depletion depth vs EPI thickness
  - NI radiation tolerance depends on depletion depth vs EPI thickness
  - Cluster multiplicity and $\sigma_{sp}$ depend on pixel pitch / EPI thickness
- **Case dependent optimisation mandatory :**
  - Deep depletion ⇛ higher SNR (seed pixel) ⇛ improved $\epsilon_{det}$ but degraded spatial resolution ....
  - Spatial resolution depends on Nb of bits encoding charge vs pixel pitch ...
  - Density of in-pixel circuitry depends on CMOS process options : feature size, Nb(ML), twin/quadruple-well, ...



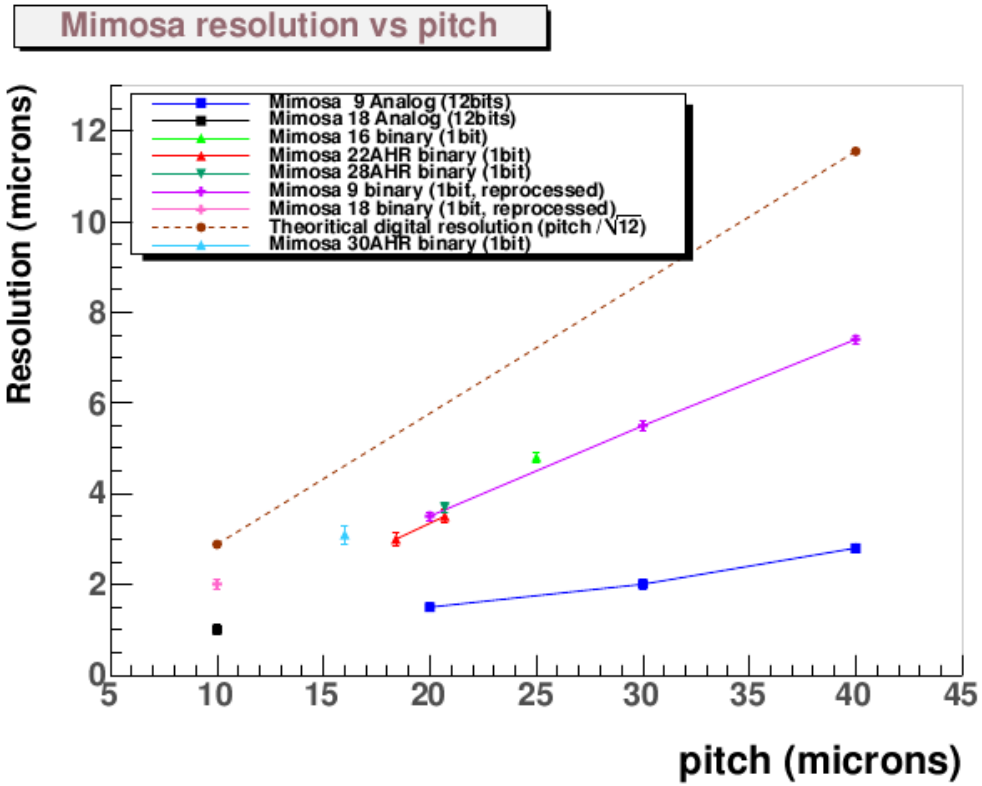



# Measured Spatial Resolution

- **Several parametres govern the spatial resolution :**
  - pixel pitch
  - epitaxial layer thickness and resistivity
  - sensing node geometry & electrical properties

  ↪ cluster charge sharing between pixels
  - signal encoding resolution

  ⇛ $\sigma_{sp}$ fct of pitch ⊕ SNR ⊕ charge sharing ⊕ ADCu, ...



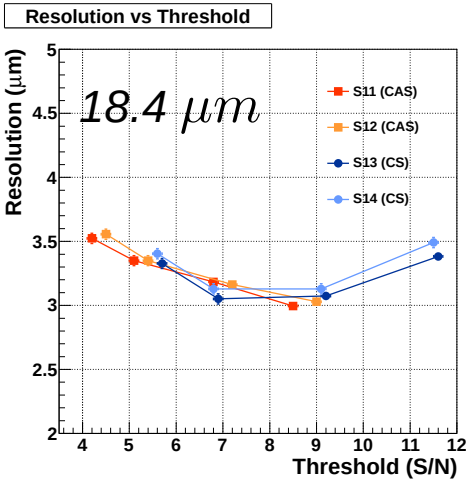

- **Impact of pixel pitch (analog output) :**

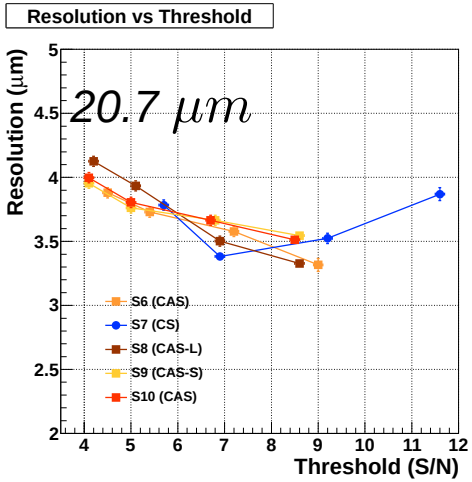
$\sigma_{sp} \sim 1\ \mu m$ (10 $\mu m$ pitch) $\rightarrowtail$ $\lesssim 3\ \mu m$ (40 $\mu m$ pitch)

- **Impact of charge encoding resolution :**

▷ ex. of 20 $\mu m$ pitch ⇛ $\sigma_{sp}^{digi}$ = pitch/$\sqrt{12}$ ∼ 5.7 $\mu m$

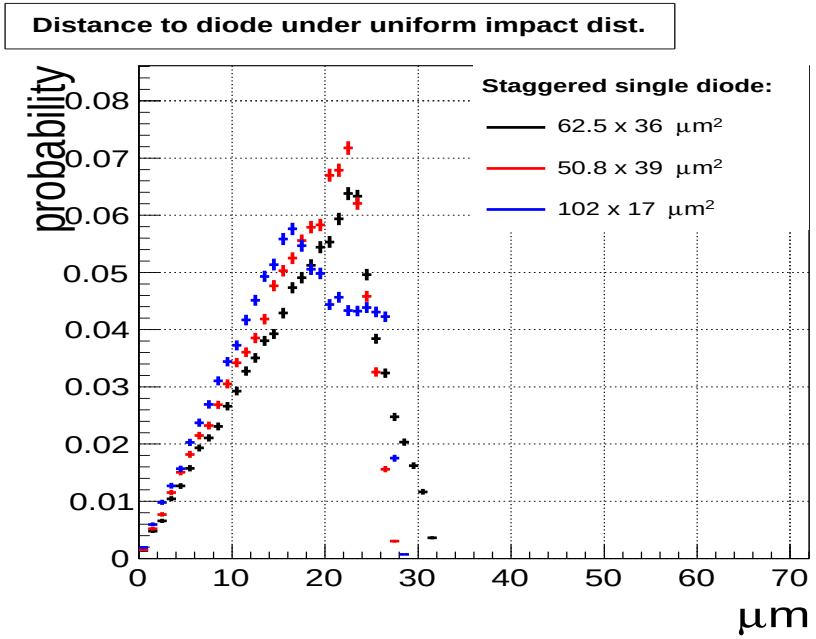
| Nb of bits | 12 | 3-4 | 1 |
|---|---|---|---|
| Data | *measured* | *reprocessed* | *measured* |
| $\sigma_{sp}$ | $\lesssim 1.5\mu m$ | $\lesssim 2\mu m$ | $\lesssim 3.5\mu m$ |



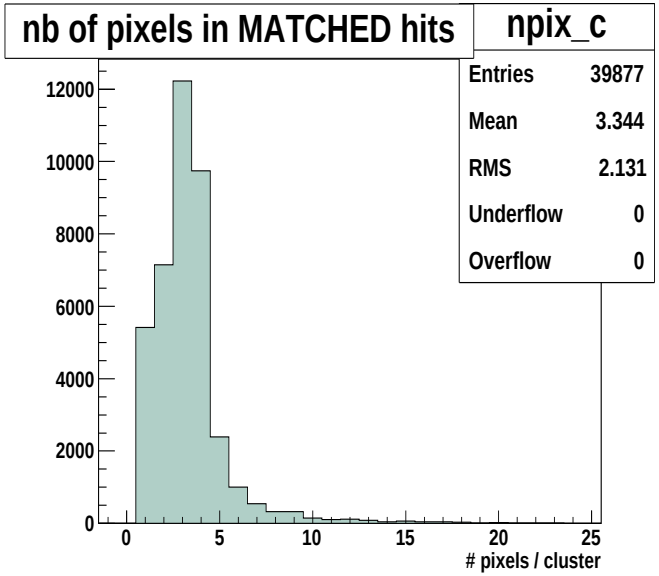



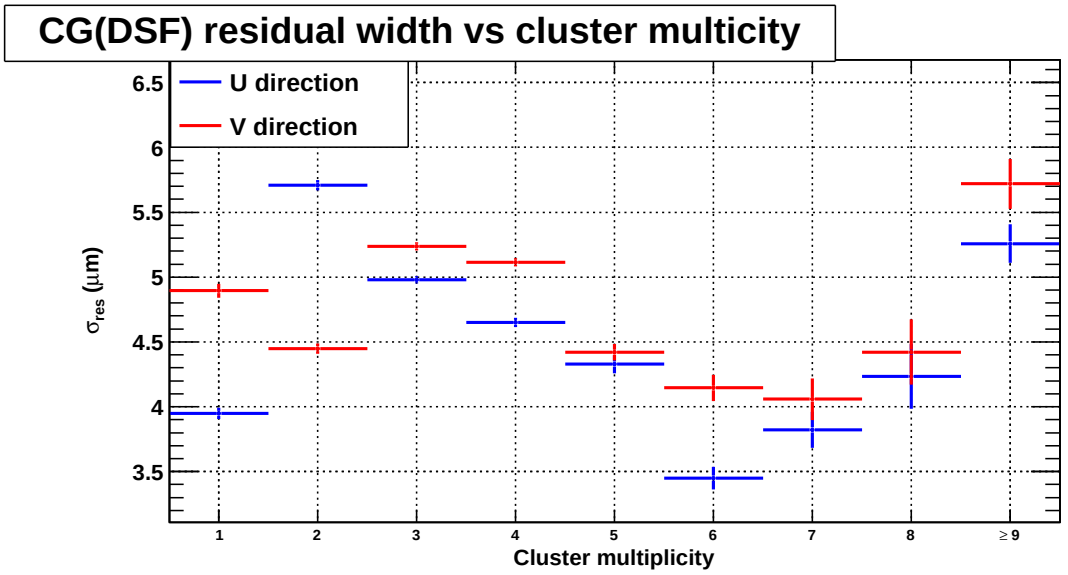
# Spatial resolution vs Cluster Dimensions

- **Correlation between $\sigma_{sp}$ & cluster hit multiplicity following from :**
  - pixel dimensions vs epitaxy characteristics (thickness, resistivity, doping profile)
  - sensing node pattern (density, staggering, geometry)
  - depletion voltage
  - ...



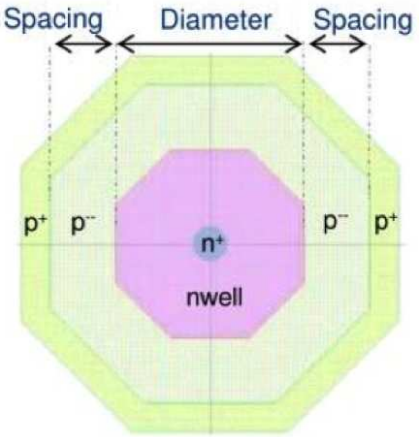

- **9 $\mu m^2$ diode :** threshold at 5 mV



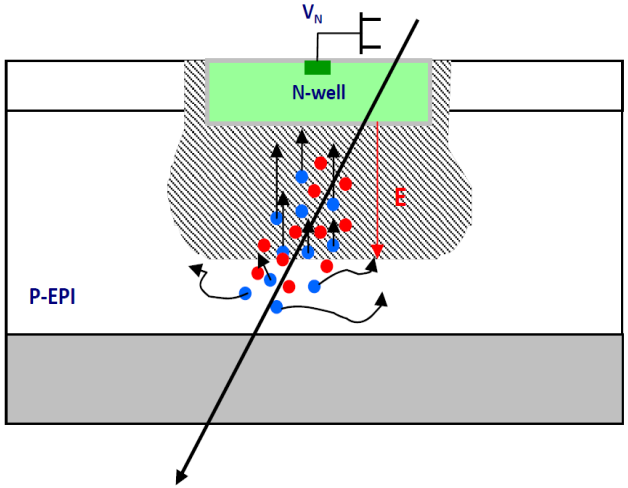



# Sensing Node & VFEE Optimisation

- **General remarks on sensing diode :**
  - should be small because : $V_{signal} = Q_{coll}/C$ ; Noise $\sim$ C ; $G_{PA} \sim 1/C$
  - BUT should not be too small since $Q_{coll} \sim$ CCE (important against NI irradiation)




- **General remarks on pre-amplifier** connected to sensing diode :
  - should offer high enough gain to mitigate downstream noise contributions
  - should feature input transistor with minimal noise (incl. RTS)
  - should be very close to sensing diode (minimise line C)

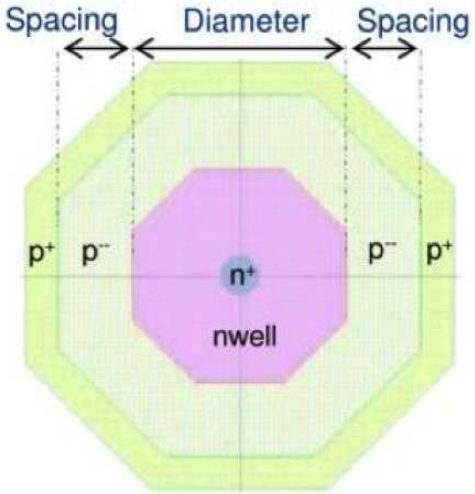


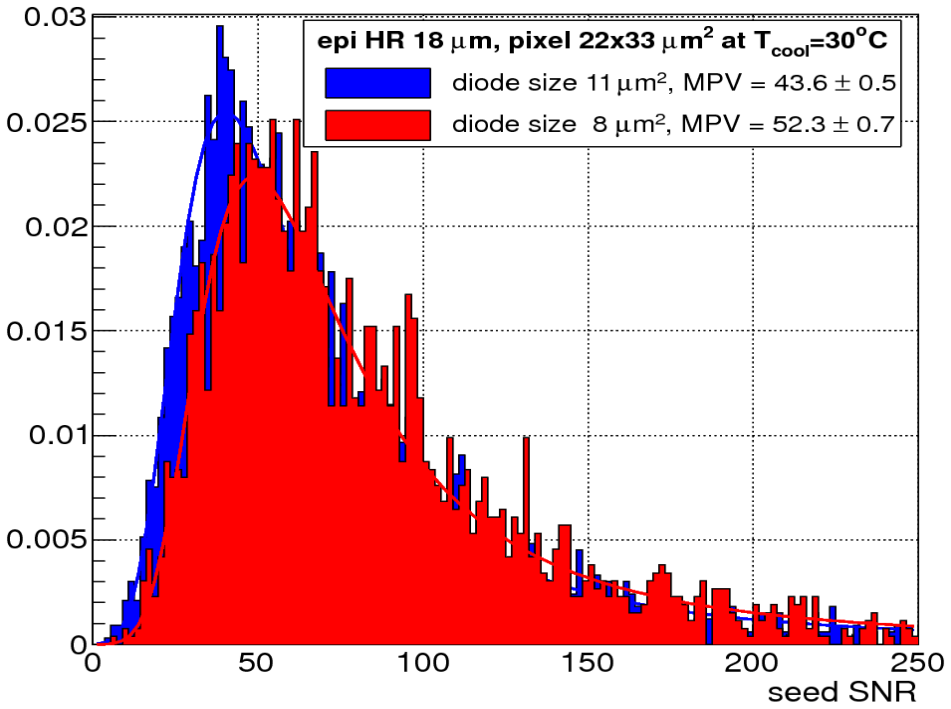

- **General remarks on depletion voltage :**
  - apply highest possible voltage on sensing diode
    preserving charge sharing $\mapsto \sigma_{sp}$
  - alternative : backside/reverse biasing

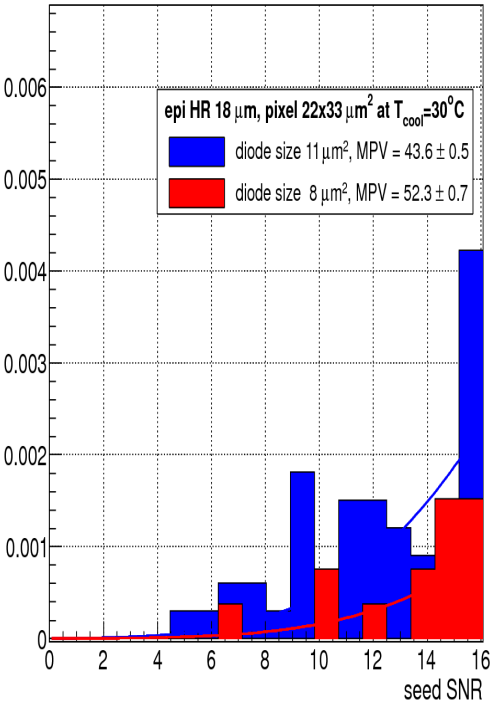
$\Rightarrow$ **Multiparametric trade-off to be found,**
**based on exploratory prototypes rather than on simulations**

# Charge Sensing Element ⟼ Optimal SNR

- **Influence of sensing diode area**



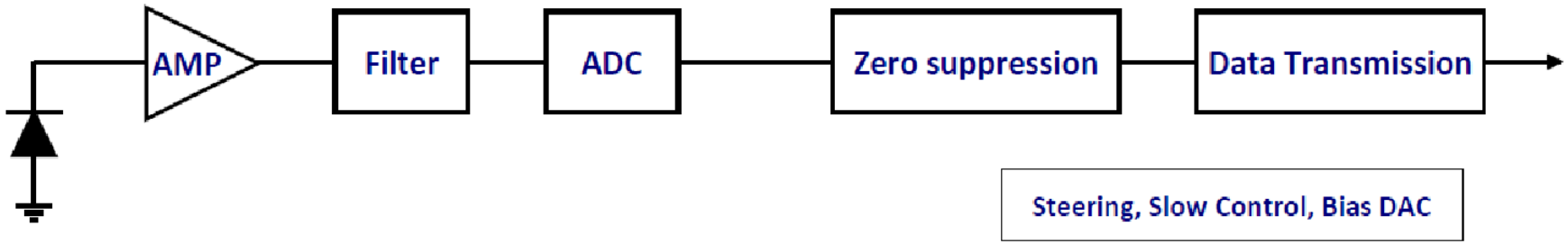




- **Benefit from reducing the sensing diode area**
  - sensing diode cross-section varied from 10.9 $\mu m^2$ to 8 $\mu m^2$ underneath 10.9 $\mu m^2$ large footprint

    ↪ suppresses low SNR tail ⟼ enhances detection efficiency (and mitigates effect of fake rate)

# Main Components of the Signal Processing Chain




- **Typical components of read-out chain :**
  - **AMP :** In-pixel low noise pre-amplifier
  - **Filter :** In-pixel filter
  - **ADC :** Analog-to-Digital Conversion : 1-bit ≡ discriminator
    ↪ may be implemented at column or pixel level
  - **Zero suppression :** Only hit pixel information is retained and transfered
    ↪ implemented at sensor periphery (usual) or inside pixel array
  - **Data transmission :** O(Gbits/s) link implemented on sensor periphery

- **Read-Out alternatives :**
  - **Synchronous :** rolling shutter architecture
  - **Asynchronous :** data driven architecture

- **Rolling shutter : best approach for twin-well processes**

↪ trade-off between performance, design complexity, pixel dimensions, power, ...

↪ MIMOSA-26 (EUDET), MIMOSA-28 (STAR), ...

# Speed vs Pixel Dimensions

- **Pixel dimensions govern the spatial resolution at the expense of read-out speed**
  - $\Rightarrow$ **Trade-off to be found specific to each application**

| **Pixel pitch** | $< 10\ \mu m$ | $\gtrsim 15\ \mu m$ | $> 20\ \mu m$ | $\gtrsim 25\ \mu m$ | $\lesssim 50\ \mu m$ |
|---|---|---|---|---|---|
| **Nb(T)** | 2–3 | 15 | $\gtrsim$ 50 | $\gtrsim$ 200 | HV: few $10^2$ |
| $\sigma_{sp}$ [$\mu m$] | $\lesssim$ 1x1 | $<$ 3x3 | $<$ 5x5 | $\lesssim$ 5x5 | $\gtrsim$ 10x10 |
| $\Delta t$ [$\mu s$] | $10^3$ | $\lesssim$ 30/200 | $\gtrsim$ 10-15 | $<$ 10 | $10^{-2}$ |
| **Pre-Amp+Filter** | Out | In-Pix | In-Pix | In-Pix | In-Pix |
| **Discrimination** | Out | Out | In-Pix | In-Pix | In-Pix |
| **Sparsification** | Out | Out | Out | In-Pix | In-Pix |
| **Ex.(chip)** | Mimosa-18 | ULTIMATE/MISTRAL | ASTRAL | ALPIDE | HV-CMOS |
| **Depleted** | No | No | No | Yes | YES |
| **CMOS Process** | AMS-0.35 | AMS-0.35/Tower-0.18 | Tower-0.18 | Tower-0.18 | AMS-0.35/0.18 |
| **Ex.(appli.)** | Beam Tele. | STAR-PXL/ALICE-ITS | ALICE-ITS | ALICE-ITS | LHC ? |

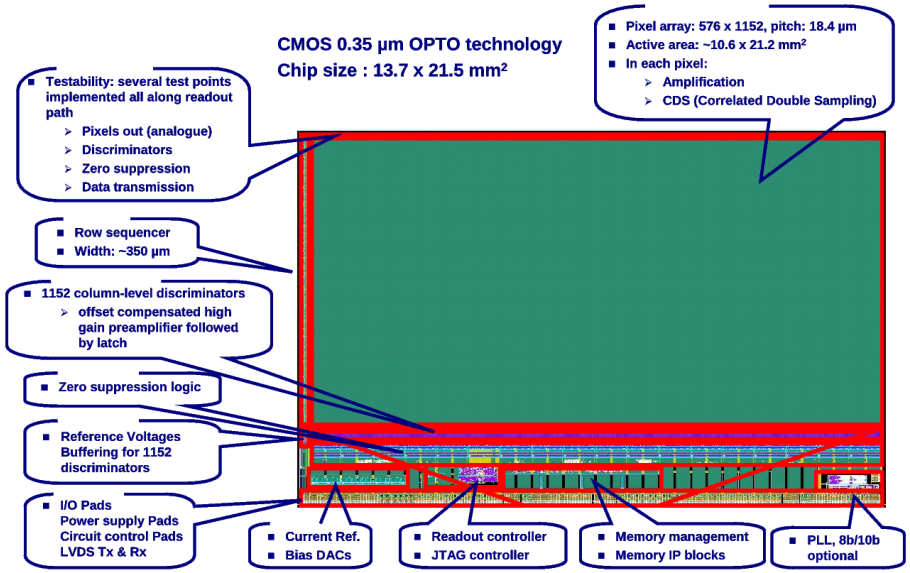
# STATE OF THE ART

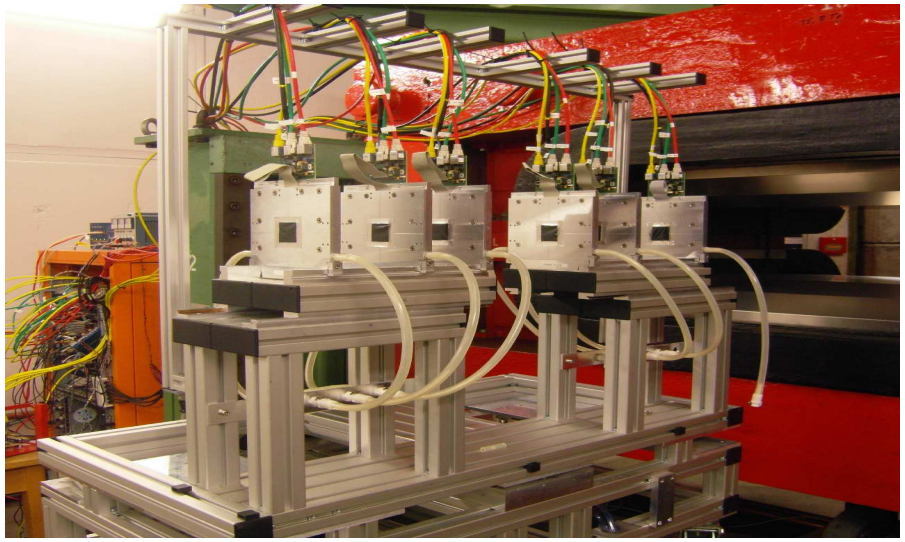
# RUNNING INSTRUMENTS

# EQUIPPED WITH CPS

# CMOS Pixel Sensors: Established Architecture

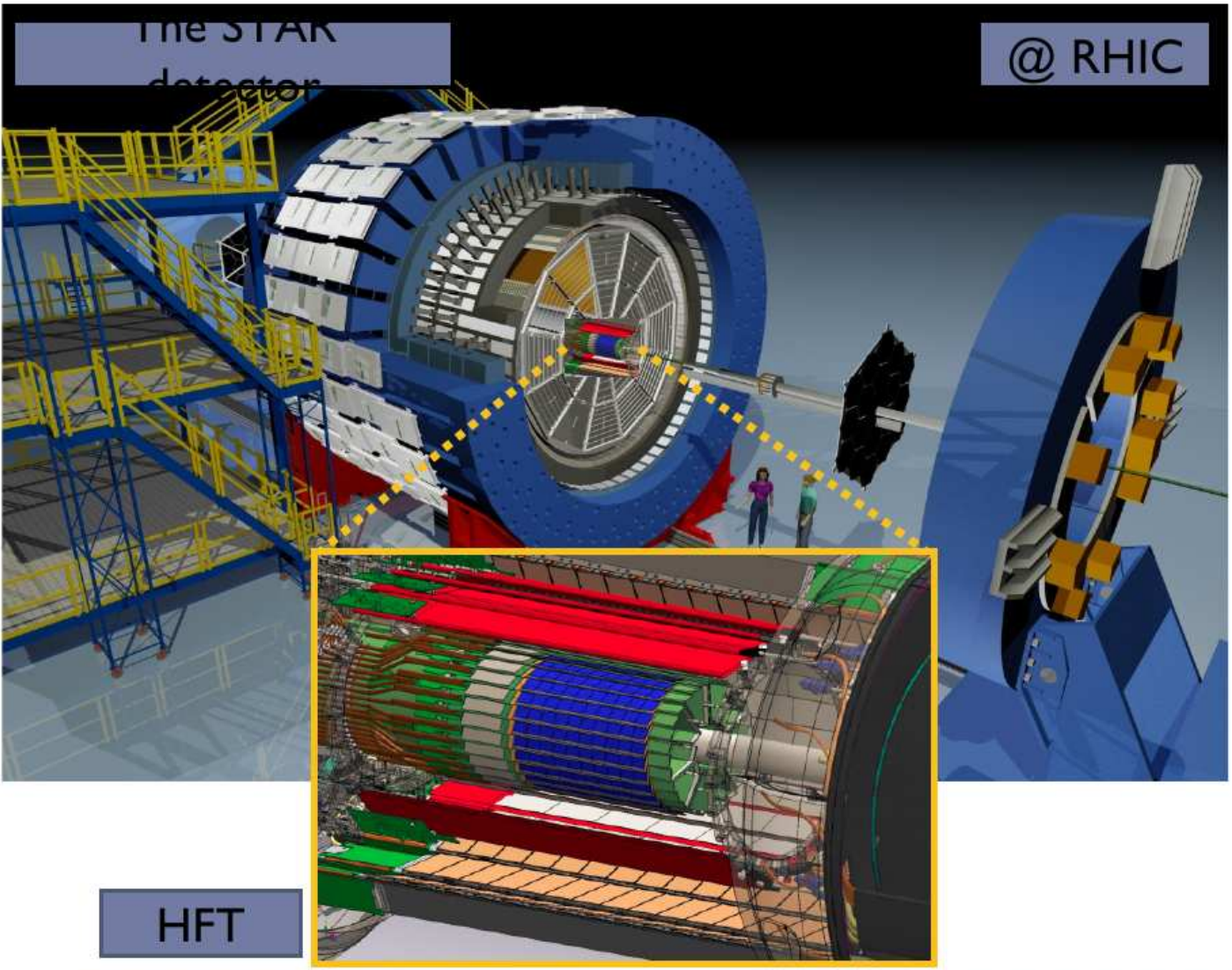
- **Main characteristics of MIMOSA-26 sensor equipping EUDET BT :**
  - 0.35 $\mu m$ process with high-resistivity epitaxial layer
    (coll. with IRFU/Saclay)
  - column // architecture with in-pixel amplification (cDS)
    and end-of-column discrimination, followed by $\emptyset$
  - binary charge encoding
  - active area: 1152 columns of 576 pixels (21.2$\times$10.6 mm$^2$)
  - pitch: 18.4 $\mu m \rightarrowtail$ $\sim$ 0.7 million pixels
    - $\triangleright$ charge sharing $\Rrightarrow$ $\sigma_{sp} \sim$ 3.-3.5 $\mu m$
  - t$_{r.o.} \lesssim$ 100 $\mu s$ ($\sim$10$^4$ frames/s)
    - $\hookrightarrow$ suited to $>$10$^6$ part./cm$^2$/s
  - JTAG programmable
  - rolling shutter architecture
    - $\Rrightarrow$ full sensitive area dissipation $\cong$ 1 row
      - $\triangleright$ $\sim$ 250 mW/cm$^2$ power consumption (fct of N$_{col}$)
  - thinned to 50 $\mu m$ (yield $\sim$ 90 %)

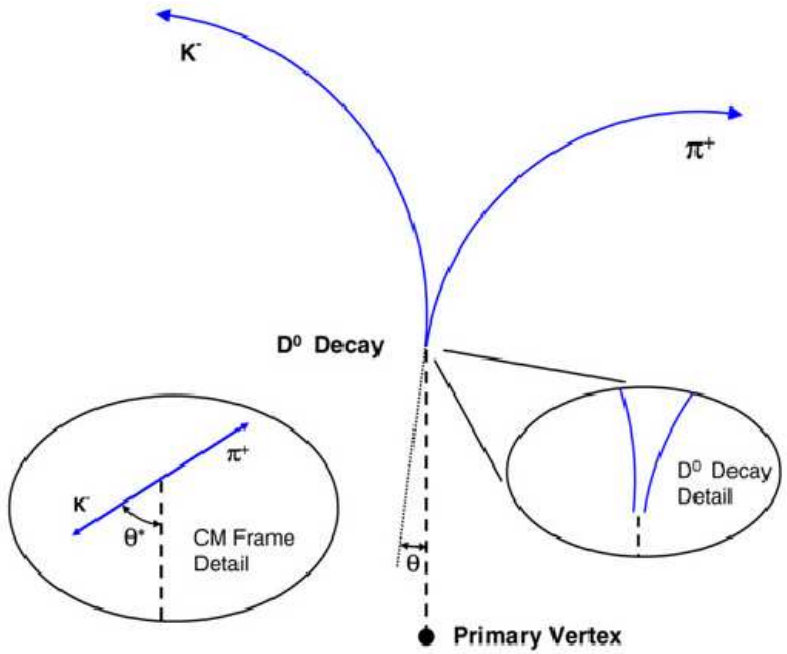


- **Various applications :** VD demonstrators, NA63, NA61, FIRST, oncotherapy, dosimetry, ...

# State-of-the-Art : STAR-PXL




Method: Resolve displaced vertices (~120 μm)

200 GeV Au+Au collisions @ RHIC

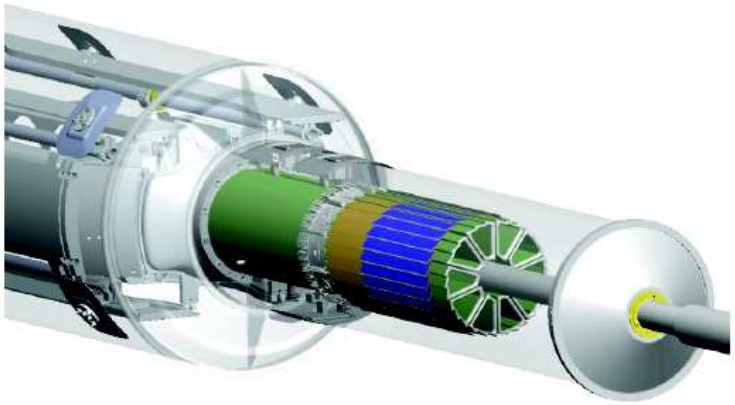
- $dN_{ch}/d\eta \sim 700$ in central events

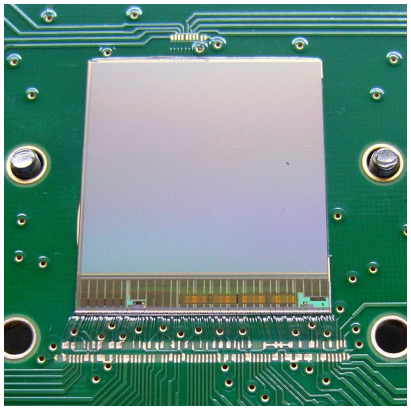


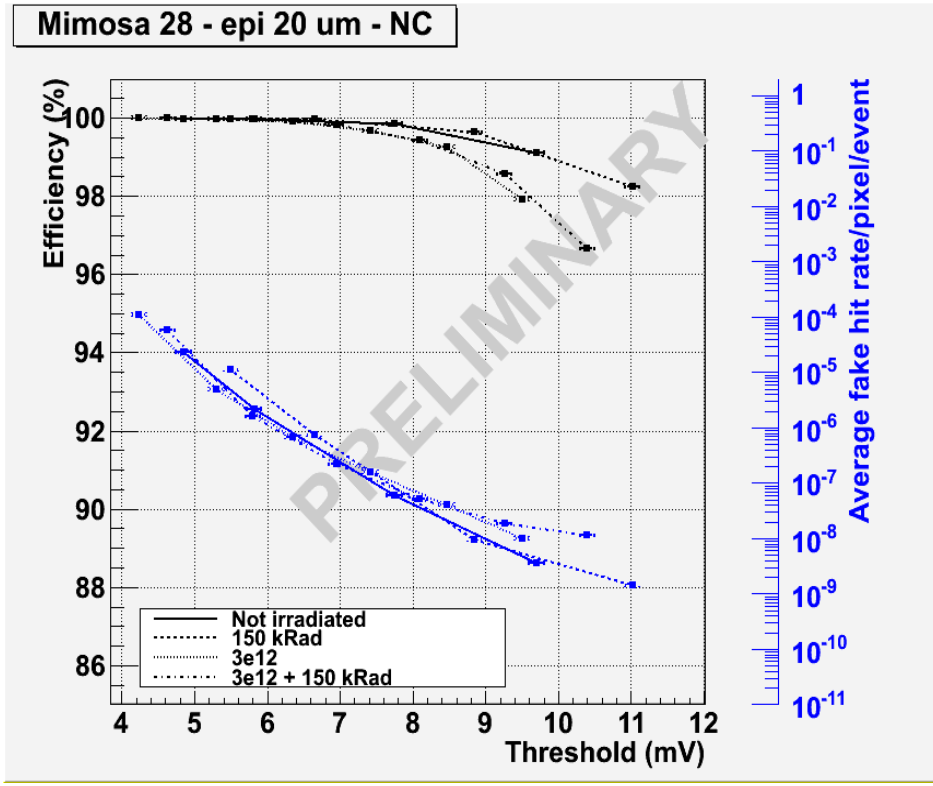
STAR

# State-of-the-Art: MIMOSA-28 for the STAR-PXL

- **Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):**
  - 0.35 $\mu m$ process with high-resistivity epitaxial layer
  - column // architecture with in-pixel cDS & amplification
  - end-of-column discrimination & binary charge encoding
  - on-chip zero-suppression
  - **active area: 960 colums of 928 pixels (19.9$\times$19.2 mm$^2$)**
  - **pitch: 20.7 $\mu m \longmapsto \sim$ 0.9 million pixels**
    $\hookrightarrow$ **charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 $\mu m$**
  - JTAG programmable
  - **t$_{r.o.}$ $\lesssim$ 200 $\mu s$ ($\sim$ 5$\times$10$^3$ frames/s) $\Rrightarrow$ suited to $>$10$^6$ part./cm$^2$/s**
  - 2 outputs at 160 MHz
  - **$\lesssim$ 150 mW/cm$^2$ power consumption**





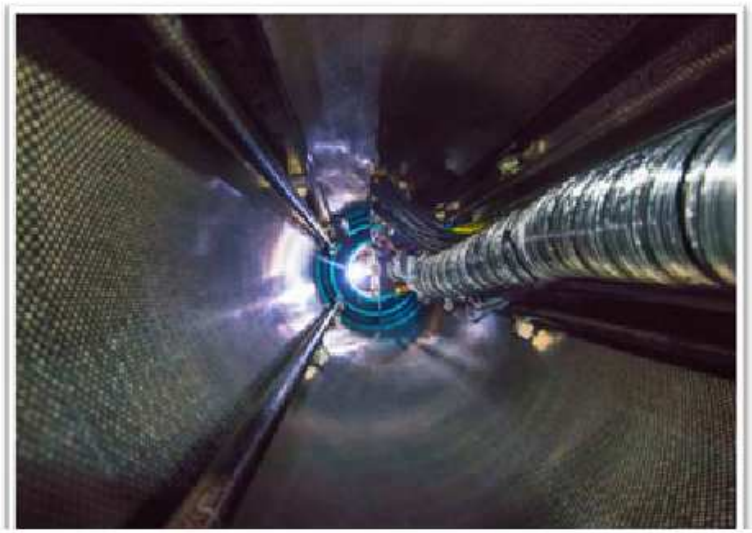



$\triangleright\triangleright\triangleright$ **Sensors FULLY evaluated/validated :** (50 $\mu m$ thin)

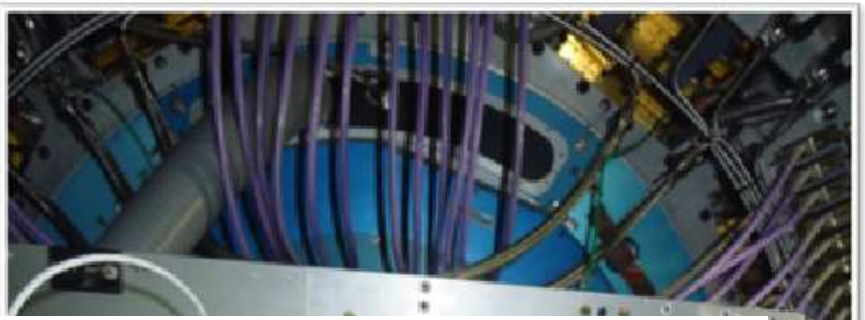
- N $\lesssim$ 15 e$^-$ ENC at 30-35$^\circ$C
- $\epsilon_{det}$, fake & $\sigma_{sp}$ as expected
- **Rad. tol. validated (3$\cdot$10$^{12}$n$_{eq}$/cm$^2$ & 150 kRad at 30$^\circ$C)**
- All specifications were met $\Rrightarrow$ 2 detectors of 40 ladders constructed

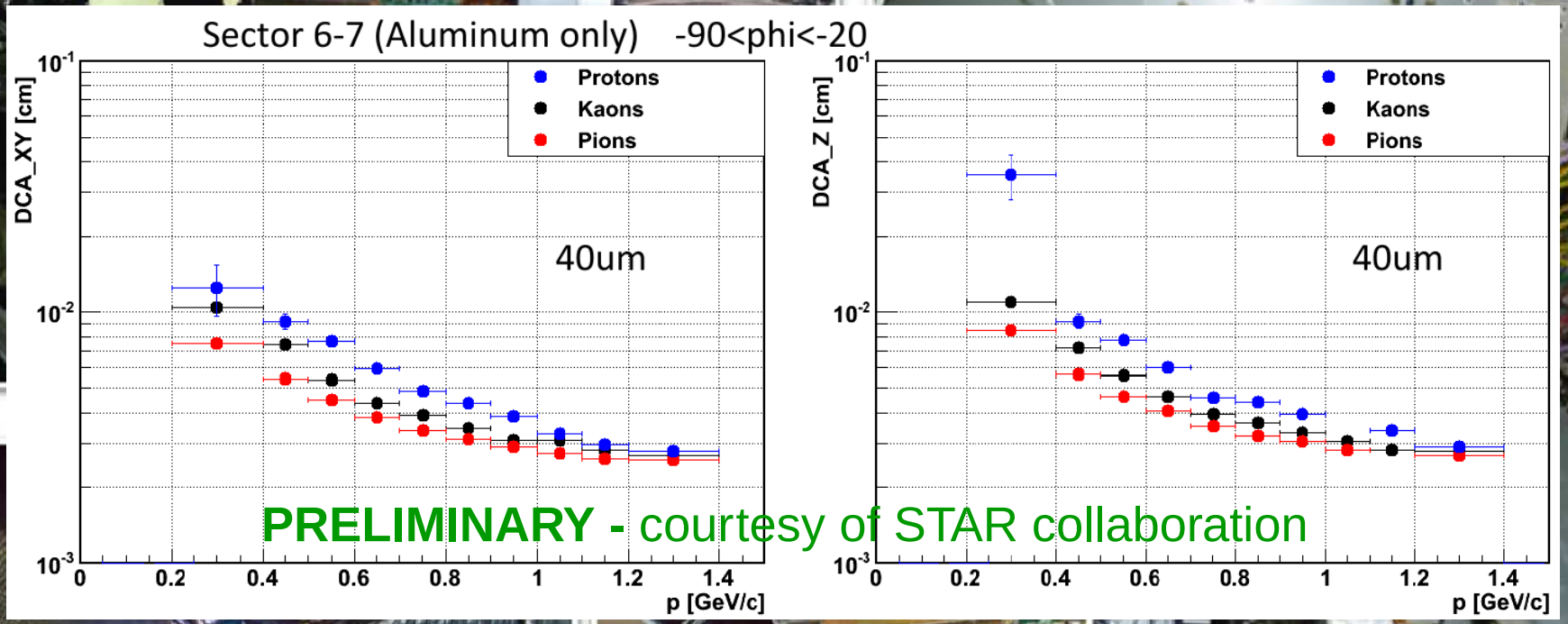
$\triangleright\triangleright\triangleright$ **Physics data taking since March 2014 $\mapsto$ measured $\sigma_{ip}(p_T)$ match requirements**

# State-of-the-Art : STAR-PXL

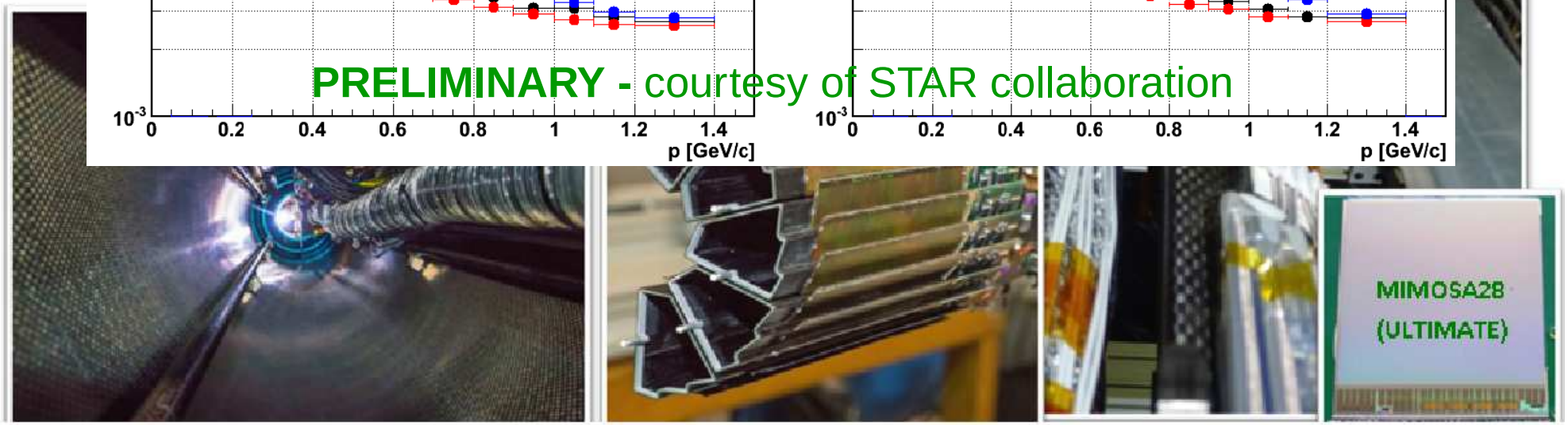


# State-of-the-Art : STAR-PXL



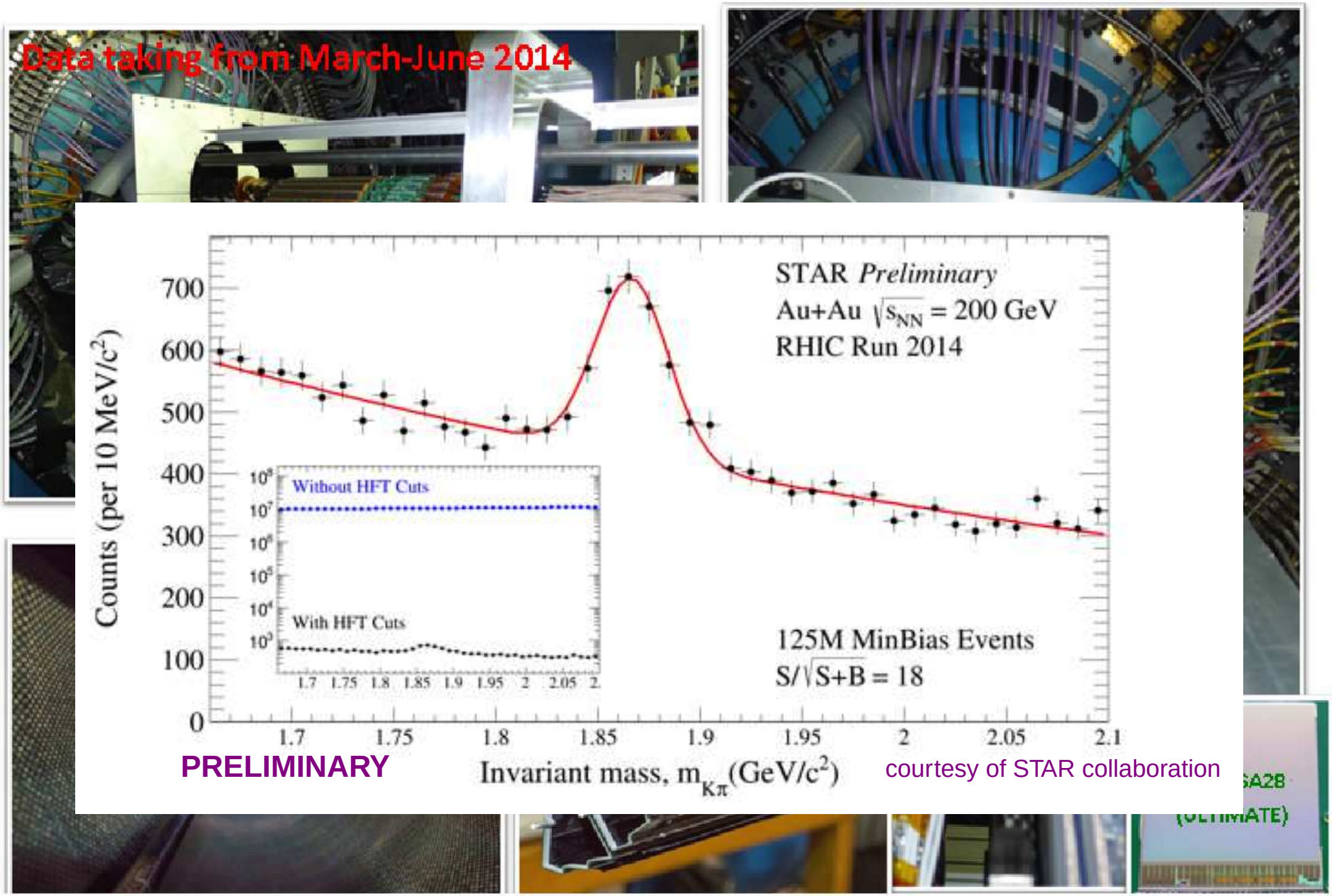



**PRELIMINARY -** courtesy of STAR collaboration




**Validation of CPS for HEP** (25/09/14 : DoE final approval, based on vertexing performance assessment)

# State-of-the-Art : STAR-PXL




**Validation of CPS for HEP** (25/09/14 : DoE final approval, based on vertexing performance assessment)

# Next Generations of High Precision Tracking & Vertexing Sub-Systems

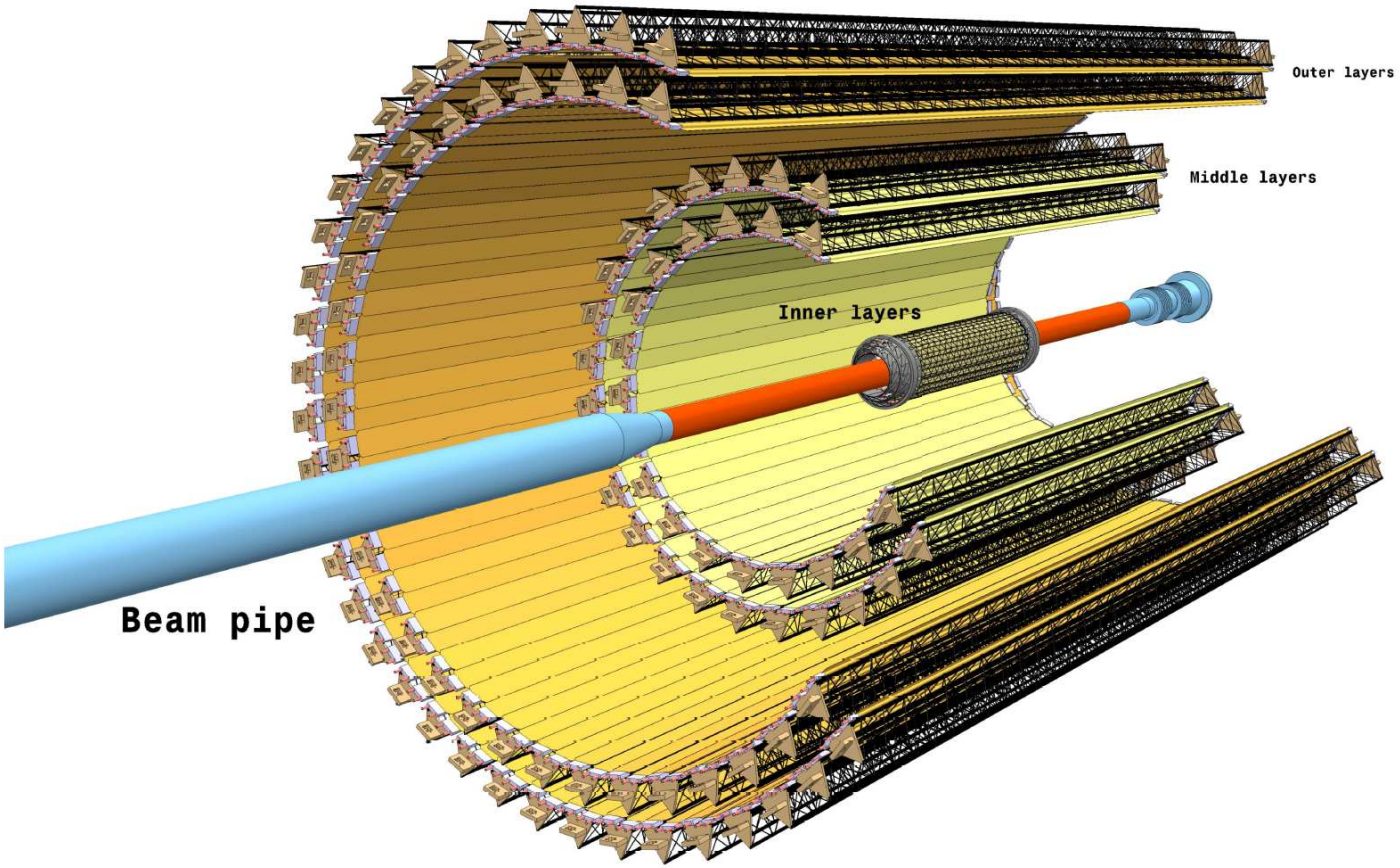
# Next Generations of High Precision Tracking & Vertexing Sub-Systems

**call for FASTER and**

**MORE RADIATION TOLERANT**

**CMOS Pixel Sensors (CPS)**

# Forthcoming Device : New ALICE Inner Tracking System



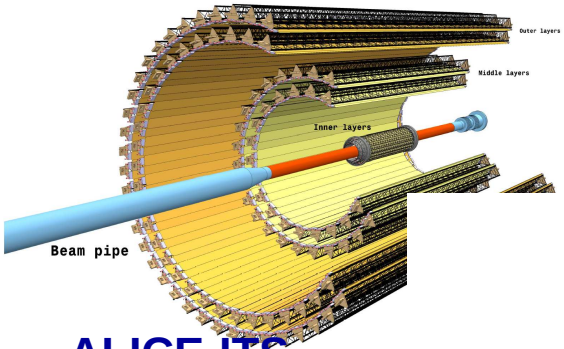

$\sigma_{sp} \lesssim 5\ \mu m$

$\simeq$ 0.3 % $X_0$ / layer

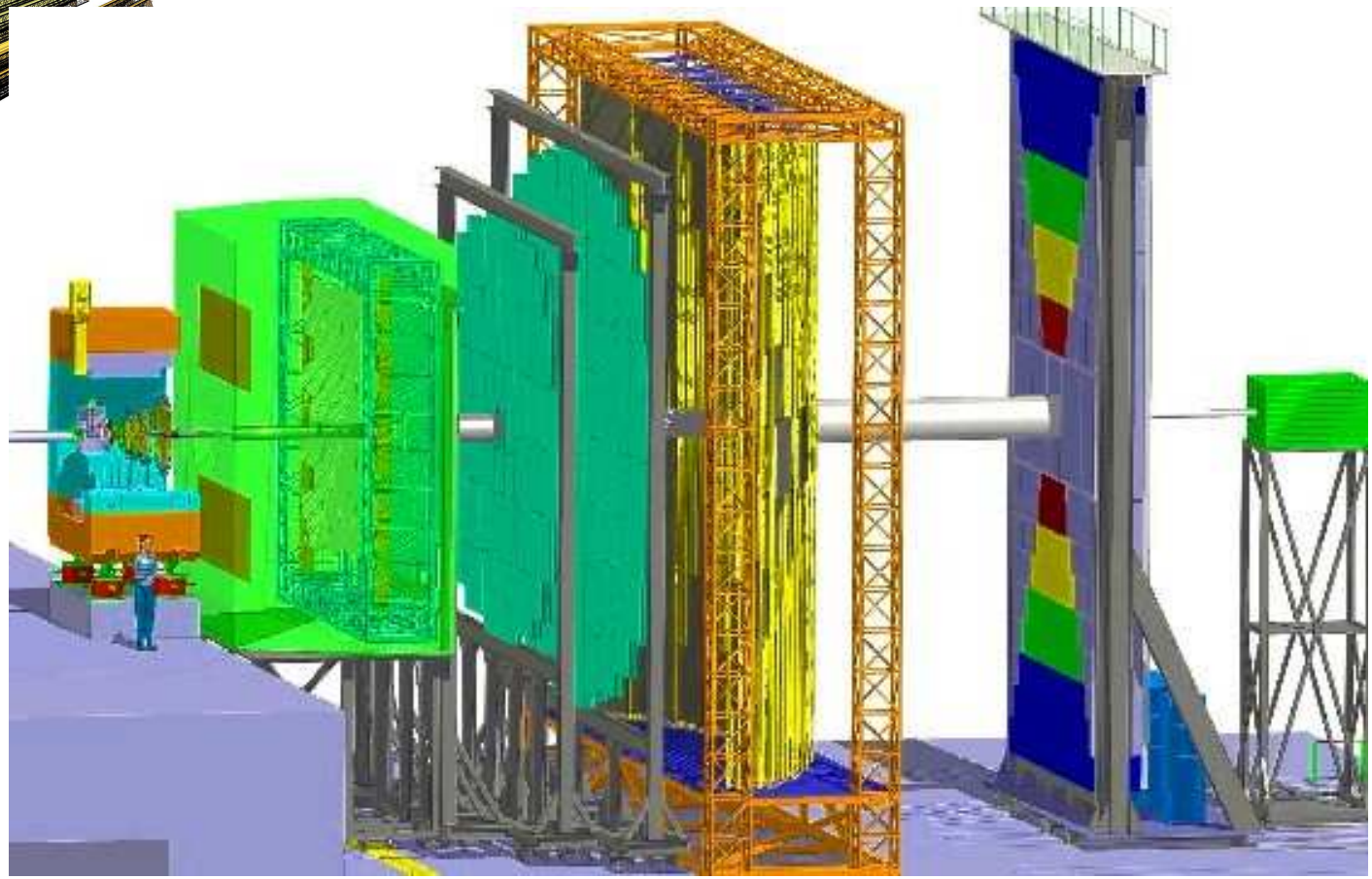
## Upgrade of ALICE-ITS at LHC

7 layers, $>$ 10 $m^2$ active area with $\gg 10^4$ CPS

# Next Forthcoming Device : CBM Micro-Vertex Detector



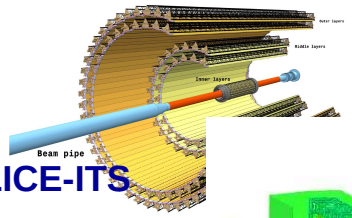

**ALICE-ITS 2018/19**



**CBM-MVD at FAIR/GSI :** **3-4** (2-sided) stations in vacuum at T $<$ 0°C

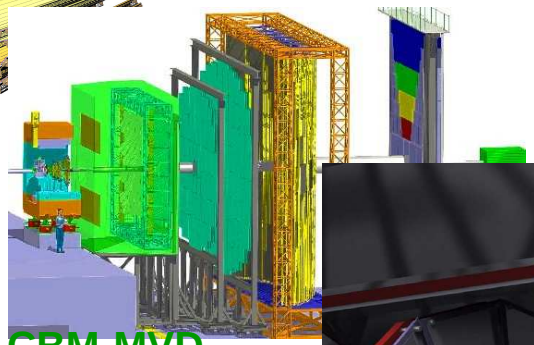
$\mapsto \sigma_{sp} \lesssim 5\ \mu m, \lesssim$ 0.5 % $X_0$/station

# Device under Study : ILC Vertex Detector




**ALICE-ITS**

**2018/19**

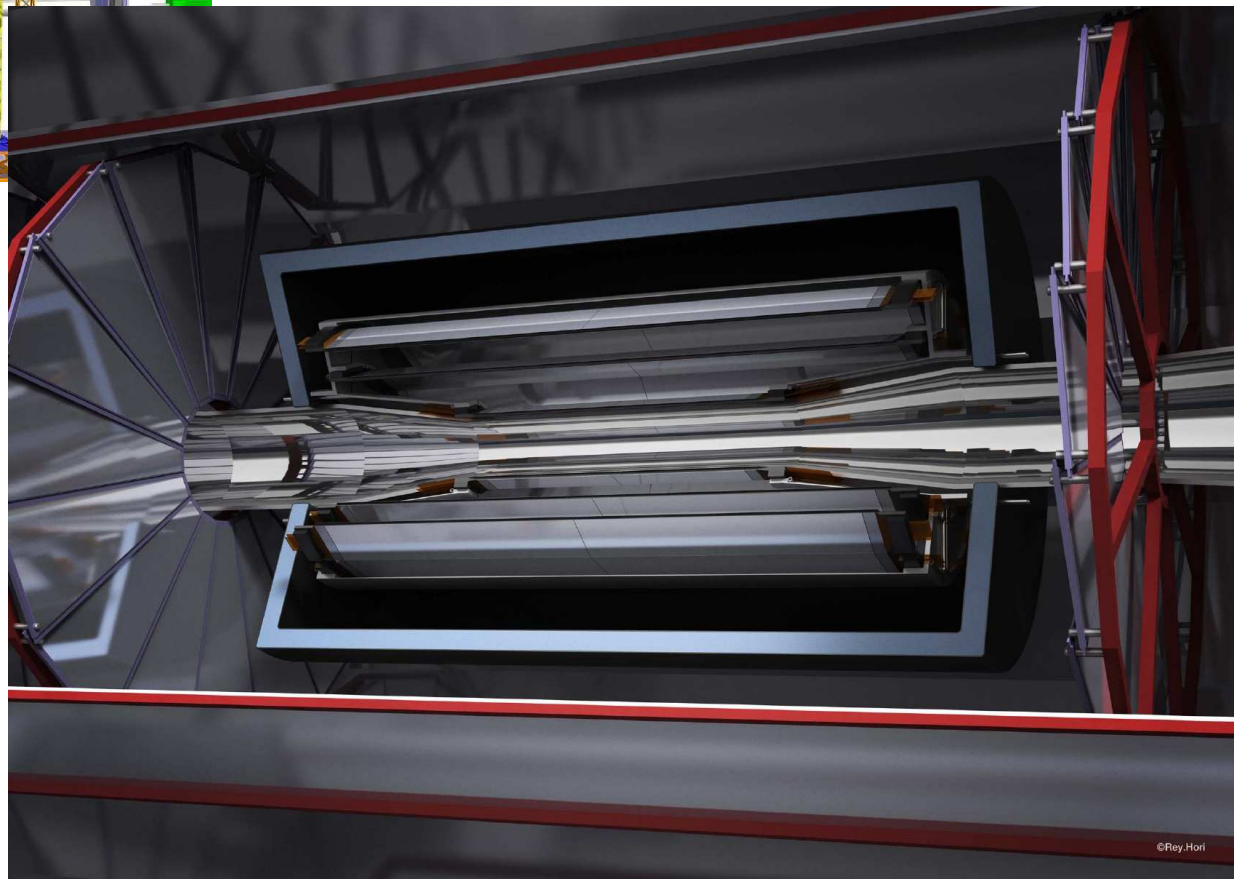


**CBM-MVD**

**$\simeq$ 2020**

**ILD-VXD**

**($>$ 2025)**




3 (2-sided) layers : CPS $\equiv$ option $\mapsto \sigma_{sp} \lesssim 3\ \mu m$, $\lesssim$ 0.3 % $X_0$/layer

# Next Challenge : ALICE-ITS Upgrade

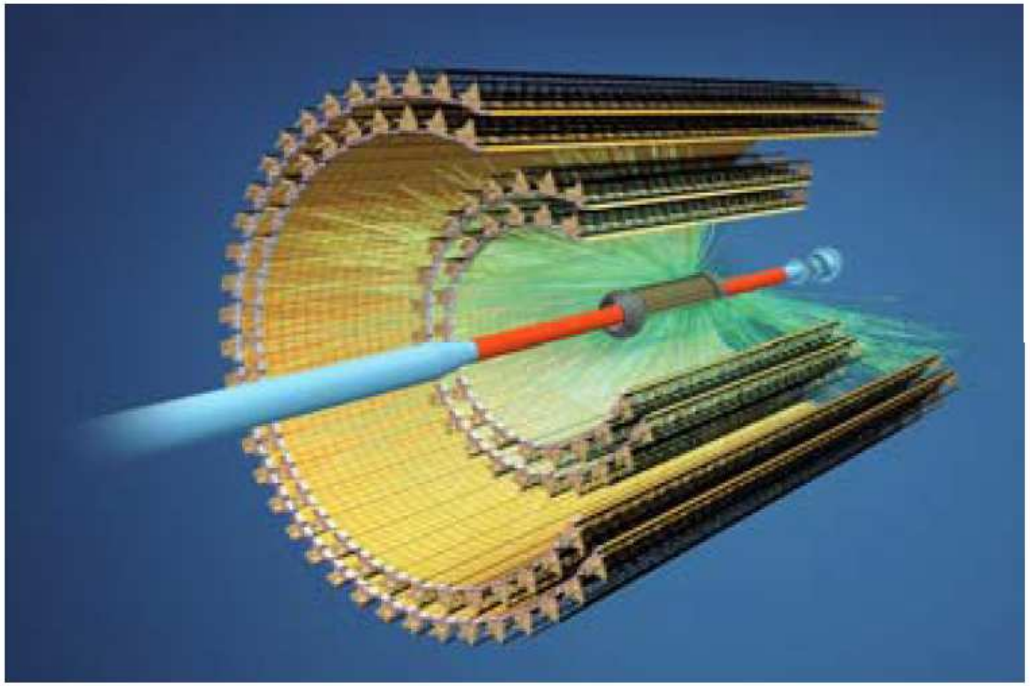
- Upgrade of ITS **entirely based on CPS** :
  - Present geometry: 6 layers

    HPS x 2 / Si-drift x 2 / Si-strips x 2
  - Future geometry : 7 layers $\longmapsto$ $\longmapsto$ $\longmapsto$

    all with CPS ($\sim$ 25-30 $\cdot$ $10^3$ chips)

    $\Rrightarrow$ 1st large tracker (10 $m^2$) using CPS
  - ITS-TDR approved March 2014 :

    Pub. in J.Phys. G41 (2014) 087002



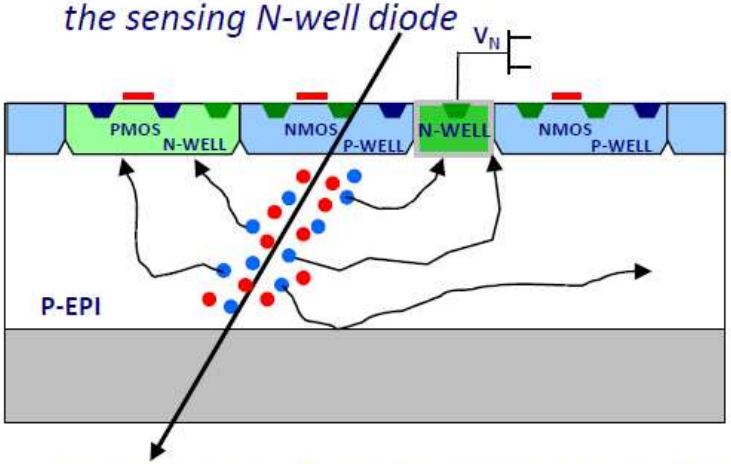
- **Requirements for ITS inner and outer barrels compared to specifications of STAR-PXL chip :**

| | $\sigma_{sp}$ | $t_{r.o.}$ | Dose | Fluency | $T_{op}$ | Power | Active area |
|---|---|---|---|---|---|---|---|
| STAR-PXL | $< 4\ \mu m$ | $< 200\ \mu s$ | 150 kRad | 3·$10^{12}$ $n_{eq}$/$cm^2$ | 30-35°C | 160 mW/$cm^2$ | 0.15 $m^2$ |
| **ITS-in** | $\lesssim 5\ \mu m$ | $\lesssim$ **30** $\mu s$ | **2.7 MRad** | **1.7·$10^{13}$ $n_{eq}$/$cm^2$** | 30°C | $<$ 300 mW/$cm^2$ | 0.17 $m^2$ |
| **ITS-out** | $\lesssim 10\ \mu m$ | $\lesssim$ **30** $\mu s$ | 15 kRad | 4·$10^{11}$ $n_{eq}$/$cm^2$ | 30°C | $<$ **100 mW/$cm^2$** | $\sim$ **10 $m^2$** |

$\Rrightarrow$ **0.35 $\mu m$ CMOS process (STAR-PXL) marginally suited to read-out speed & radiation tol.**

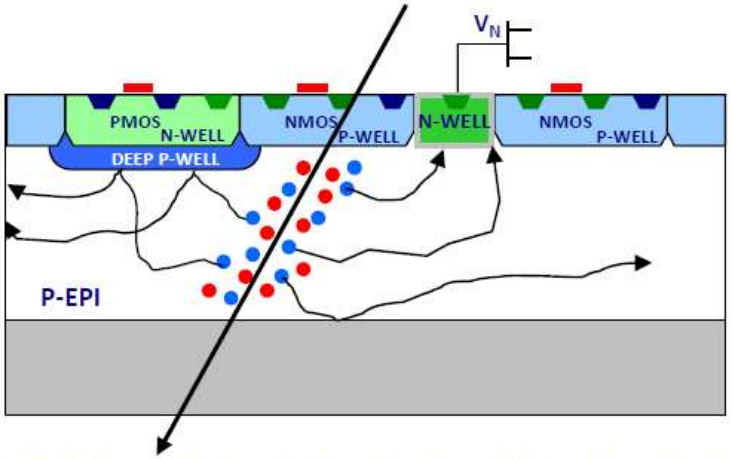
# CMOS Process Transition : STAR-PXL ⟼ ALICE-ITS

- *Twin well process: 0.6-0.35 µm*
  - *Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode*

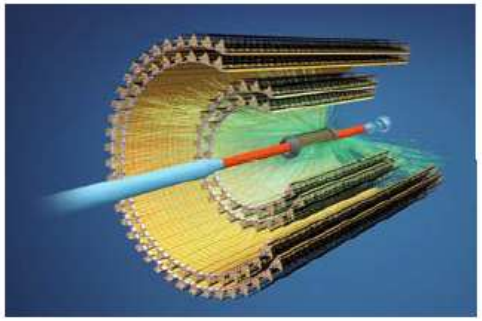



  - *Limits choice of readout architecture strategy*
  - *Already demonstrate excellent performances*
    - *STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 µm process*
      - ✓ $\varepsilon_{eff} > 99.5\%$, $\sigma < 4$ µm
    - *1st CPS based VX detector at a collider experiment*

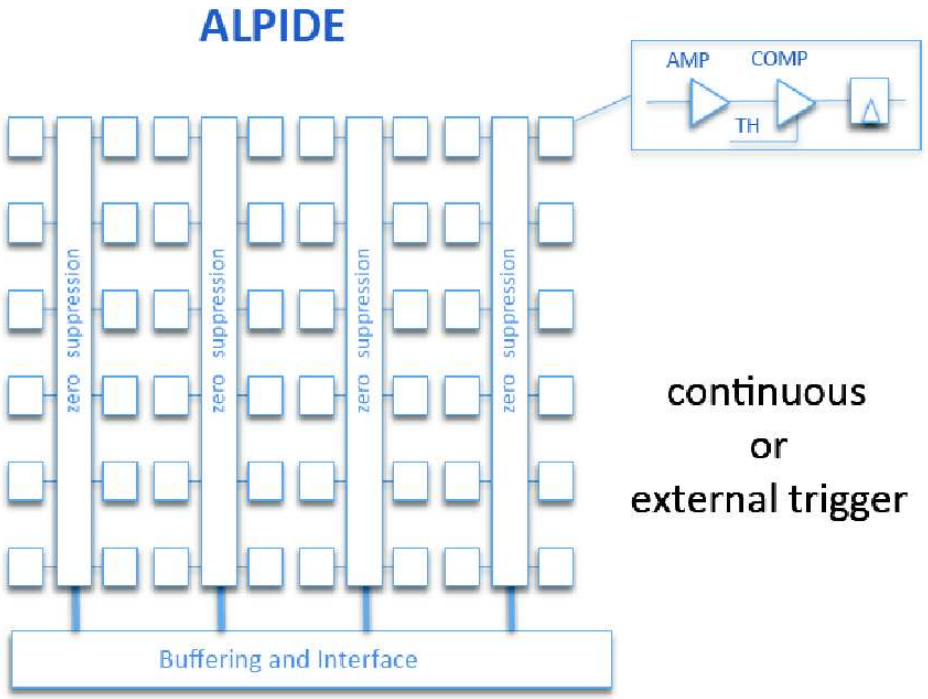
- *Quadruple well process (deep P-well ): 0.18 µm*
  - *N-well used to host PMOS transistors is shielded by deep P-well*
  - *Both types of transistors can be used*



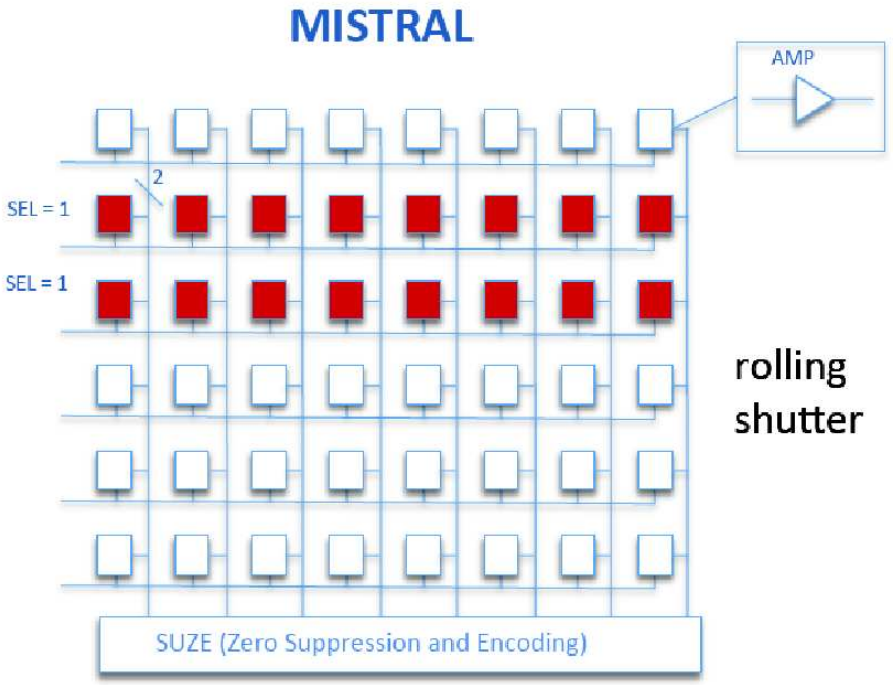

  - *Widens choice of readout architecture strategies*
    - *Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18 µm process (quadruple well)*
      - *Synchronous Readout R&D:*
        - ✓ *proven architecture = safety*
      - *Asynchronous Readout R&D: challenging*



# ITS Pixel Sensor : Two Architectures




continuous
or
external trigger




rolling
shutter

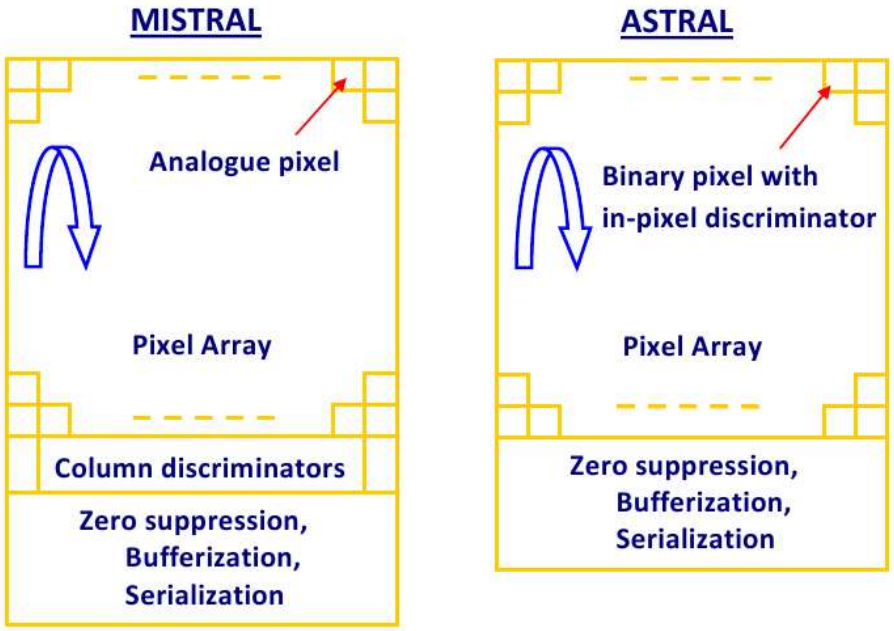
| | |
|---|---|
| **Pixel dimensions** | **27$\mu m$ x 29$\mu m$** |
| **Event time resolution** | **4$\mu s$** |
| **Power consumption** | **$<$ 50mW/cm$^2$** |
| **Insensitive area** | **$\sim$ 1mm x 30mm** |

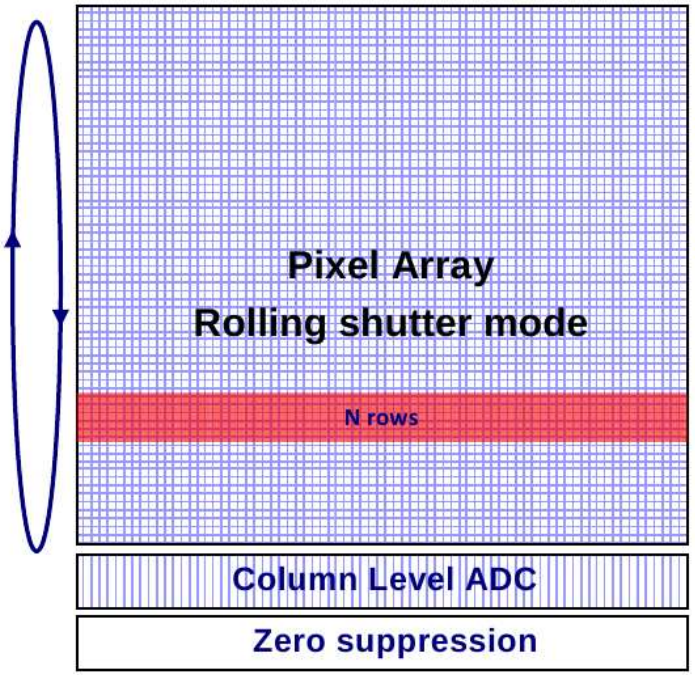
| | |
|---|---|
| **Pixel dimensions** | **36$\mu m$ x 65$\mu m$** |
| **Event time resolution** | **20$\mu s$** |
| **Power consumption** | **$\lesssim$ 90mW/cm$^2$** |
| **Insensitive area** | **1.5mm x 30mm** |

- **Both chips have identical dim. (15mm x 30 mm) as well as physical and electrical interfaces:**
  - ⁕ position of interface pads
  - ⁕ electrical signaling
  - ⁕ steering, read-out, ... protocoles

# Synchronous Read-Out Architecture : Rolling Shutter Mode

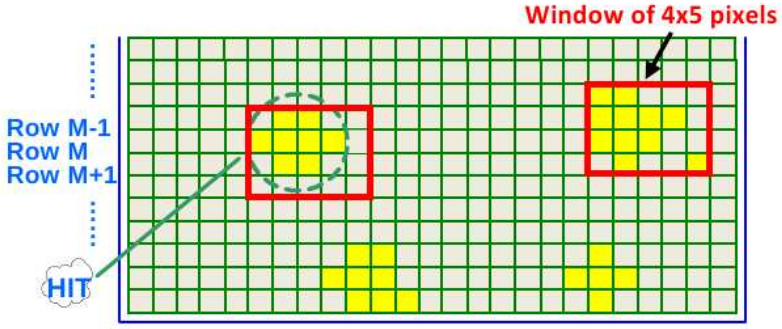
- *Design addresses 3 issues:*
  - *Increasing S/N at pixel-level*
  - *A to D Conversion: at column-level (MISTRAL)*
    *at pixel-level (ASTRAL)*
  - *Zero suppression (SUZE) at chip edge level*



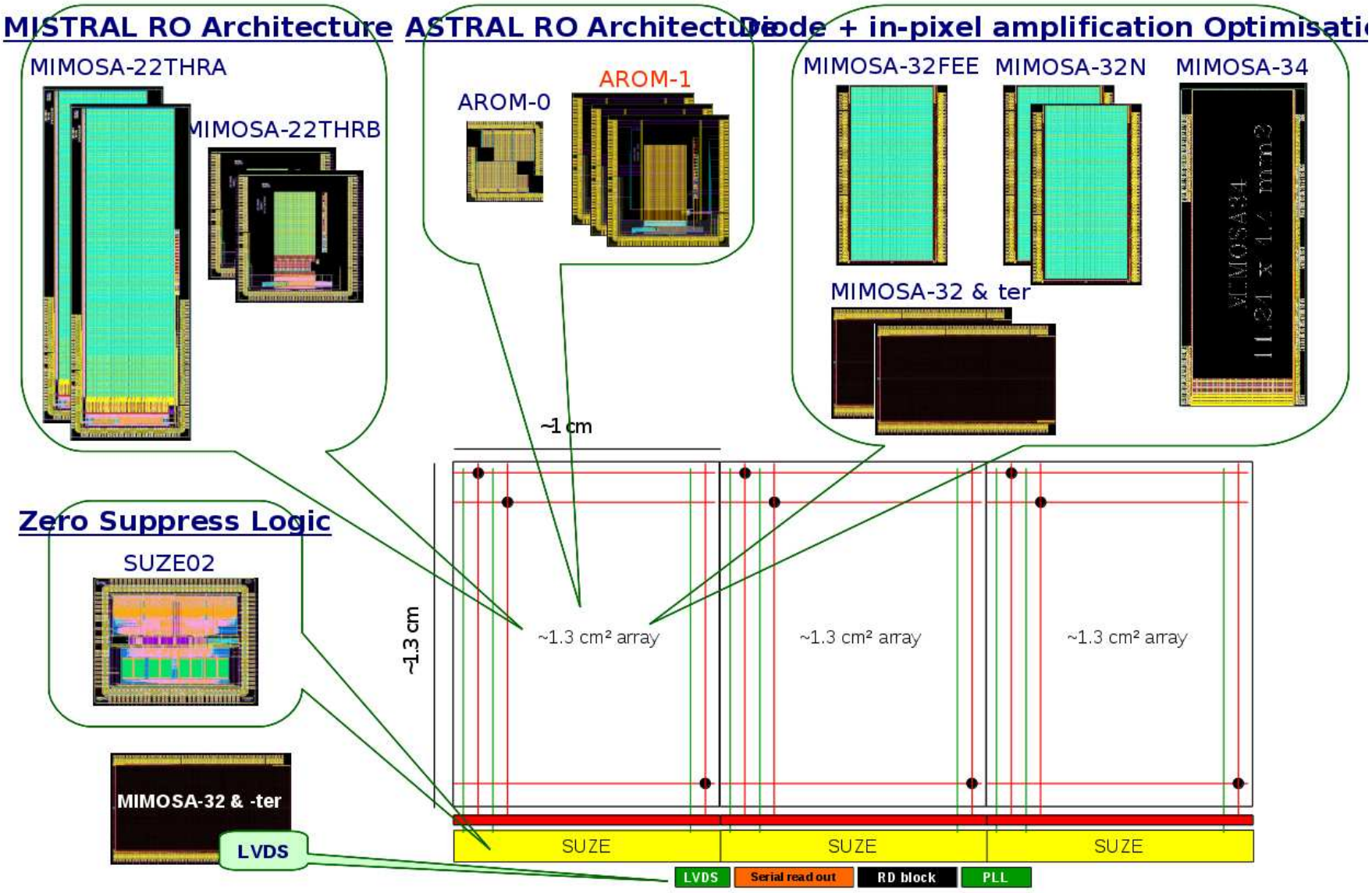




- *Power vs speed:*
  - *Power: only the selected rows (N=1, 2, …) to be read out*
  - *Speed: N rows of pixels are read out in //*
    - *Integration time = frame readout time*

$$t_{\text{int}} = \frac{(\text{Row readout time}) \times (\text{No. of Rows})}{N}$$



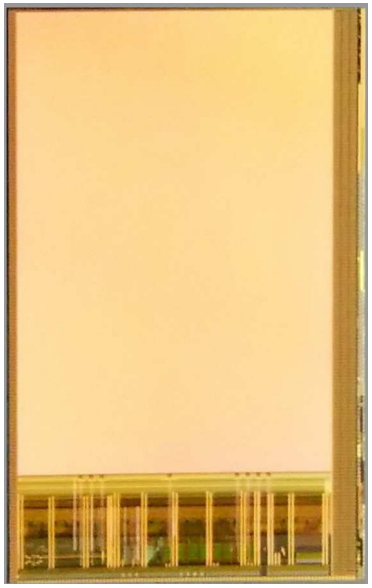
# Sensor Development Organisation



# Main Features of the Final Prototypes

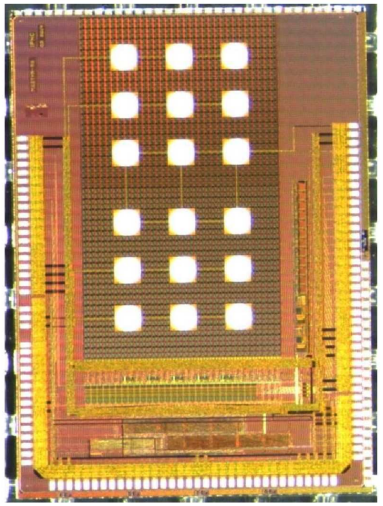
- **Full scale sensor building block :**
  - complete (fast) read-out chain $\simeq$ ULTIMATE
  - pixel area ($\sim$ 1 cm$^2$) $\simeq$ area of final building block
  - same nb of pixels (160,ooo) than complete final tracker chip
  - fabricated with 18 $\mu$m thick high-resistivity EPI
  - BUT : pixels are small (22 x 32.5 $\mu m^2$) and sparsification circuitry is oversized (power !)
  - **Tested at DESY (few GeV e$^-$) in June'15 and CERN-SPS (120 GeV "pions") in Oct. '15**

**FSBB-M0bis**



- **Large-pixel prototype without sparsification :**
  - 2 slightly different large pixels :
    - 36.0 $\mu$m x 62.5 $\mu$m
    - 39.0 $\mu$m x 50.8 $\mu$m
  - pads over pixels (3 ML used for in-pixel circuitry)
  - fabricated with 18 $\mu$m thick high-resistivity EPI
  - BUT : only $\lesssim$ 10 mm$^2$, 4,ooo pixels, no sparsification
  - **Tested in Frascati (450 MeV e$^-$) in March & May'15**

**MIMOSA-22THRb**



# Detection Performances of the Final Prototypes

- **Full scale sensor building block :**
  - complete (fast) read-out chain $\simeq$ ULTIMATE
  - pixel area ($\sim$ 1 cm$^2$) $\simeq$ area of final building block
  - same nb of pixels (160,ooo) than complete final tracker chip
  - fabricated with 18 $\mu$m thick high-resistivity EPI
  - BUT : pixels are small (22 x 32.5 $\mu m^2$) and sparsification circuitry is oversized (power !)
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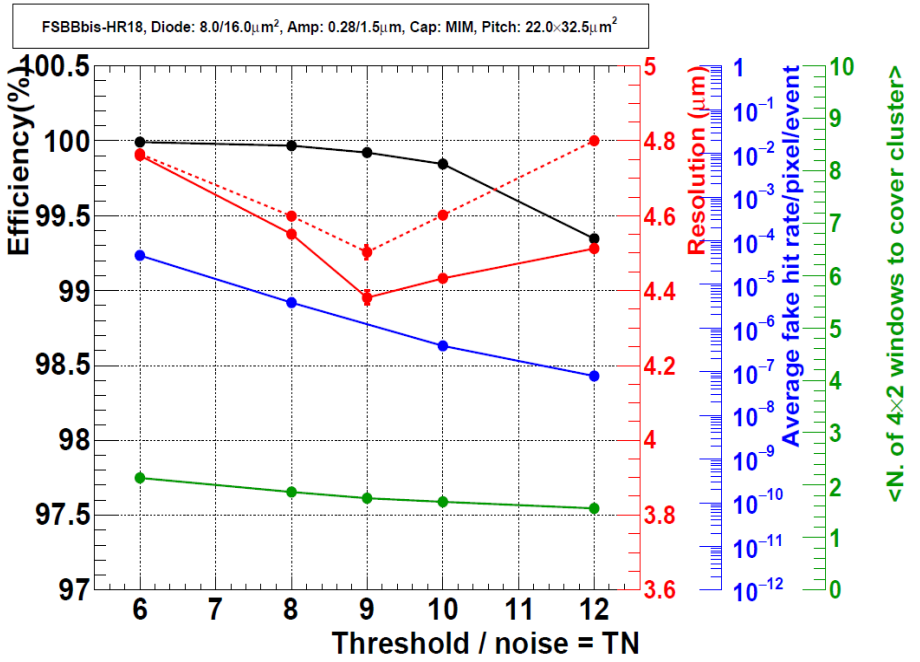


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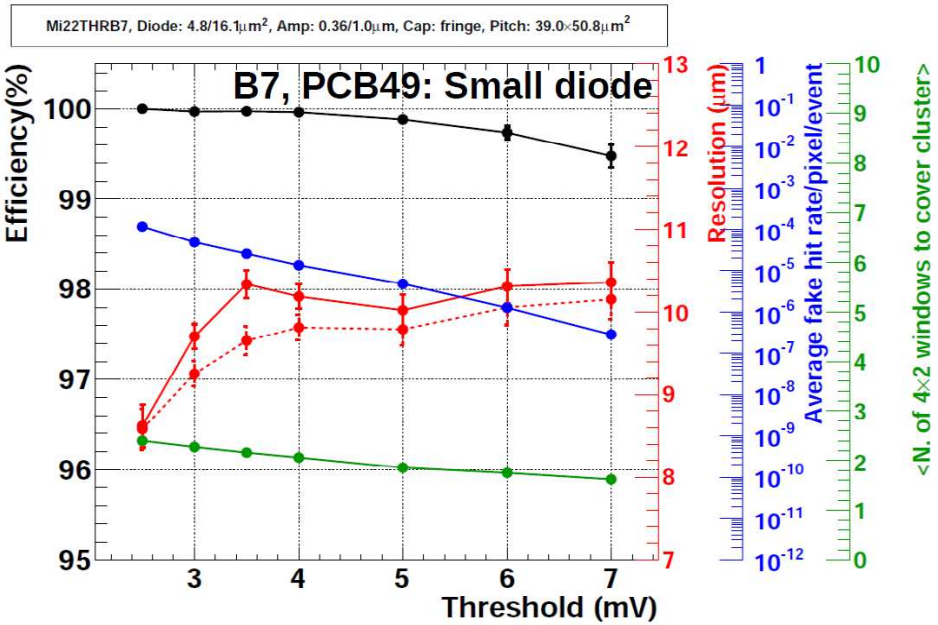
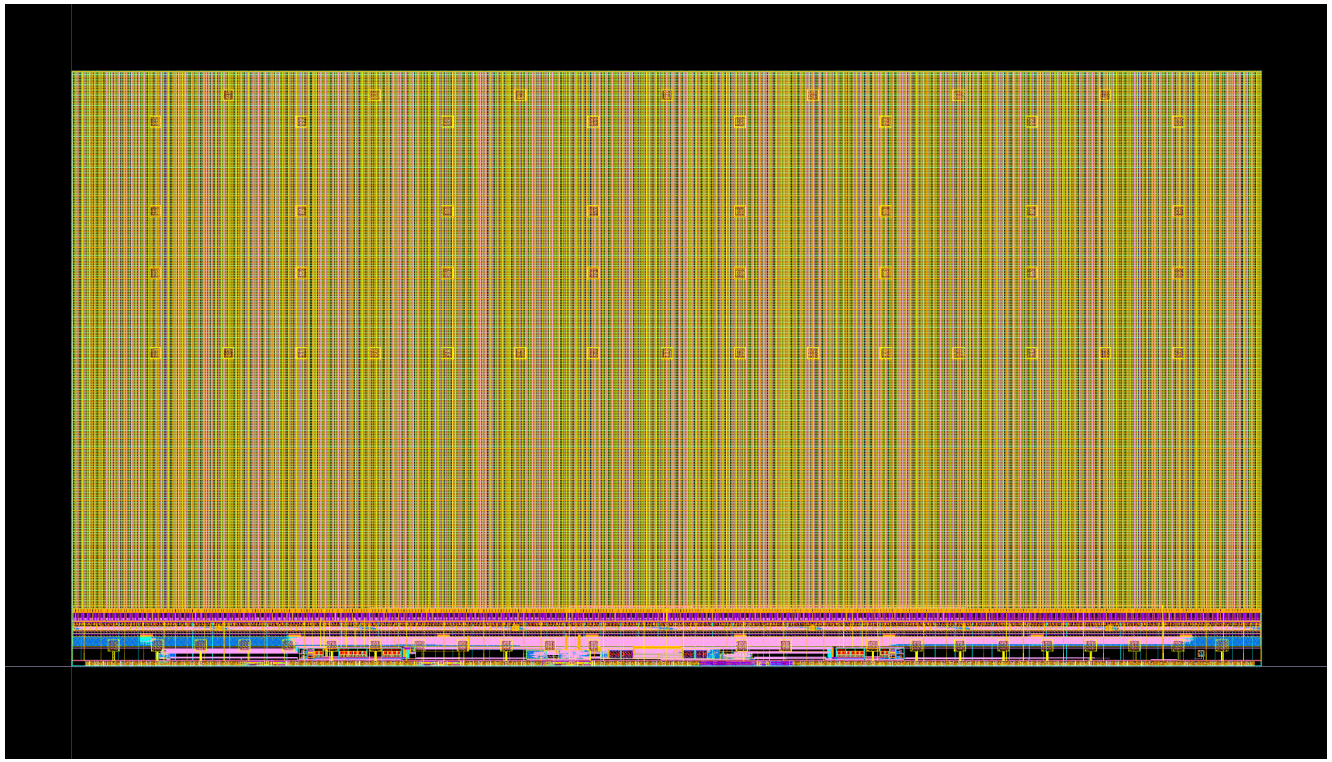


# Final Sensor : MISTRAL-O

- **Combination of 4 FSBBs with MIMOSA-22THRb7 pixels**
- **Main characteristics :**
  - chip dimensions : 15 mm x 30 mm
  - Sensitive area = 13.50 mm x 29.95 mm
    - ↪ 1.5 mm wide side band (evolving towards $\sim$ 1 mm)
  - 832 columns of 208 pixels (1.6 $10^5$ pixels)
  - pixel dimensions : 36 $\mu m$ x 65 $\mu m$
  - in-pixel pre-amp & clamping (fringe capa)
  - end-of-column signal discrimination
  - discriminators' output sparsification
  - fully programmable control circuitry
  - pads over pixel array
  - possibility to mask noisy pixels

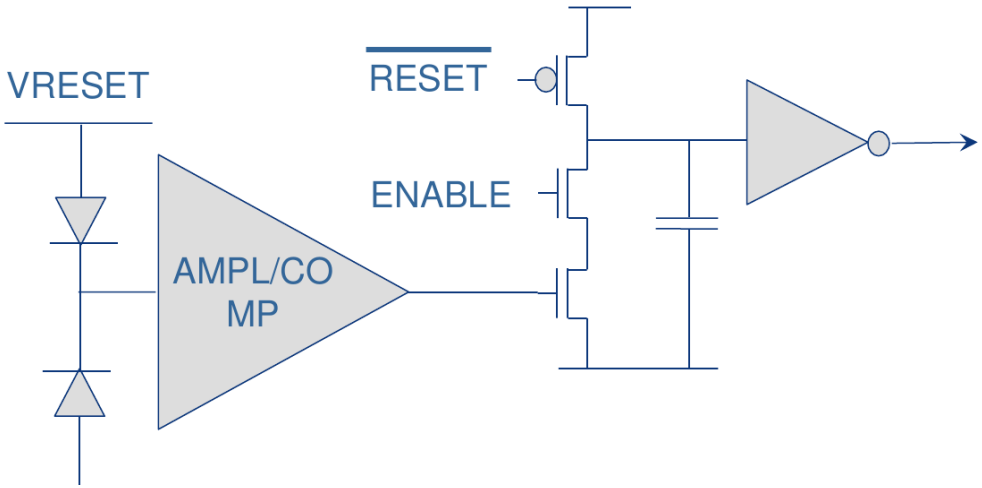


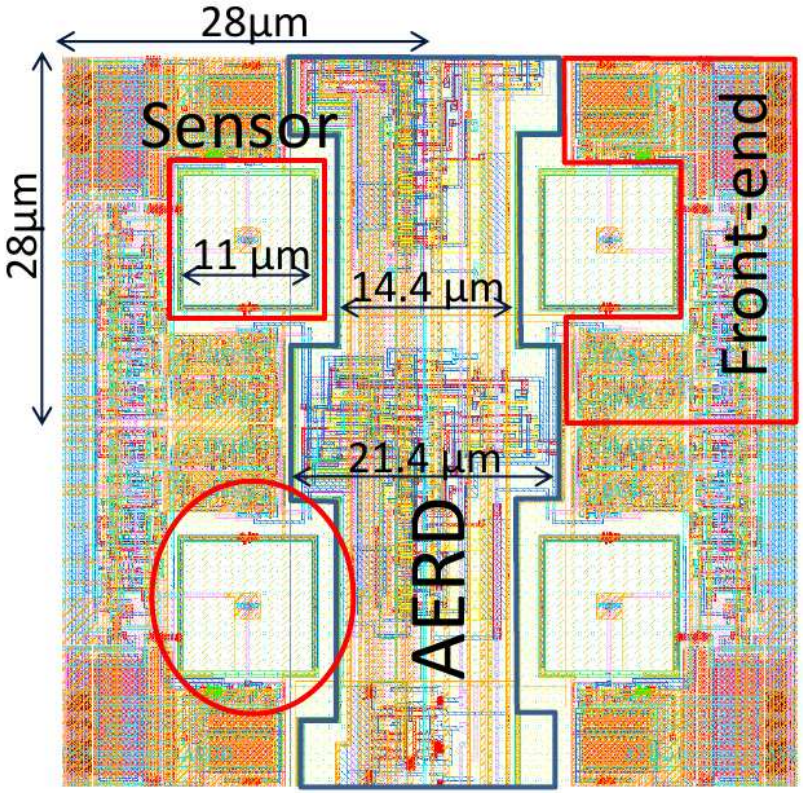
- **Typical performances :** (based on FSBB and MIMOSA-22THRb7 beam tests)
  - read-out time $\sim$ 20 $\mu s$
  - spatial resolution $\sim$ 10 $\mu m$
  - power density $\lesssim$ 90 mW/cm$^2$
  - radiation tolerance $>$ 1.5·$10^{12}$ $n_{eq}$/cm$^2$ and 150 kRad at T $>$ 30°C

# Asynchronous Read-Out Architecture : ALPIDE (Alice PIxel DEtector)

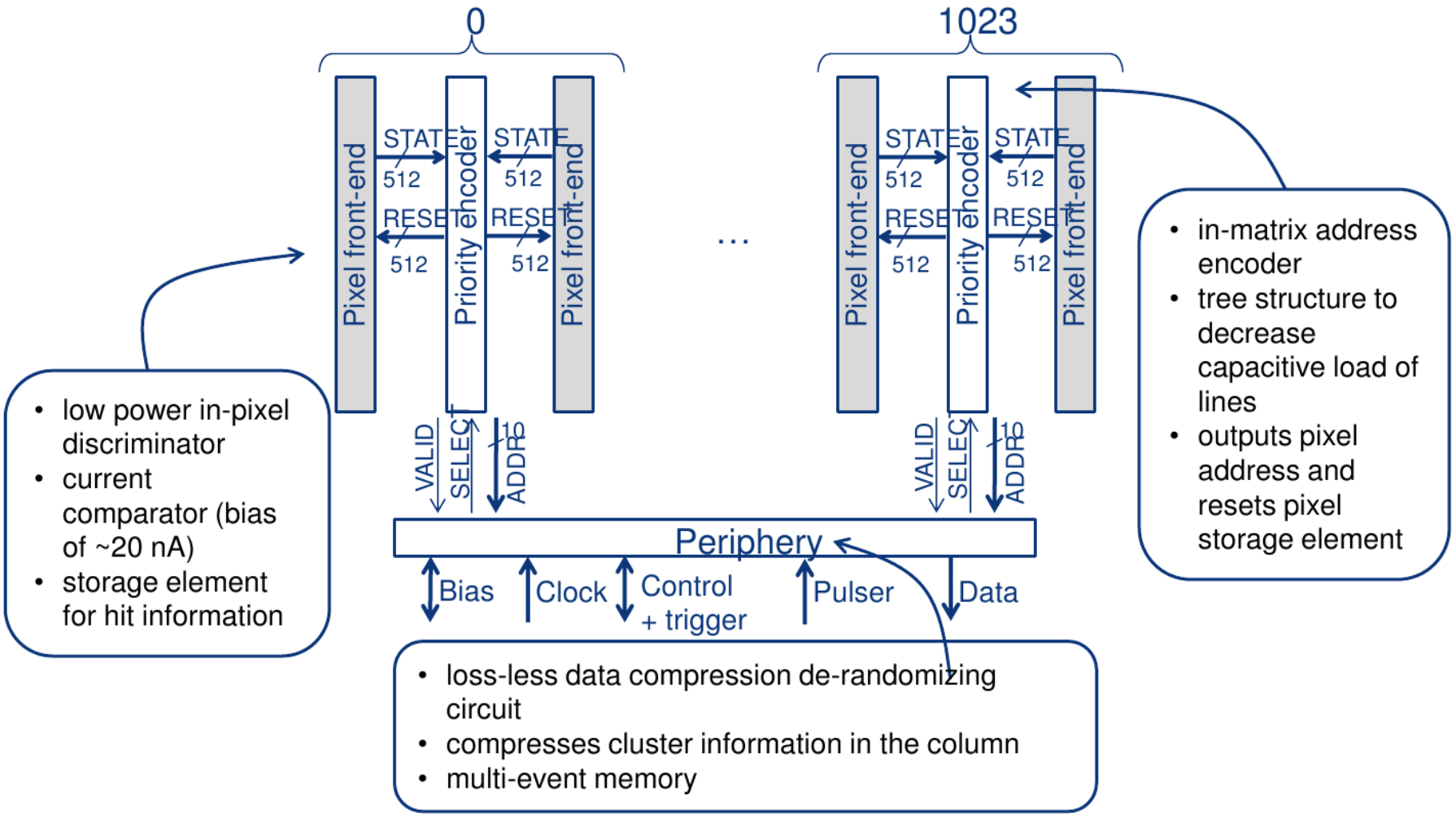
- **Design concept similar to hybrid pixel read-out architecture**
  **exploiting availability of TJsc CIS quadruple well process :** pixel hosts N- & P-MOS transistors

- **Each pixel features a continuously power active**
  - low power consumming analogue front end (P $<$ 50 nW/pixel)
    based on a single stage amplifier with shaping / current comparator
    - amplification gain $\sim$ 100
    - shaping time $\sim$ few $\mu s$
  - Data driven read-out of the pixel matrix
    $\Rrightarrow$ only zero-suppressed data are transfered to periphery



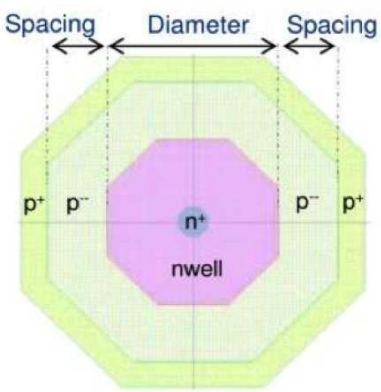



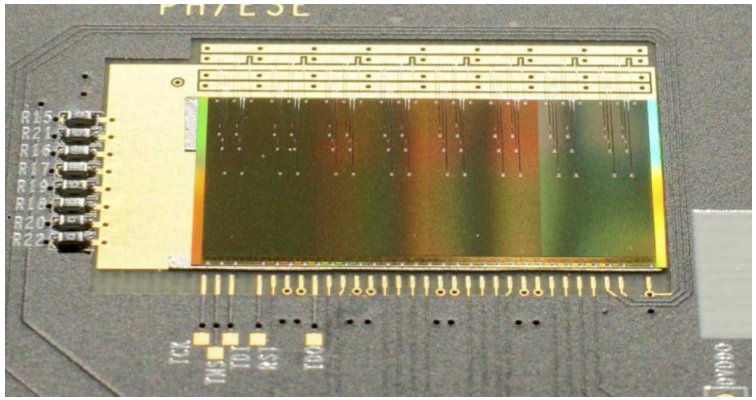
# Asynchronous Read-Out Architecture : ALPIDE

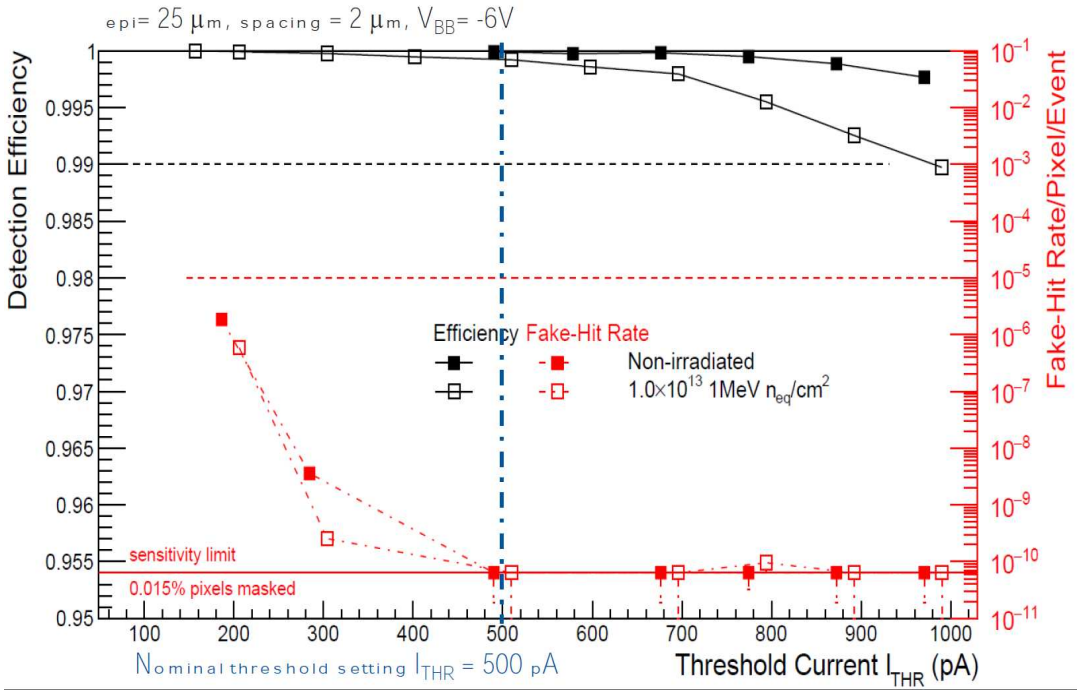


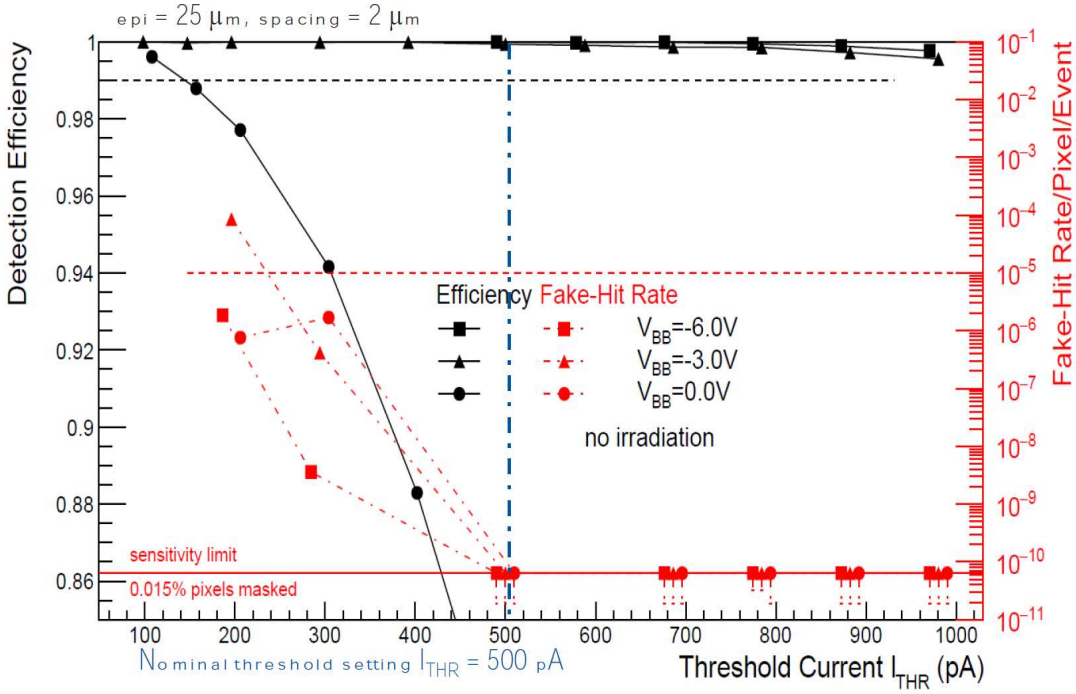
# ALPIDE Detection Performance Assessment

- **ALPIDE-2 beam tests :**
  - Final sensor dimensions : 15 mm $\times$ 30 mm
  - About 0.5 M pixels of 27 $\mu m \times 29\ \mu m$
  - Various sensing node geometries studied
  - Substrate reverse biased for the sake of SNR
    - ↪ default : - 6 V
  - Possibility to mask pixels (fake rate mitigation)
    - ↪ default : $\lesssim$ O($10^{-3}$) masked pixels



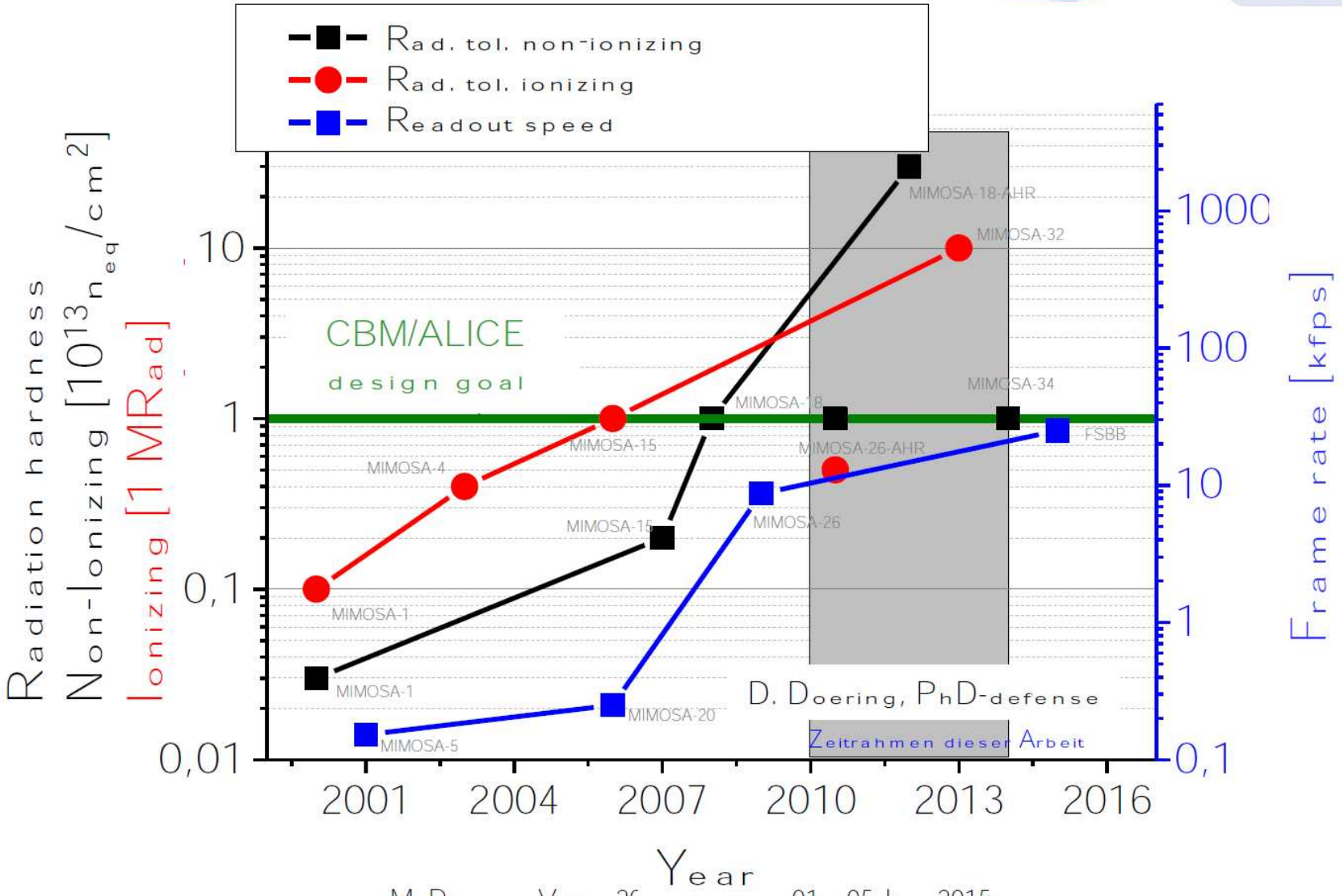


# Radiation Tolerance

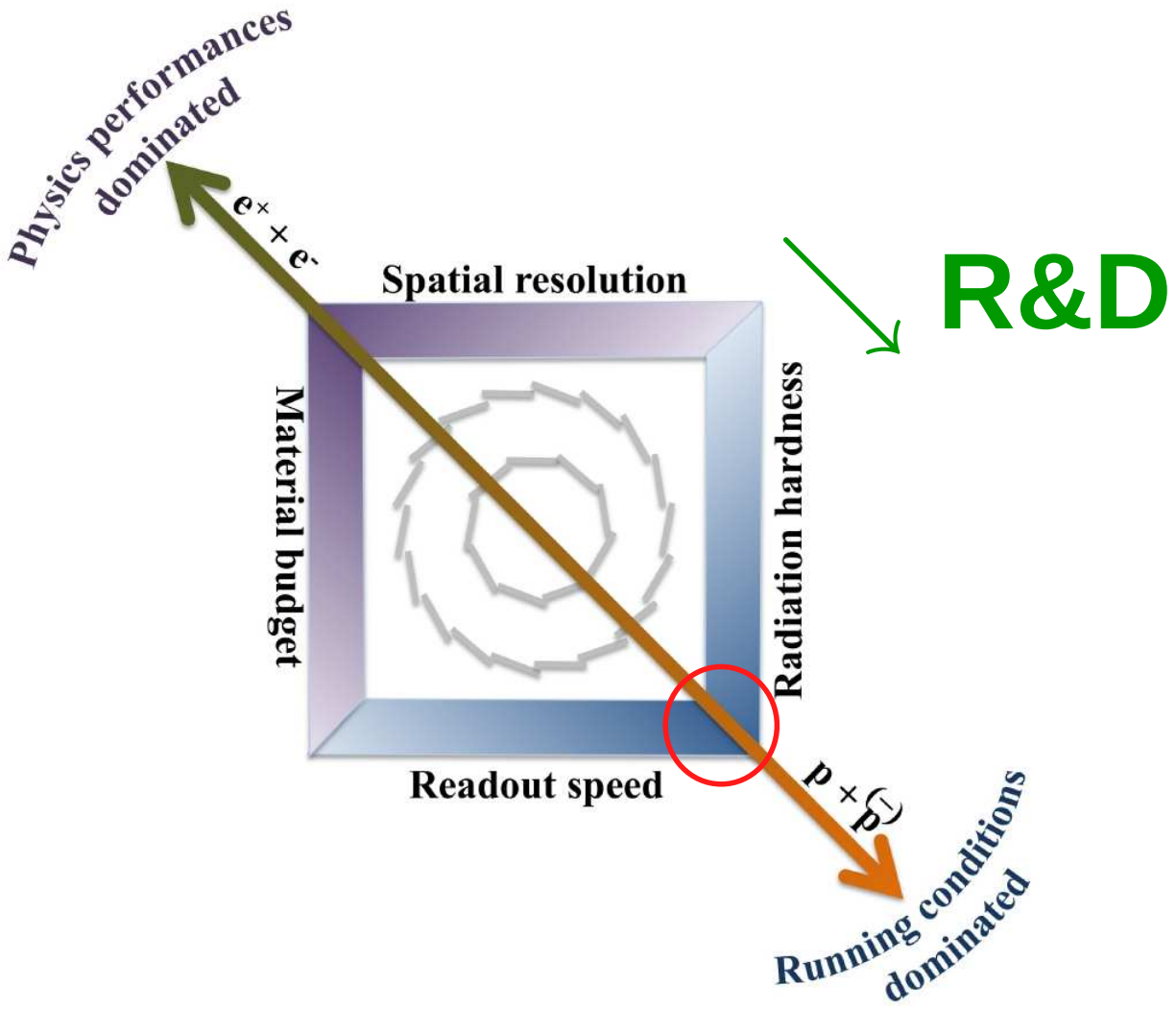
Material budget: 0.05% $X_0$

Spatial resolution: ~ 3-5 µm



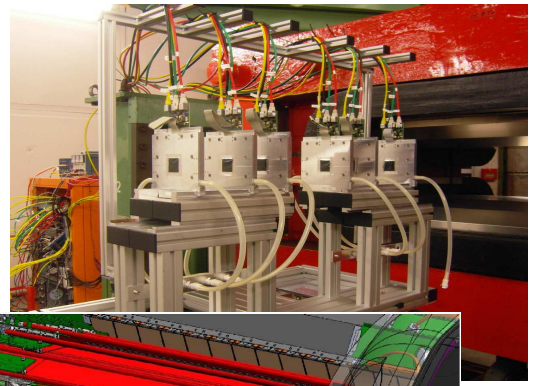
# Forthcoming Challenges

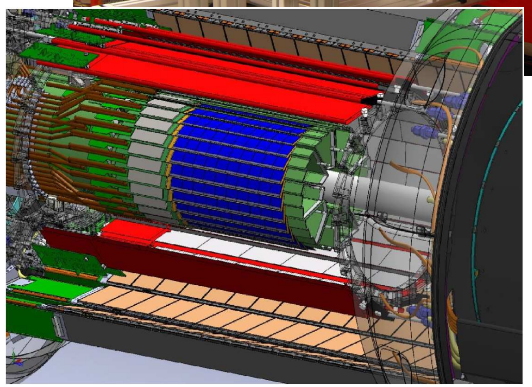
*How to reach the bottom right corner of the "Quadrature" ?*



# Improving Speed and Radiation Tolerance

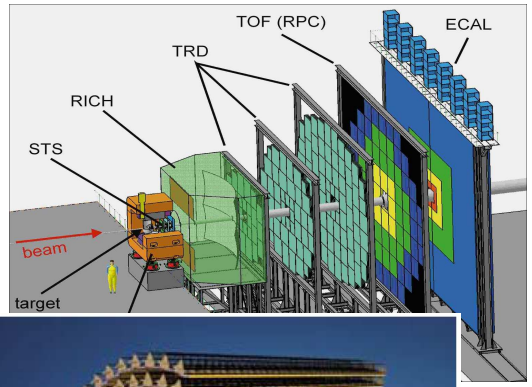
**O($10^2$)** $\mu s$

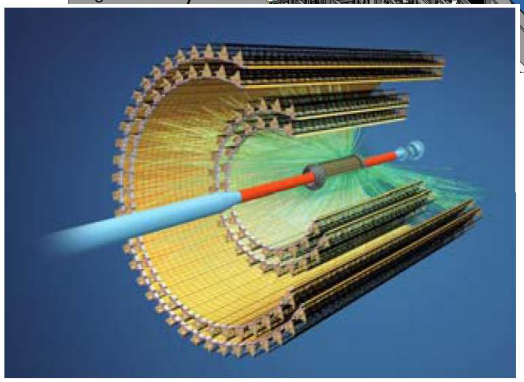




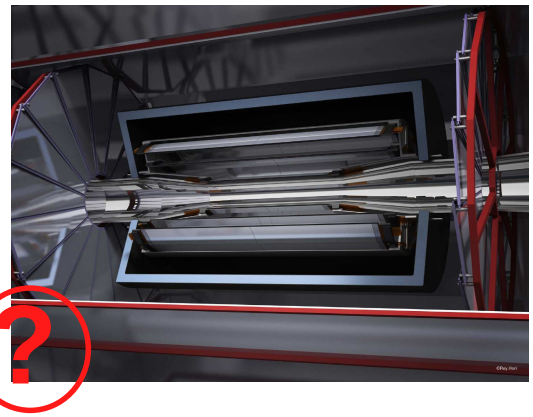
*How to improve speed & radiation tolerance while preserving 3-5 $\mu m$ precision & $<$ 0.1% $X_0$ ?*

**O(10)** $\mu s$



**O(1)** $\mu s$




**EUDET/STAR** $\longmapsto$ **ALICE/CBM** $\longmapsto$ **?X?/ILC**

2010/14 $\longmapsto$ 2015/2019 $\longmapsto$ $\gtrsim$ 2020

# Enhancing the Epitaxial Layer Depletion

- **Motivations for High Energy Physics :**
  - Tolerance to Non-Ionising radiation
  - Charge collection speed

    $\Rightarrow$ integration time $\ll \mu s$

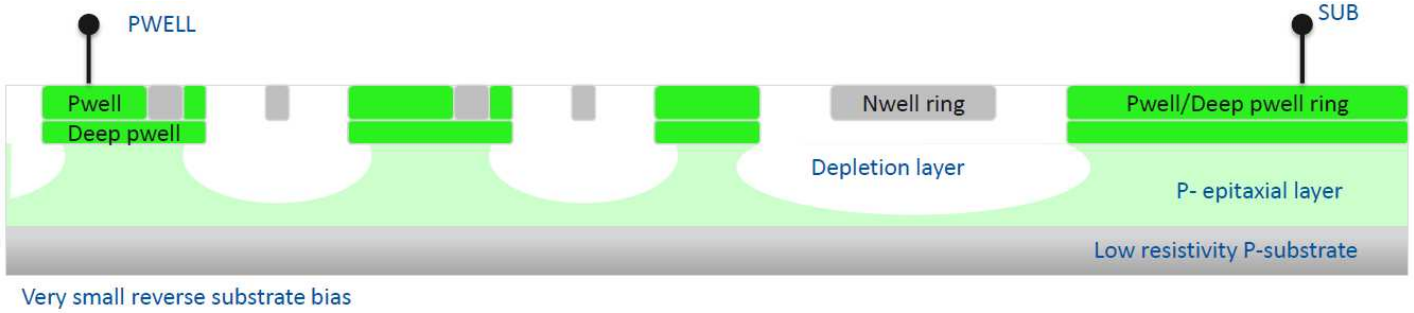
- **Motivations for X-Ray detection :**
  - Thickness of sensitive vol. (Beer-Lambert law)
  - Uniformity of det. prop. across sensitive area

- **Alternative top-down ($\equiv$ reverse) biasing approaches :**
  - Electrode voltage

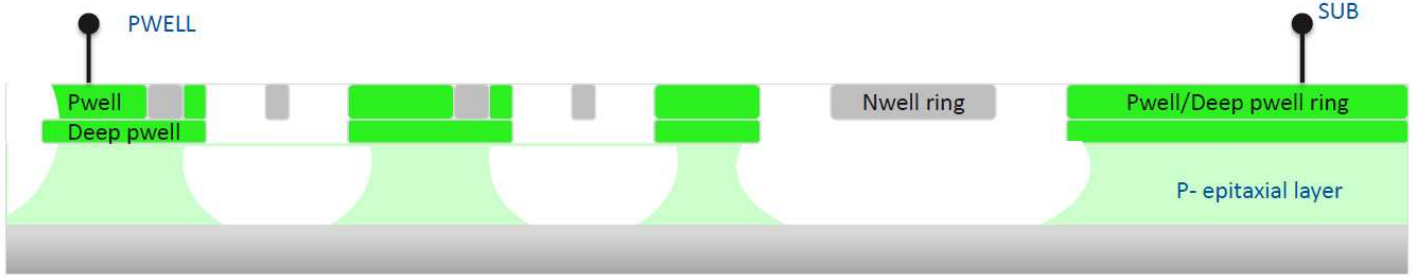
    Ex: ALPIDE: P+ wells $\longrightarrow$
  - Sensing diode potential

    $\Rightarrow$ decoupled from Pre-Amp

    (see next slides)



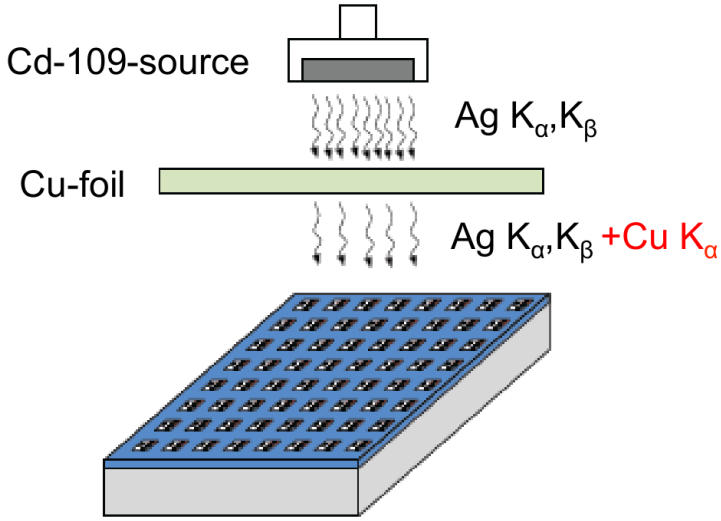
Very small reverse substrate bias

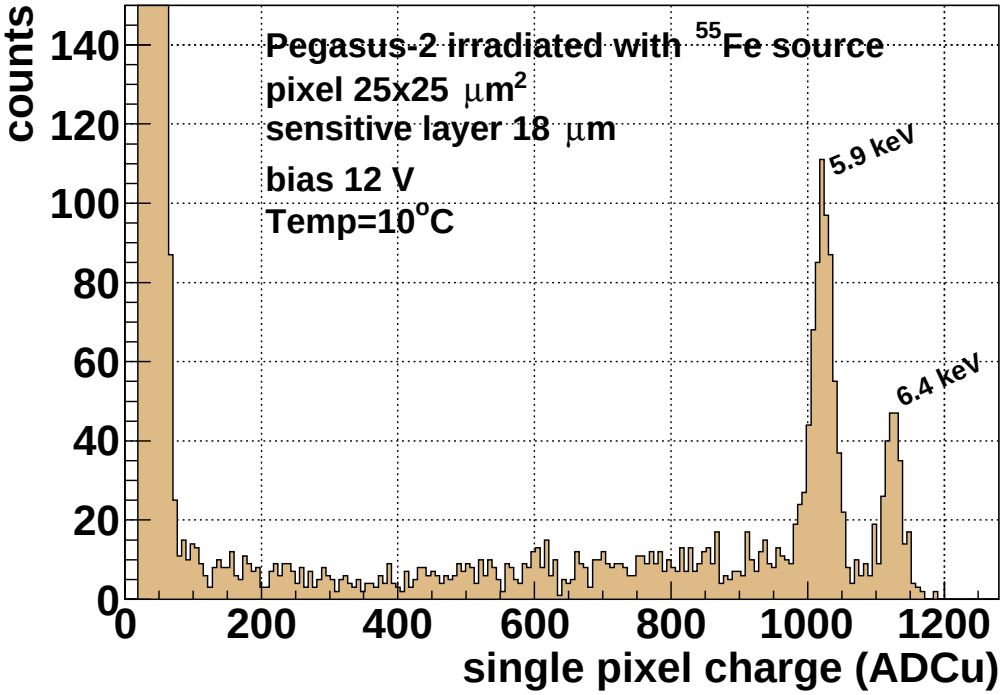


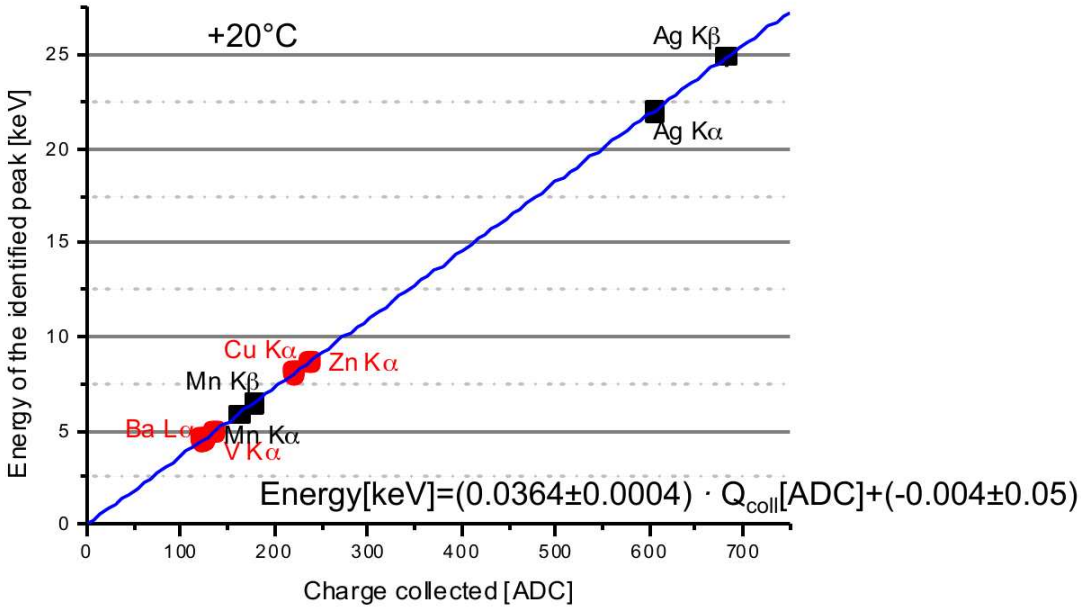
Larger reverse substrate bias

# Epitaxial Layer Depletion via Sensing Diode

- **Pegasus-2 sensor:**
  - Tower-Jazz 0.18 CIS process
  - 56 x 8 pixels (25 $\mu m$ pitch)
  - Epitaxy: 18 $\mu m$, 1 k$\Omega \cdot cm$ predominantly depleted
  - TN $\simeq$ 16 $\pm$ 1 e$^-$ ENC at 10$^\circ$C



# CONCLUSION

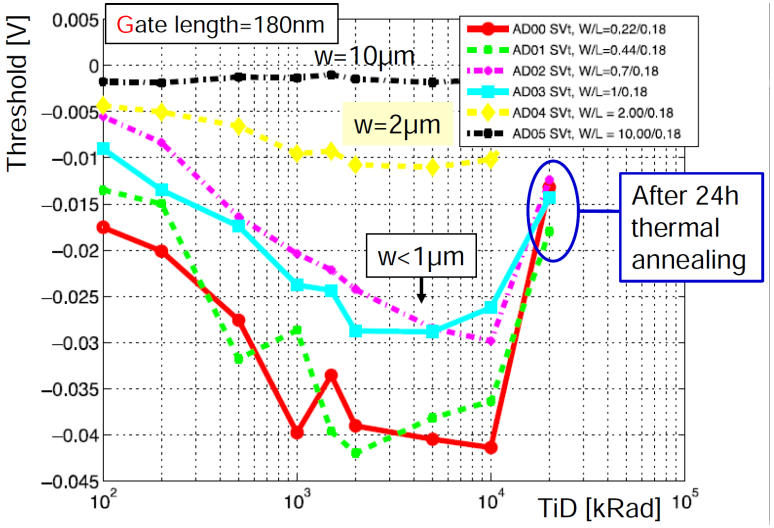
- **CPS based on rolling shutter r.o. (mainly AMS-0.35 process) now in use for several years:**
  - Beam Telescopes providing precision tests on multi-GeV $\rightarrowtail$ sub-GeV $e^{\pm}$ beams (DESY, LNF)
  - Vertex detectors providing unprecedented flavour tagging capabilities (STAR-PXL, FIRST)
  - Various spin-offs

- **Tower-Jazz 0.18 $\mu m$ CIS technology now under control :**
  - Techno. validated for charged particle detection with full custom epitaxy (thickness, resistivity)
  - STAR-PXL chip successfuly translated: 2-4 times faster & $\gtrsim$ 10 times more rad. tolerant
  - New, asynchronous r.o., CPS progressing rapidly towards $<$ 10 $\mu s$ (active depletion)
  - 1st large (10 $m^2$) pixelated tracker (ALICE-ITS) soon starting construction (25,ooo CPS)

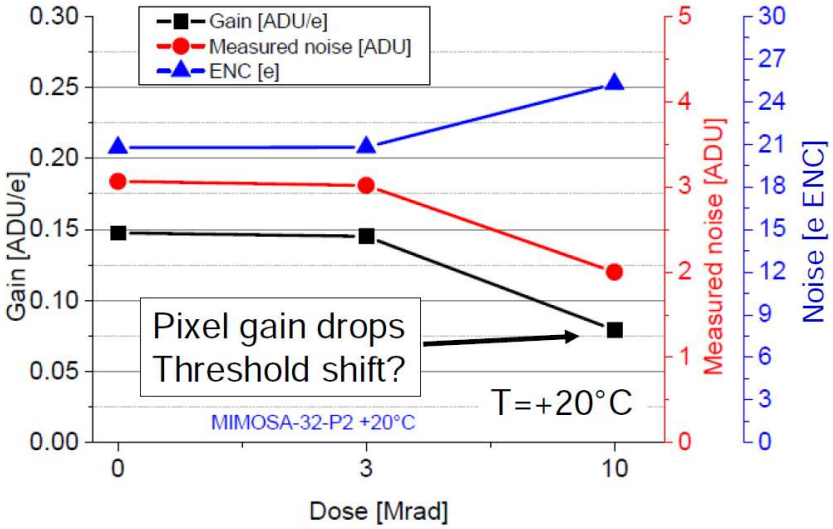
- **Perspectives:**
  - few $\mu s$ read-out CPS for CBM expt at FAIR and ILC in Japan
  - depleted epitaxy CPS for low energy X-Ray imaging based on photon counting
  - beta-imaging based on counting

# Tolerance to Ionising Radiation

- **Studies of 0.18 $\mu m$ transistors exposed to TID $\geq$ 10 MRad**
  - measurements performed (+20°C) :
    leakage current & threshold shift
  - increase of leakage current remains small
  - threshold shifts remain small if W $\gtrsim 2\mu m$
    and are recoverable with thermal annealing



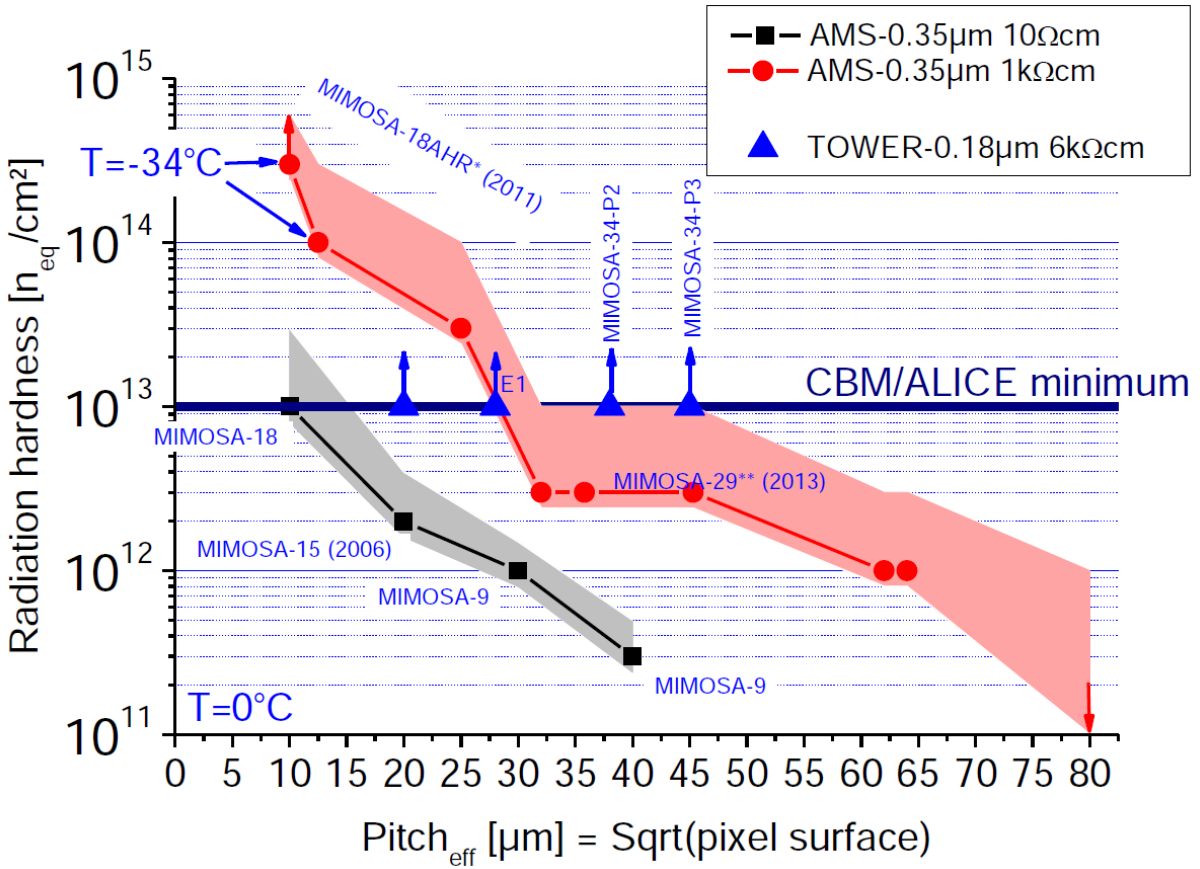

- **Studies of sensing node in 0.18 $\mu m$ process at +20°C :**
  - Pixel gain drops $>$ 5 MRad (threshold shift ?)
    ↪ but SNR seems acceptable up to 10 MRad
  - Well known remedies seem efficient up to $\gtrsim$ 10 MRad :
    short integration time, low temperature, ELT with guard rings
  - Potential conflict : space available in high resolution pixels



# Tolerance to Non-Ionising Radiation

- **Main parametres governing the tolerance to NI radiation :**
  - epitaxial layer : thickness and resistivity
  - sensing node : density, geometry, capacitance, depletion voltage
  - operating temperature
  - read-out integration time

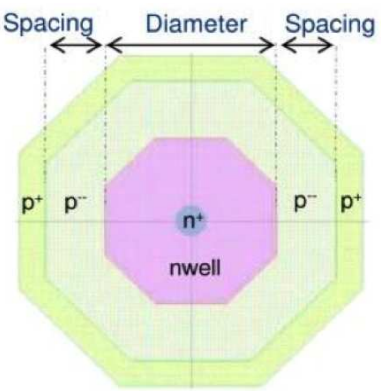
- **Most measurements performed with chips manufactured in two CMOS processes :**
  - 0.35 $\mu m$ with low & high resistivity epitaxy
  - 0.18 $\mu m$ with high & resistivity epitaxy (mainly 18 & 20 $\mu m$ thick)

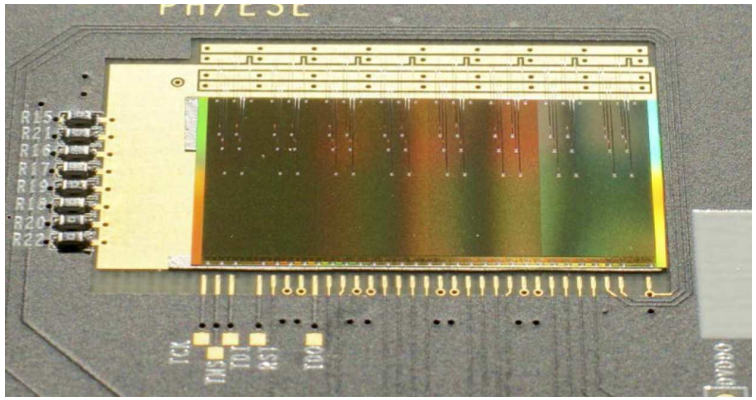


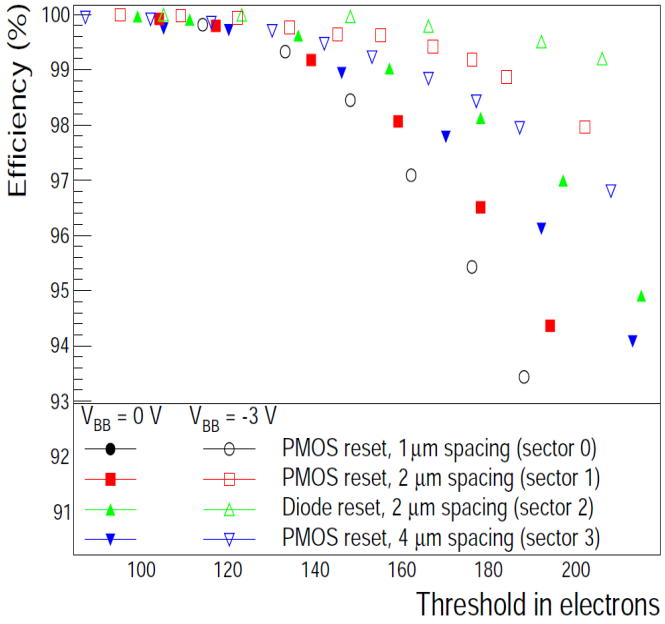

- **Clear improvement with 0.18 $\mu m$ process w.r.t. 0.35 $\mu m$ process**
  - ALICE-ITS requirement seems fulfiled : 2.7 MRad & $1.7 \cdot 10^{13} n_{eq}/cm^2$ at T = +30°C
  - Fluences in excess of $10^{14} n_{eq}/cm^2$ seem within reach
    - $\Rightarrow$ requires global optimisation of design & running parametres

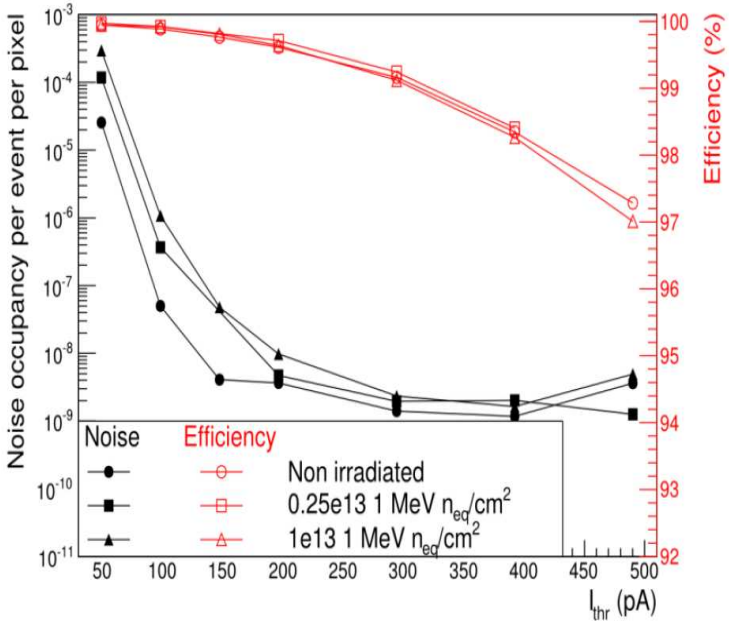
# ALPIDE Detection Performance Assessment

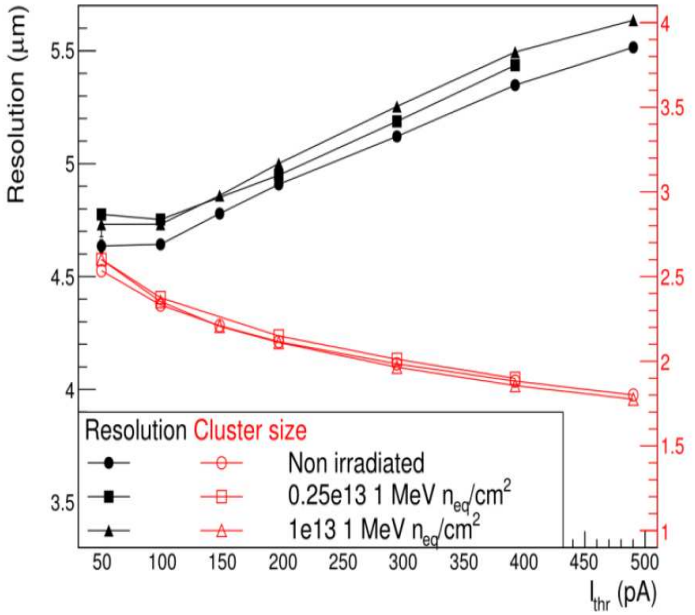
- **ALPIDE-1 beam tests (5–7 GeV pions) :**
  - Final sensor dimensions : 15 mm $\times$ 30 mm
  - About 0.5 M pixels of 28 $\mu m \times 28\ \mu m$
  - 4 different sensing node geometries
  - Possibility to reverse bias the substrate
    - ↪ default : - 3 V
  - Possibility to mask pixels (fake rate mitigation)
    - ↪ default : $\lesssim$ O($10^{-3}$) masked pixels



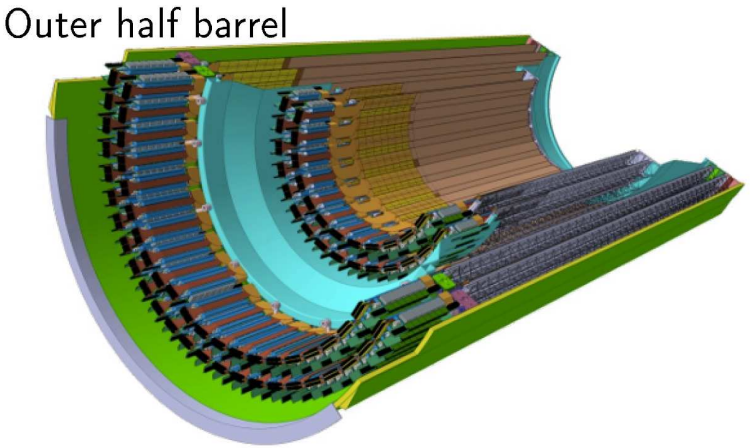


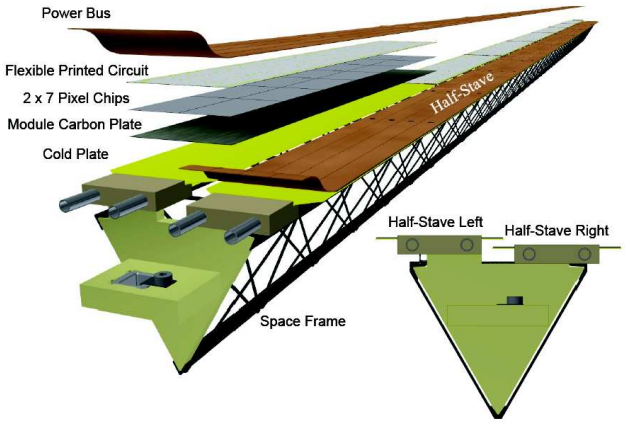



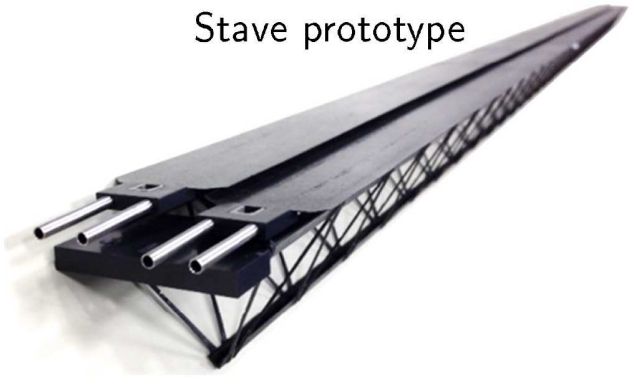
# Extrapolation to ILC Trackers

- ALICE-ITS CONCEPT :
  - Cylindrical geometry based on 7 concentric single-sided layers
  - Outer Barrel (4 layers; 10 $m^2$) serves as a tracker
  - All layers equipped with CMOS Pixel Sensors (CPS)
  - Baseline sensor (ALPIDE) : 5 $\mu m$ & 4 $\mu s$
    (not yet validated on detector ladder)
  - Outer Barrel material budget $\lesssim$ 1% $X_0$/layer
  - Stave length up to $\sim$ 1.5 m

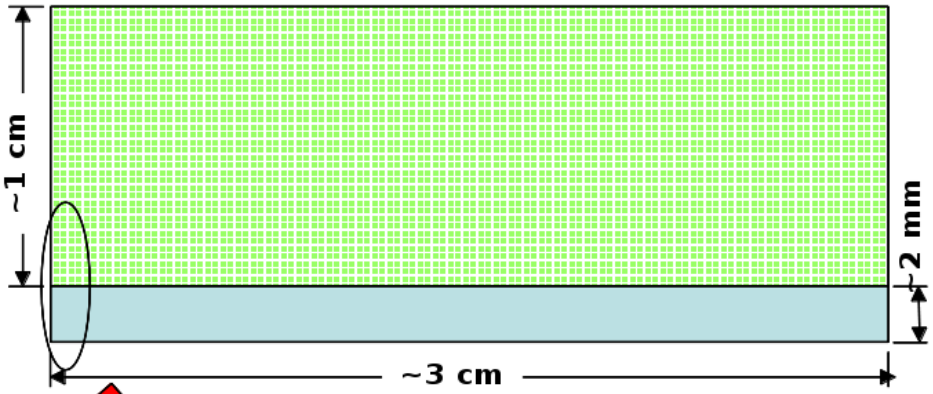



- CPS FOR DOUBLE-SIDED TRACKER LAYERS ACHIEVABLE WITH PRESENT KNOWLEDGE :
  - transposing the ITS concept to an ILC exp.
    allows for 5 $\mu m$ resolution
    and 4 $\mu s$ read-out time
  - alternative : use ITS sensor (5 $\mu m$ & 4 $\mu s$)
    on one ladder side and a faster
    (time stamping) version based on
    elongated pixels on the other side :
    $\sim$ 1 $\mu s$ seems achievable (tbc)

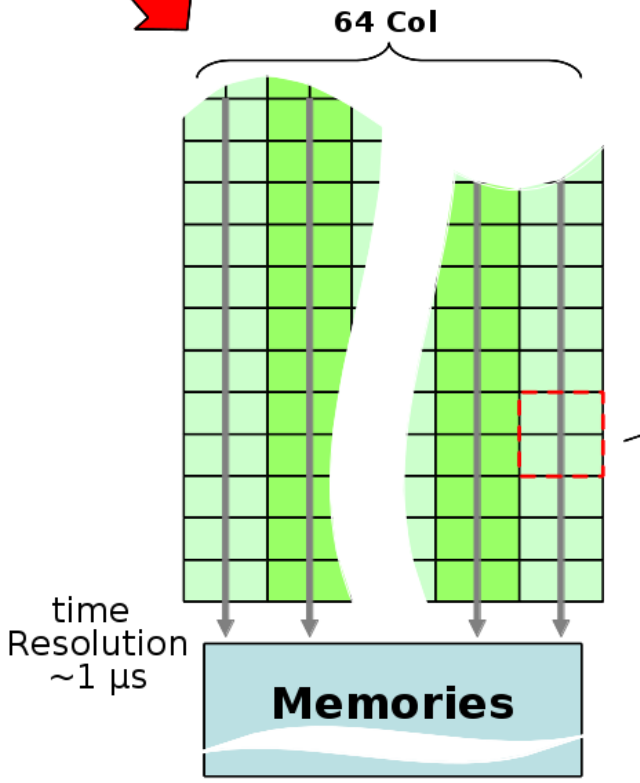


# Noria Based CPS Architecture for (ILC) Single Bunch Identification




- Pixel dimensions ~20x20 µm²
  - $\sigma_{sp}$ ~ 3 µm
- In-pixel amplification-shaping
  - integration time < 1 µs
- In-pixel digitisation
- Organised in N sub-matrices of 64 x 512 pixels




- Data-driven pixel readout in every pair of columns
  - Asynchroneous readout
- Time stamp at the bottom of pixel array within µs
- Hit pixel clusters of each column pair are stored into memories (possibly after cluster selection)
  - Cluster format 2x2 pixels
  - Column address
  - Row address
  - Time stamp (structure)
- Data readout in a few ms after end of train

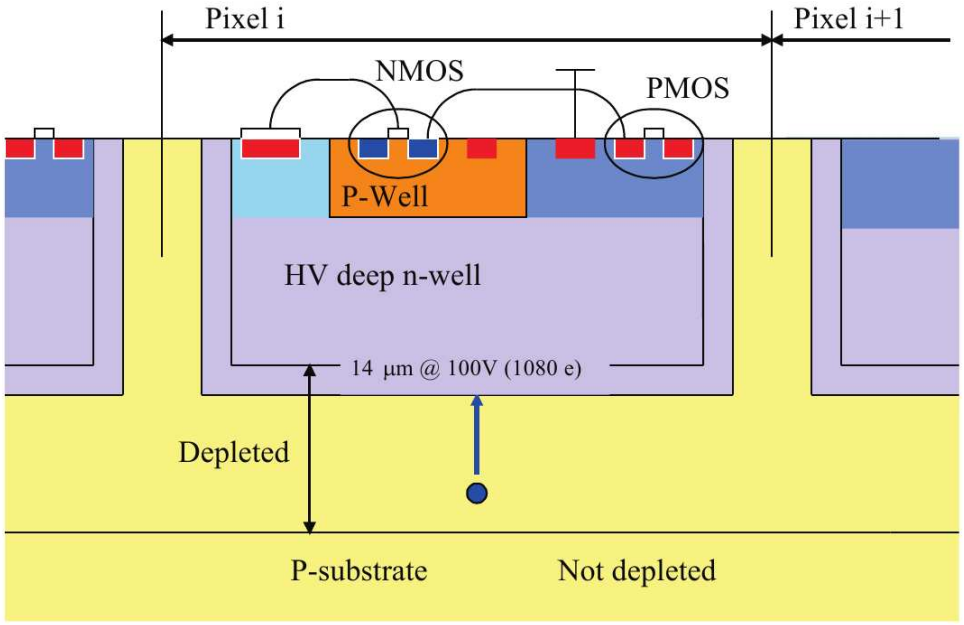
**Still only a concept, not yet a design**

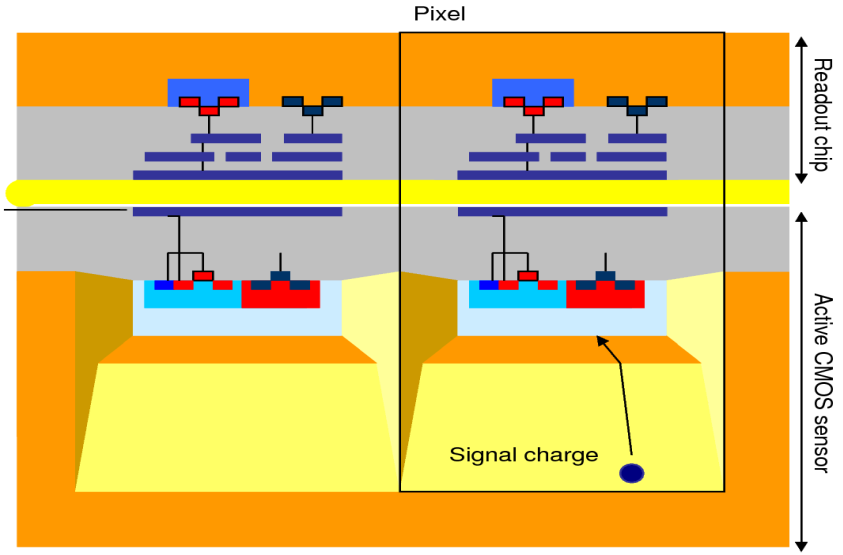
# Further Perspectives of Performance Improvement

- **Expected added value of HV-CMOS :**
  - Benefits from extended sensitive volume depletion :
    - faster charge collection
    - higher radiation tolerance
  - Not bound to CMOS processes using epitaxial wafers

    ⇛ easier access to VDSM ($<$ 100 nm) processes

    ⇛ higher in-pixel micro-circuit density




- **Questions :**
  - minimal pixel dimensions vs $\sigma_{sp} \lesssim 3\ \mu m$ ?
  - uniformity of large pixel array, yield ?

- **Attractive possible evolution : 2-tier chips**
  - signal sensing & processing functionnalities distributed over 2 tiers interconnected at pixel level (capa. coupling)
  - combine 2 different CMOS processes if advantageous : 1 optimal for sensing, 1 optimal for signal processing
  - benefit : small pixel ⟼ resolution, fast response, data compression, robustness ?
  - challenge : interconnection technology (reliability, cost, ...)