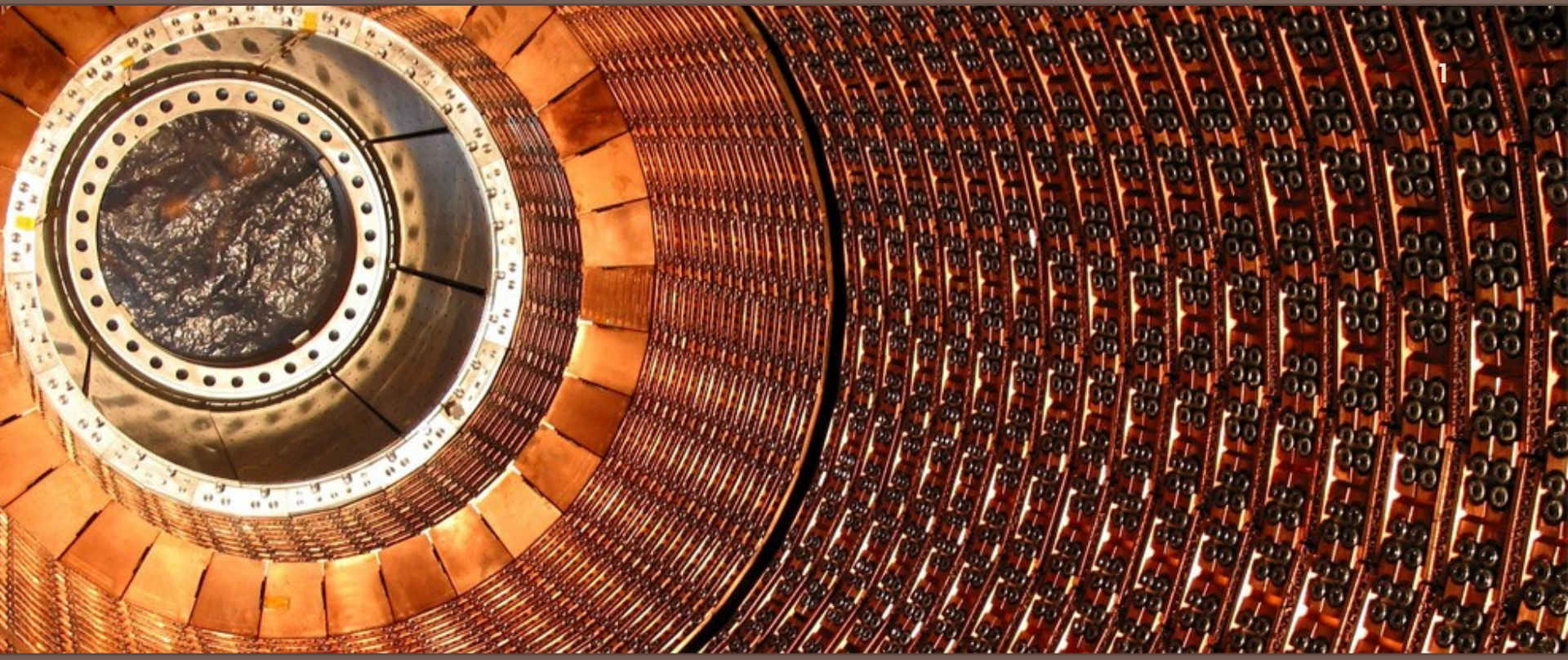
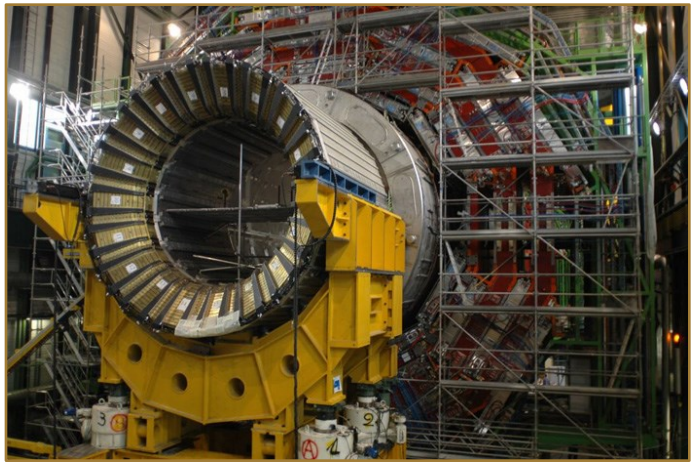


HADRON CALORIMETER BACK-END UPGRADE: DDR3 TO FPGA INTERFACE

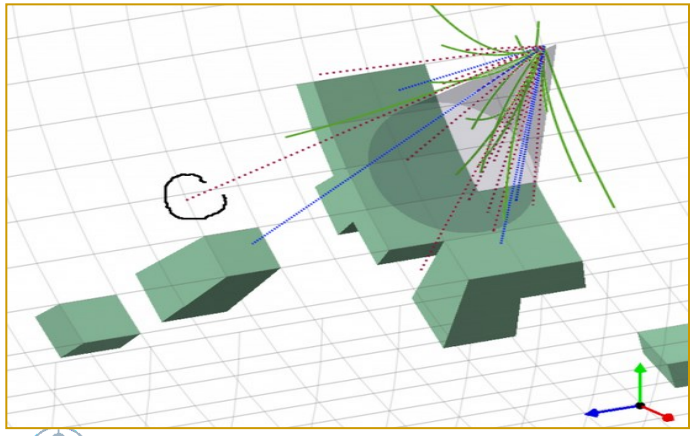
Hui Qing Li
Engineering Physics, University of British Columbia

03.09.2015

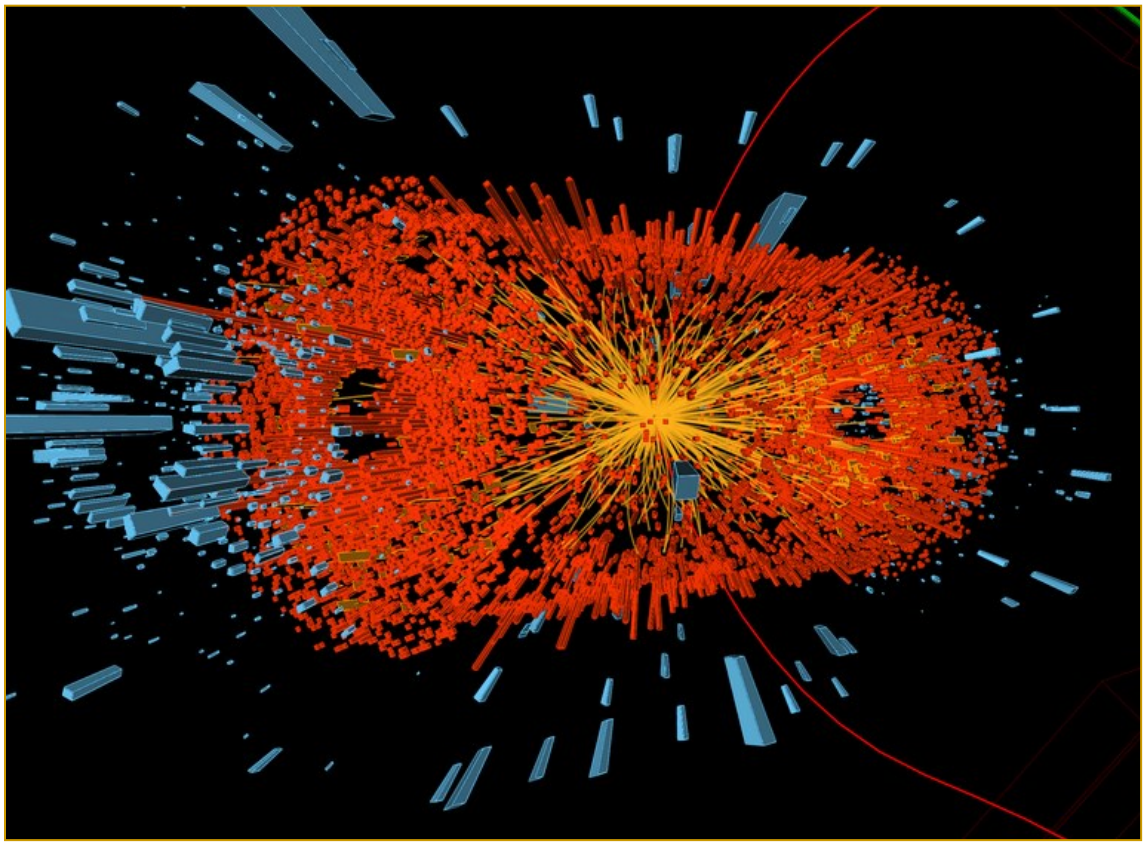
Hadron Calorimeter (Hcal)



Hadron Calorimeter is a part of Compact Muon Solenoid(CMS) inside the **Large Hadron Collider(LHC)**.

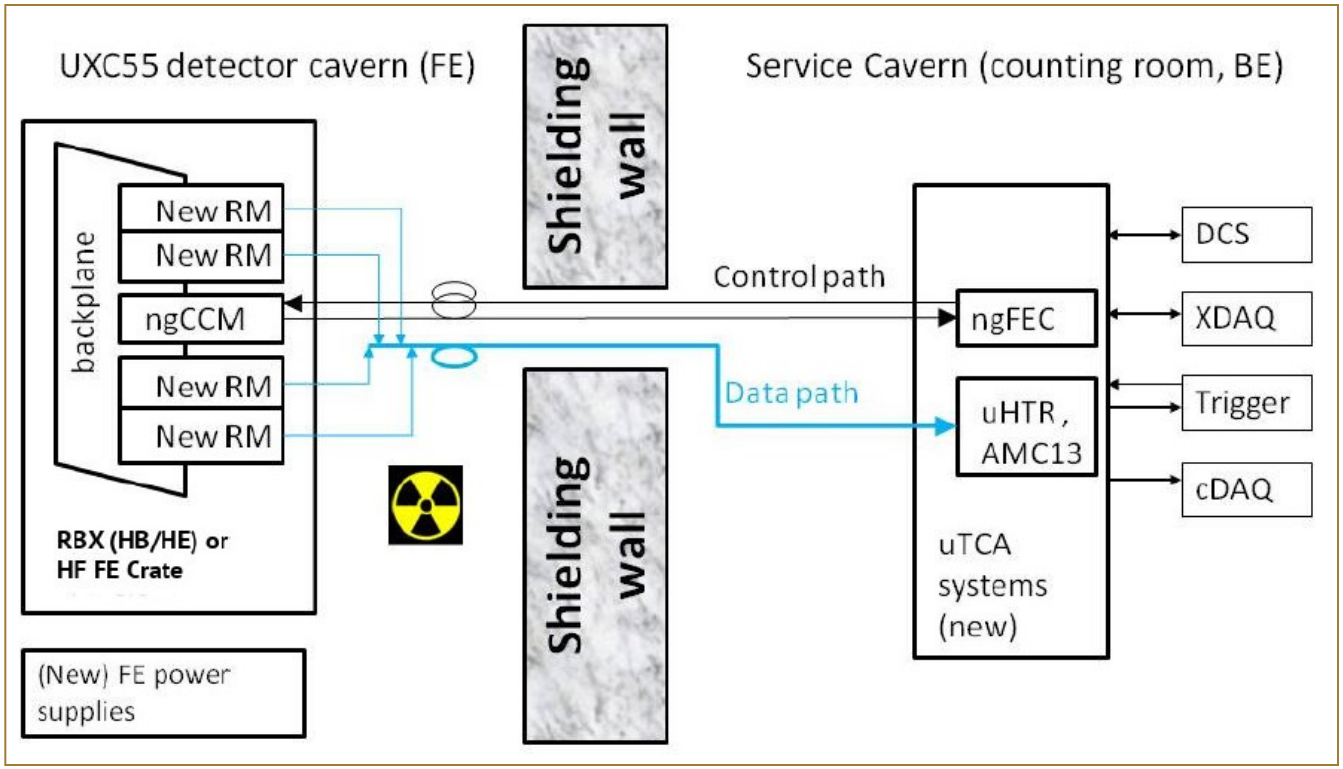


During experiments, a particle collision will produce many jets whose energy will be measured by detector and digitized by a QIE (Charge Integration and Encoder)

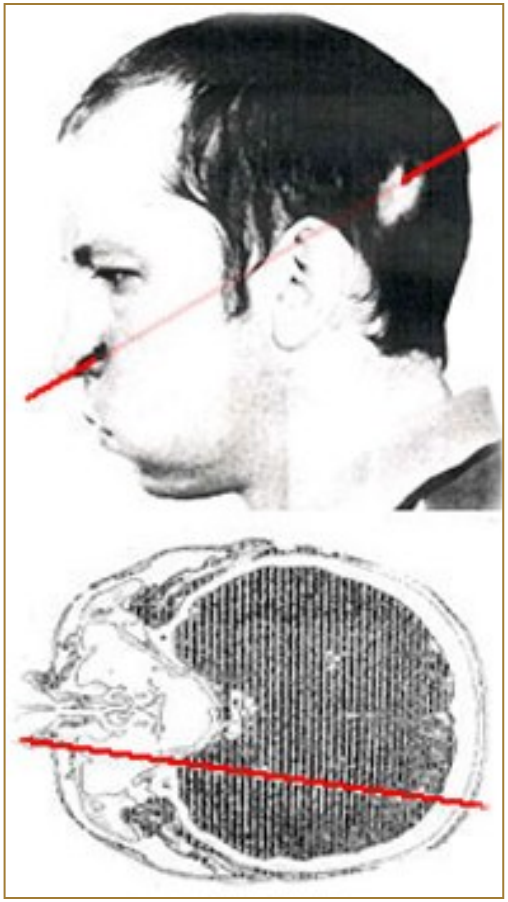


HCal Electronics Upgrade

Detector electronics set up. Back-end allows constant monitoring of QIE and stores control data such as temperature, voltage input, etc.

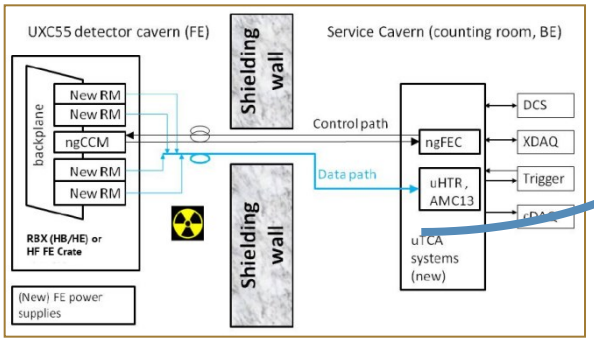


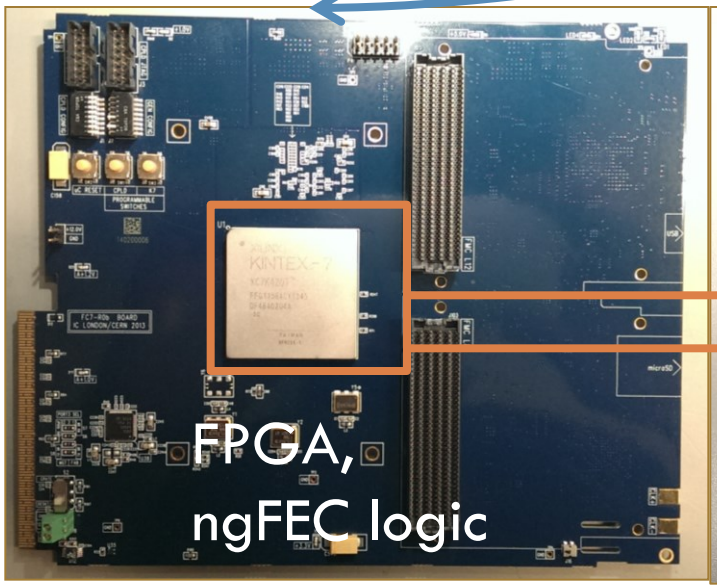
Hcal requires a detector upgrade during the next phase of LHC shutdown. Back End electronics system will upgrade from VMA to microTCA for faster and simpler data buffering.



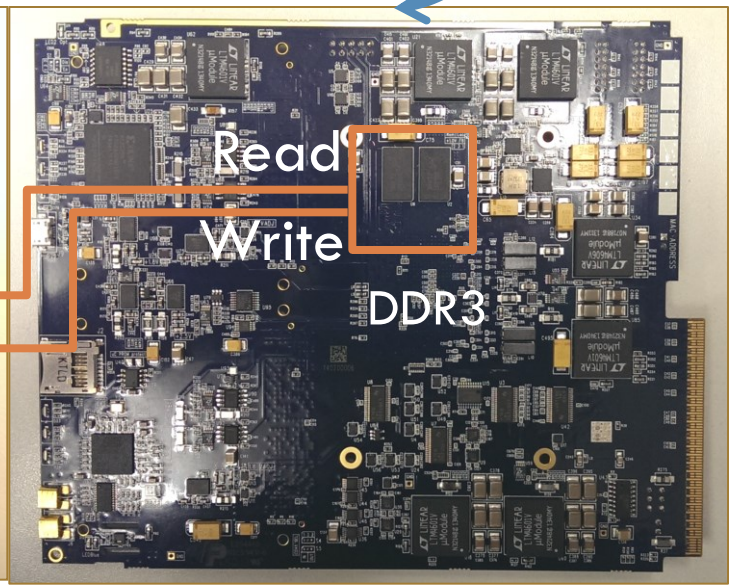
U70 Incident: Anatoli Bugorski was struck by a particle beam. Particle accelerators are dangerous.

Project Goals





KC 7 front



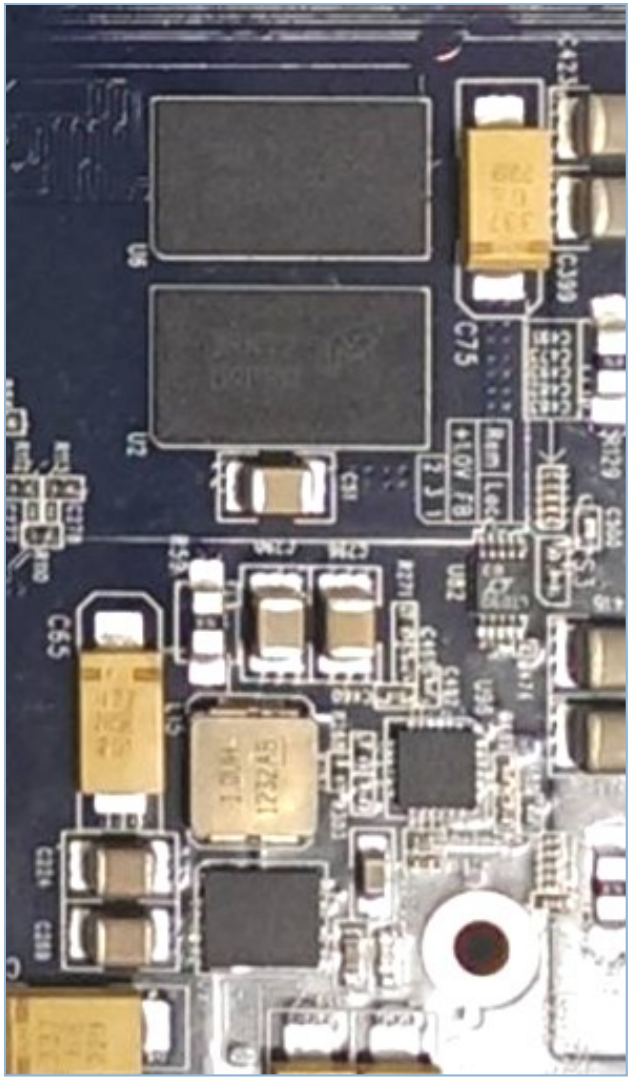
KC 7 back

DDR3:

4Gb storage space
Dual Port
240 MHz system clock
Stores control data from ngCCM via GigaBit Transceiver(GBT)

DDR3- Double Data Rate Type 3

- SDRAM
  - **S**ynchronous
  - **D**ynamic
  - **R**andom **A**ccess **M**emory
  - **D**ouble **R**ate
  - Found in your laptop!



VHDL vs Computer Programming

VHDL

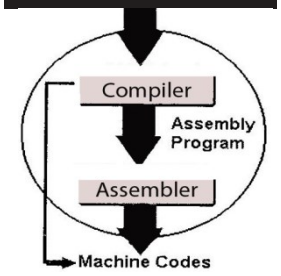
```
5   process(A, B)
6   begin
7       B <= "1";
8       A <= B;
9       B <= "0";
10
11  end process;
```

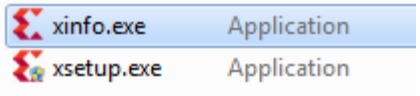
Synthesis

A has value of 0
B has value of 0

C++

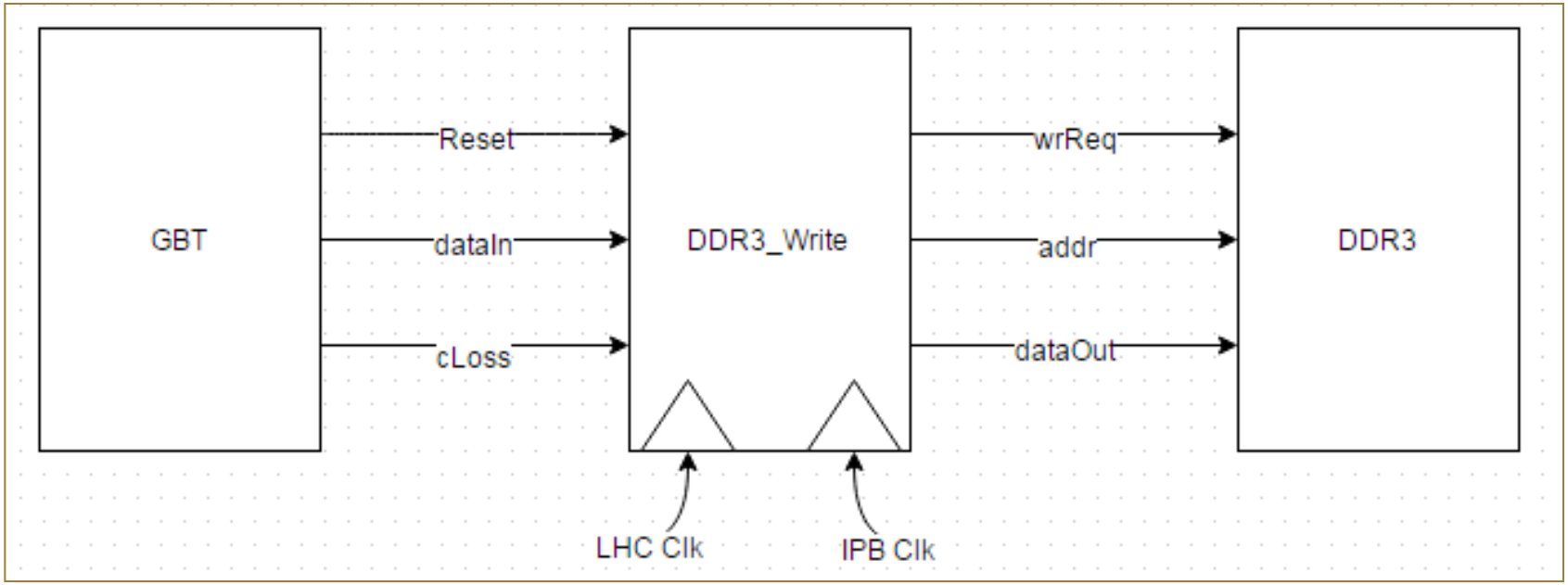
```
int main ()
{
    bool a, b;
    b = true;
    a = b;
    b = false;

    return 0;
}
```





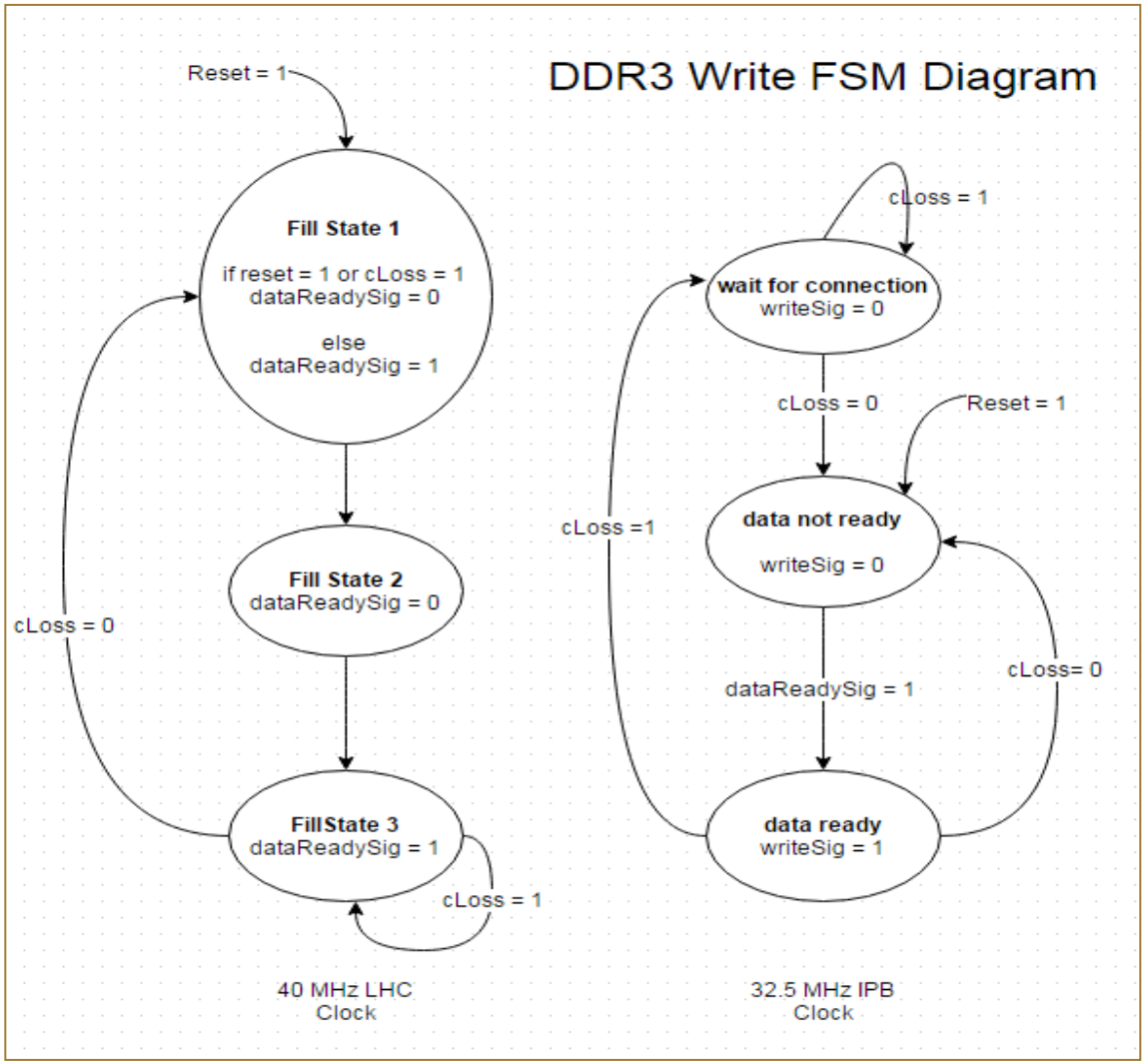
A has value of 1
B has value of 0

Writing Interface

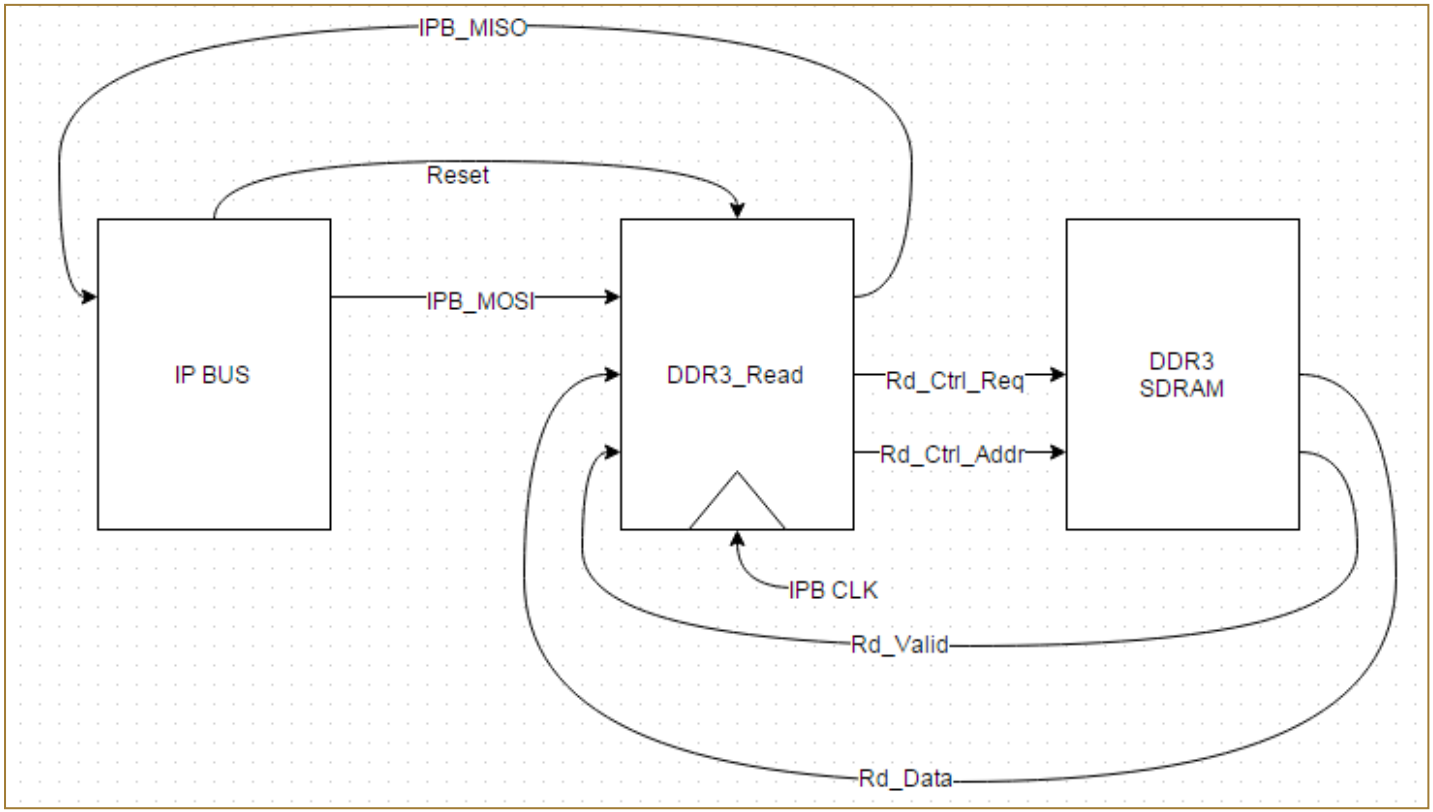


- Writes control data from front-end to DDR3
- Within VHDL:
  - Connects ngCCM_GBT to DDR3_external_interface_wrapper
- ngCCM_GBT: fibres connected to front end detectors
- Continuous writing of front_end control data

Writing Interface

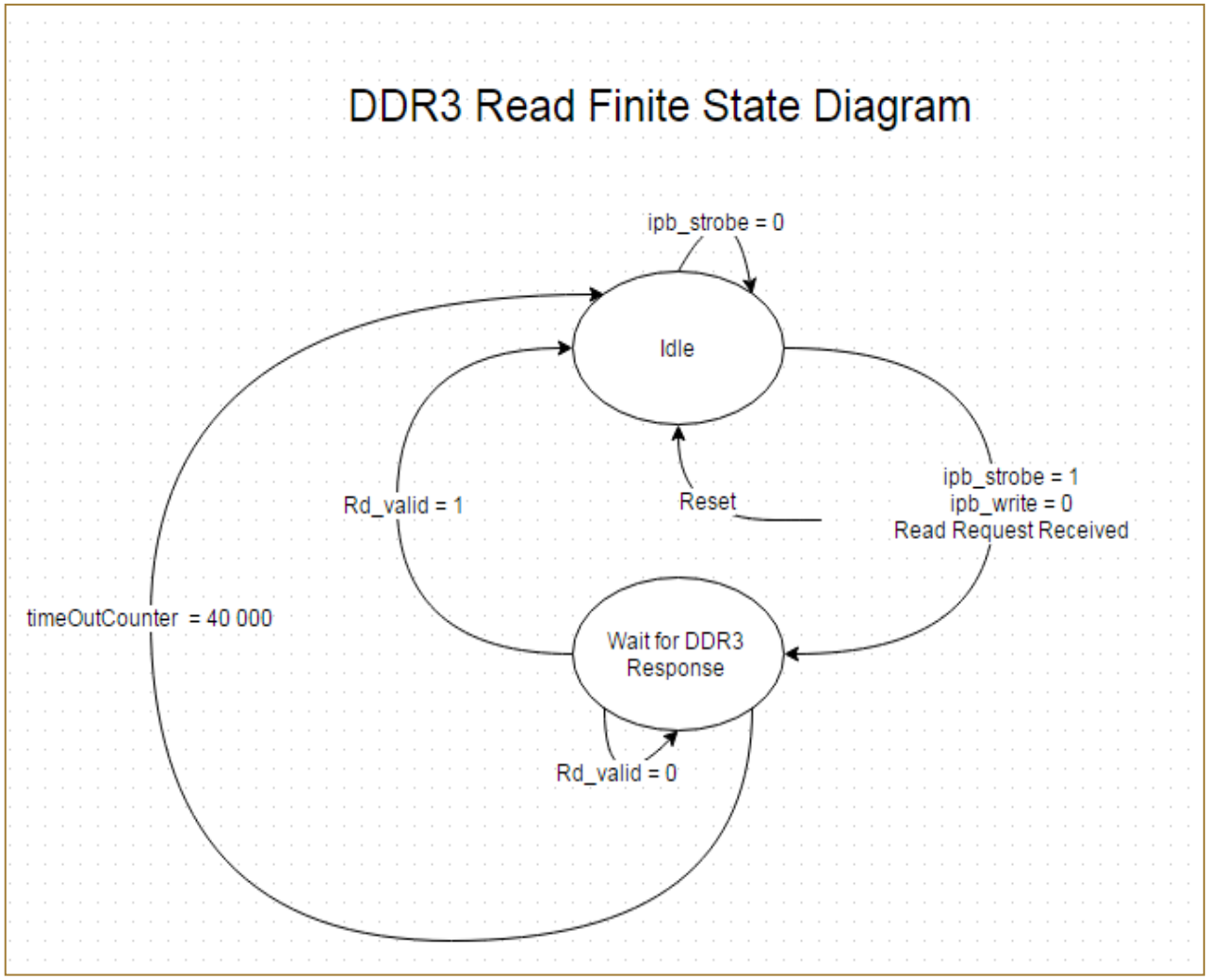


Reading Interface

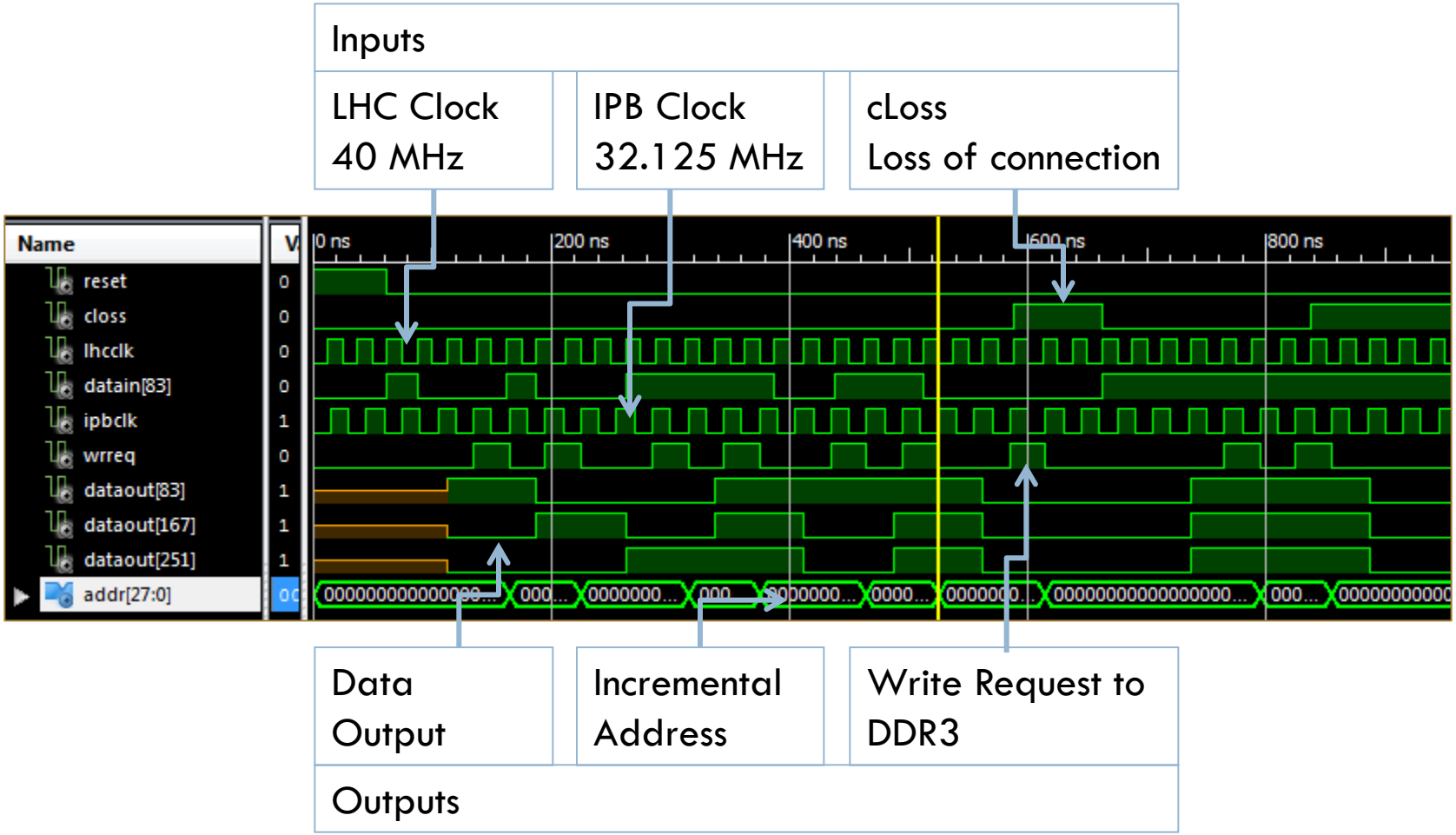


- Software access to stored DDR3 data
- Within VHDL: Connects IP Bus read and write bus structures to DDR3_external_interface_wrapper
- IP Bus: Communication protocol with software connected through ethernet

Reading Interface



Simulation Test: Writing Interface



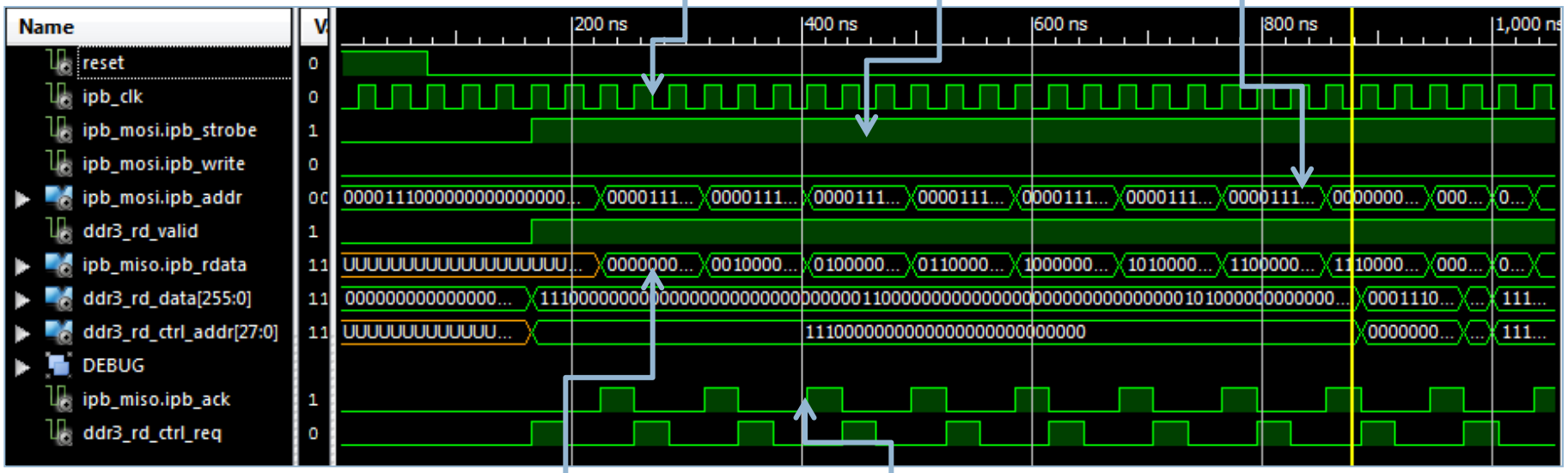
Simulation Test: Reading Interface

Inputs

IPB Clock 32.125 MHz

Reading Request

Software Specified Address



Requested Data

Handshaking Procedure with DDR3

Outputs

Further Work

- Testing DDR3 incorporated firmware on physical hardware
- Requirements:
  - Change test station to use test board
  - Check clock registers for correct frequencies
  - Read DDR3 memory via software

```
Registers
EAX = 00000000 EBX = 7FFDF000
ECX = 00000000 EDX = 00430DA0
ESI = 00000000 EDI = 0012FF80
EIP = 00401062 ESP = 0012FF30
EBP = 0012FF80 EFL = 00000246 CS = 001B
DS = 0023 ES = 0023 SS = 0023 FS = 0038
GS = 0000 OV=0 UP=0 EI=1 PL=0 ZR=1 AC=0
PE=1 CY=0 ST0 = +0.00000000000000000e+0000
ST1 = +0.00000000000000000e+0000
ST2 = +0.00000000000000000e+0000
ST3 = +0.00000000000000000e+0000
ST4 = +0.00000000000000000e+0000
ST5 = +0.00000000000000000e+0000
ST6 = +0.00000000000000000e+0000
ST7 = +0.00000000000000000e+0000
CTRL = 027F STAT = 0000 TAGS = FFFF
EIP = 00000000 CS = 0000 DS = 0000
EDO = 00000000
```

Acknowledgements

These wonderful people…

DESY and CMS

Özgür Şahin

And my awesome supervisor…

danke schön!