Firmware Upgrade Framework for MTCA.4

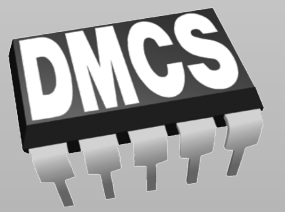
Piotr Perek, Dariusz Makowski [1)]

Łukasz Butkowski [2)]

[1)]Department of Microelectronics and Computer Science
Lodz University of Technology, Poland

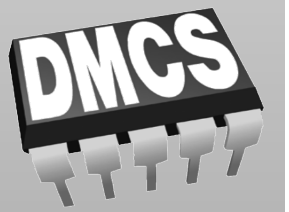
[2)]Deutsches Elektronen-Synchrotron, Hamburg, Germany

4th MicroTCA Workshop for Industry and Research
9-10 December 2015
DESY, Hamburg, Germany



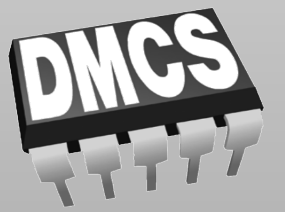
Agenda

1. Introduction
2. Requirements
3. Firmware Upgrade Framework
4. Summary



Programmable devices in MTCA.4

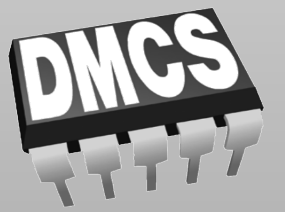
- Module Management Controllers (MMCs)
- Payload devices
  - Field Programmable Gate Arrays (FPGAs)
  - Digital Signal Processors (DSPs)
  - Microcontrollers (MCUs)



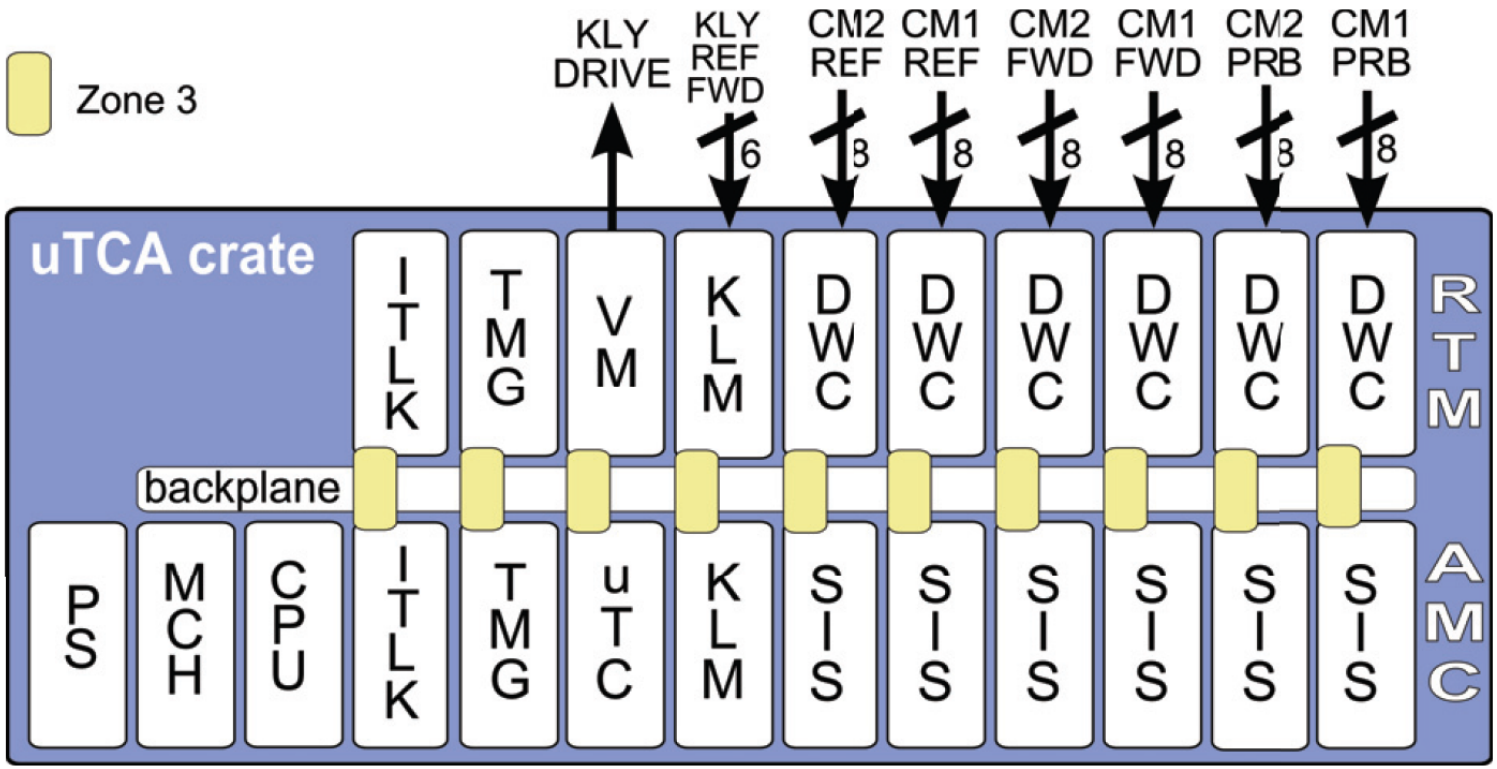
Programmable devices in MTCA.4

- Module Management Controllers (MMCs)
- Payload devices
  - Field Programmable Gate Arrays (FPGAs)
  - Digital Signal Processors (DSPs)
  - Microcontrollers (MCUs)

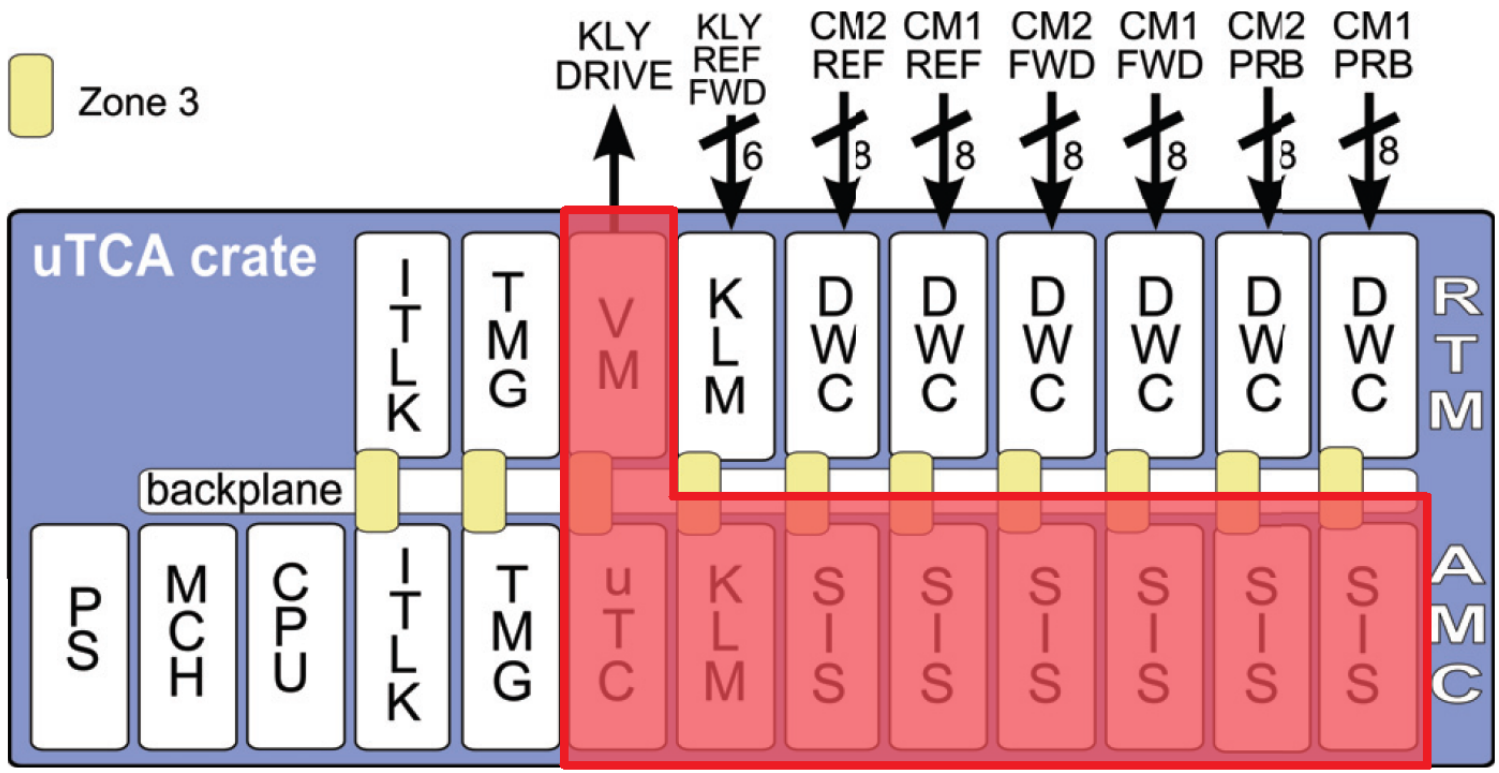
	Memory
Microcontrollers	tens of kB – a few MB
FPGAs	tens of MB
DSPs	a few kB — a few MB



Programmable devices in LLRF system



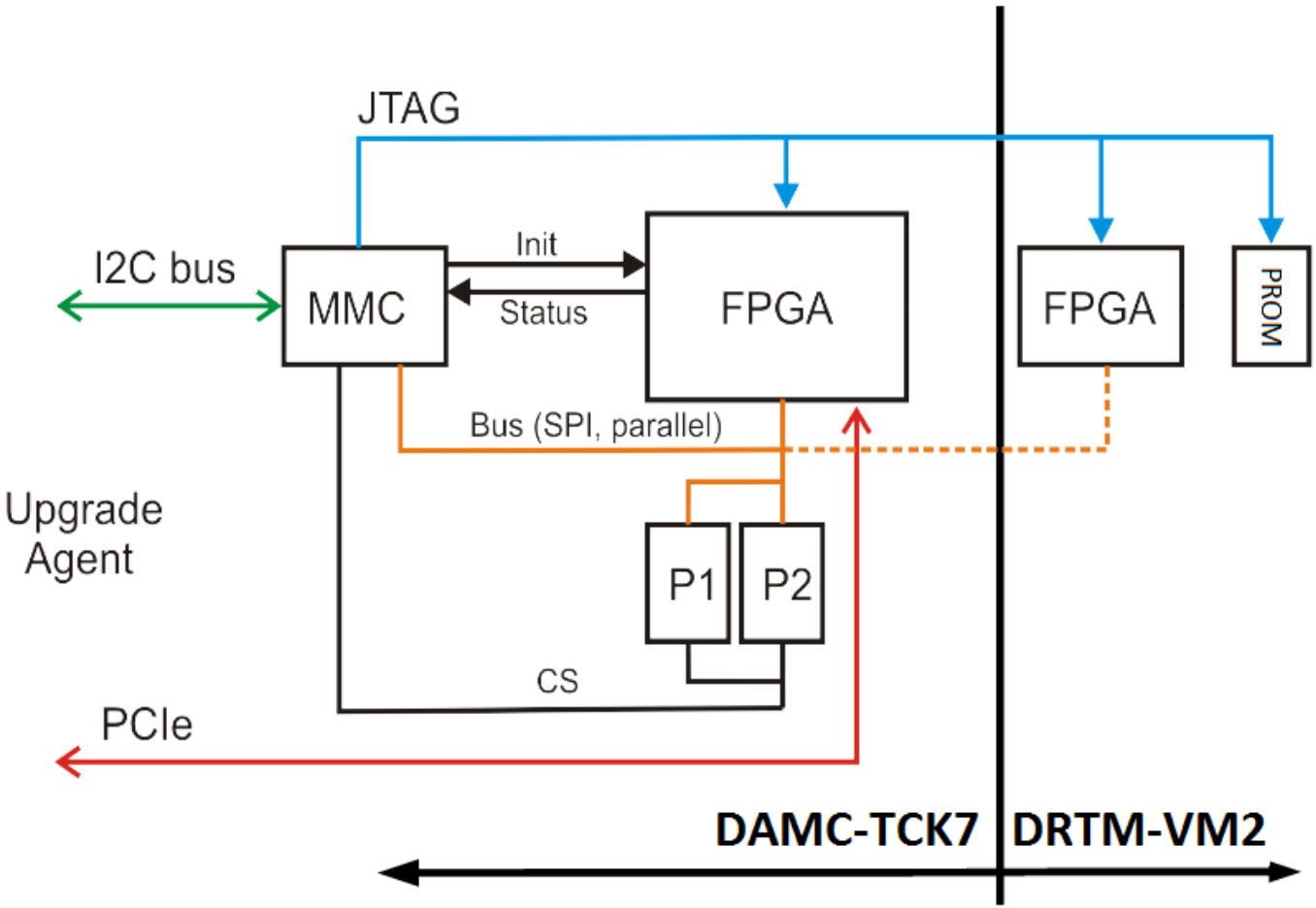
Programmable devices in LLRF system



Number of MTCA.4 crates for LLRF at XFEL – 58
Number of FPGAs for LLRF at XFEL – ∼550

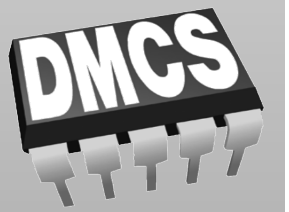
Programmable devices in LLRF system

Programmable devices on DAMC-TCK7 — DRTM-VM2 boards



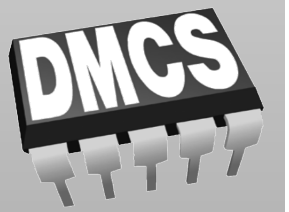
Firmware Upgrade Methods for FPGA

- Dedicated programmers with JTAG interface
- Direct bitstream upload
- Indirect programming
- HPM.1 firmware upgrade
- JTAG switch module (NAT)



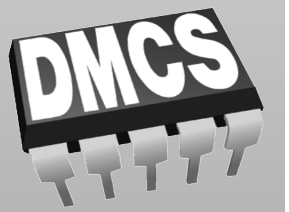
Requirements

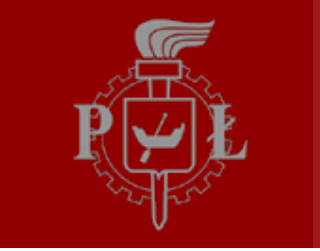
- Universal framework for remote memory programming
- Support for both SPI and Platform FLASH memories
- Support for all modules used in LLRF system:
  - DAMC-TCK7
  - VM
  - SIS8300L
- Programming interface - PCIe



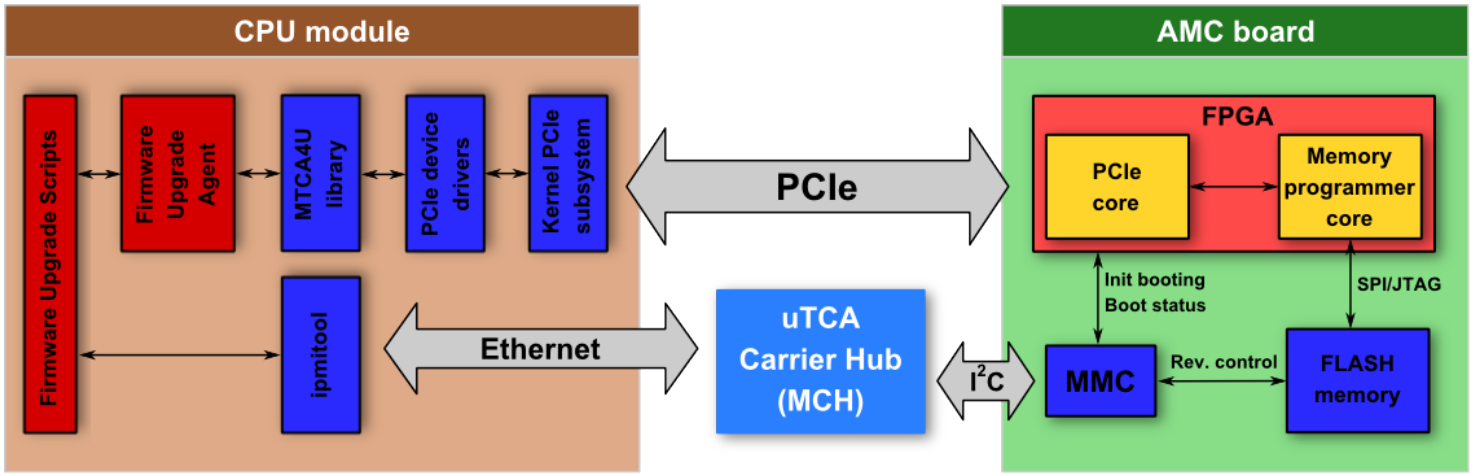
Framework Components

- Firmware
  - Memory programming core
    – *provides PCIe interface to access and program an on-board memory*
- Software
  - Firmware Upgrade Agent
    – *implements algorithms ensuring an execution of the firmware upgrade procedure for SPI and Platform FLASH memories*
  - Firmware Upgrade Scripts
    – *supporting scripts for board-specific operations e.g. memory/revision selection, FPGA reloading etc.*



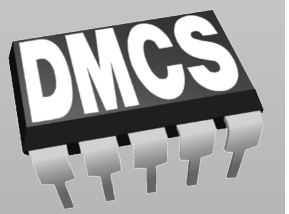


Framework Structure

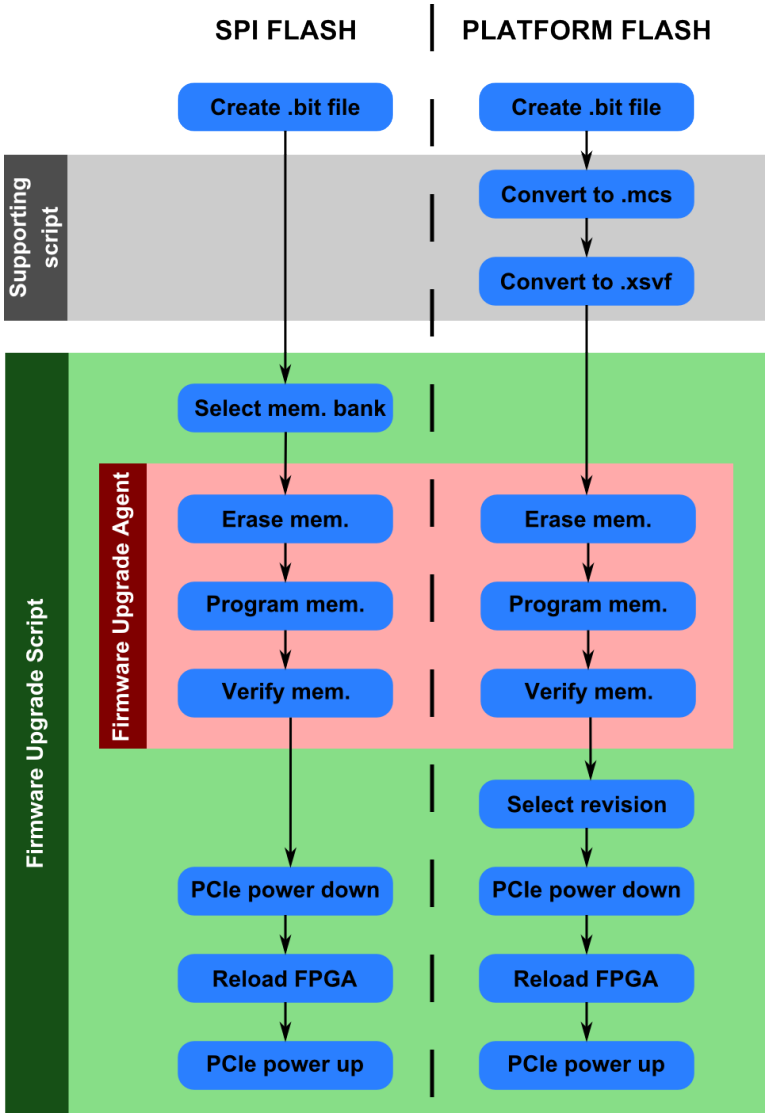


FPGA resources utilization (Spartan6 xc6slx45t):

- Slice Registers – 390/54576 (0.7%)
- Slice LUTs – 401/27288 (1.5%)



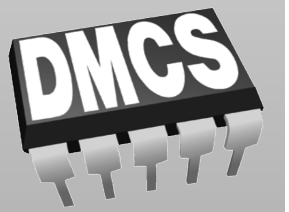
Firmware Upgrade Procedure



Tests

Framework has been tested with the following modules:

- DAMC-TCK7 (CM045)
- uTC
- SIS8300L
- FMC20
- DRTM-VM2



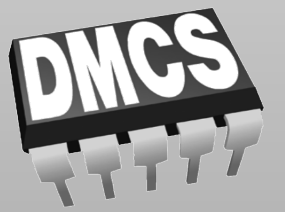
Tests

Framework has been tested with the following modules:

- DAMC-TCK7 (CM045)
- uTC
- SIS8300L
- FMC20
- DRTM-VM2

Time required for memory reprogramming:

	FUF	**Xilinx programmer**
DAMC-TCK7 (SPI)	70 s	1800 s
SIS8300L (SPI)	60 s	450 s
DRTM-VM2 (JTAG)	230 s	100 s



Summary

- Firmware Upgrade Framework – allows reprogramming of all LLRF system modules in an unified way
- Allows remote, parallel programming of SPI and Platform FLASH memories
- Working on various FPGA devices
  – Spartan 6 (FMC20), Virtex 6 (SIS8300L), Kintex 7 (DAMC-TCK7)
- Can be easily adapted to other FPGAs and MTCA.4 modules
- Programming time for SPI memories much faster than with standard JTAG programmer