All programmable:

Current development and future trends in the world of FPGAs

Michael Oelmann

Agenda

- Mission
- Market Trends
- Business & Roll-Out Status Update

Xilinx – The All Programmable Company

XILINX
ALL PROGRAMMABLE™

XILINX - Founded 1984

- Headquarters
- Research and Development
- Sales and Support
- Manufacturing

$2.38B FY15 revenue

>55% market segment share

3,500+ employees worldwide

20,000 customers worldwide

3,500+ patents

60 industry firsts

Market Segment Share Leadership

Xilinx Market Segment Share Total

FY11: **53%**		FY15: **56%**	
High-End:	60%	High-End:	60%
Mid-Range:	1%	Mid-Range:	54%
Low-End:	40%	Low-End:	51%

Xilinx Market Segment Share in Advanced Nodes

28nm	20nm
FY15: **62%**	FY15: **70%**

Note: All numbers derived from Altera and Xilinx Only
Source: Public Reports and Xilinx Estimates

Expanding the Scope of our Business

ALL PROGRAMMABLE

ALL Programmable Technologies – HW, SW, I/O

ALL Programmable Devices – FPGA, SoC, 3D IC

ALL Programming Models – RTL and SW Defined

Enabling ALL Programmable Electronic Systems and Networks

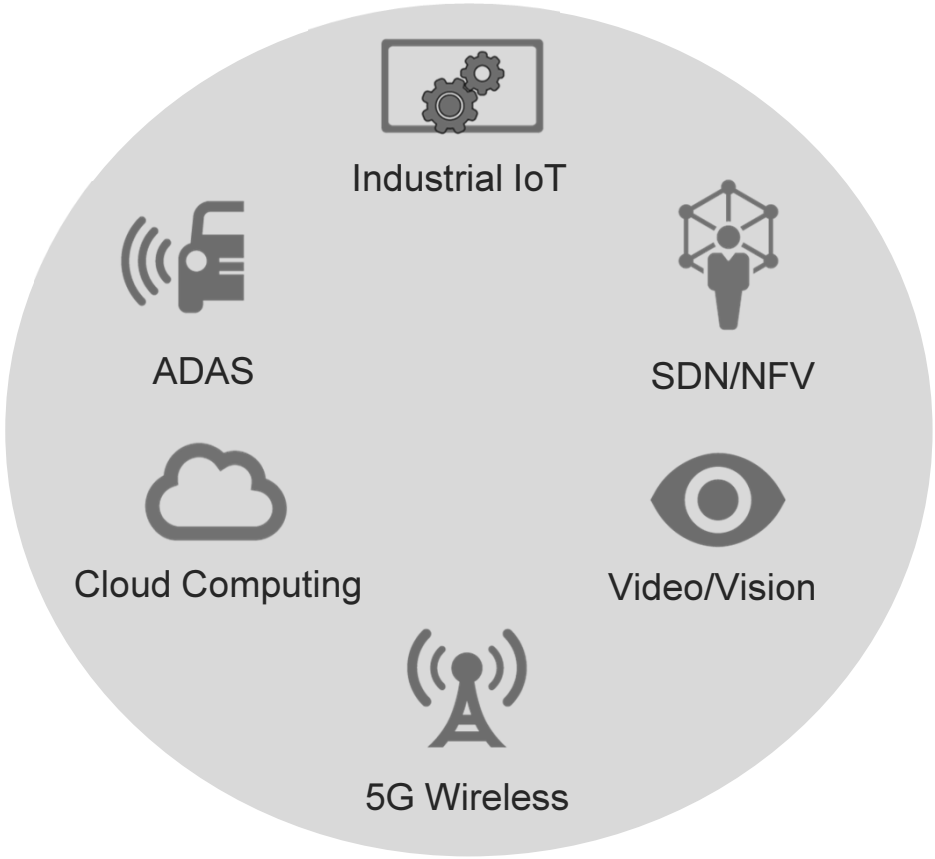
Requirements for Megatrends

XILINX ENABLED

ALL PROGRAMMABLE

Next Gen Requirements

- Connected
- Secure & Safe
- Software Defined
- Virtualized
- Analytics
- Video Everywhere
- Multi-Processing
- Scalable Acceleration



A New Era of All Programmable Solutions

ALL PROGRAMMABLE

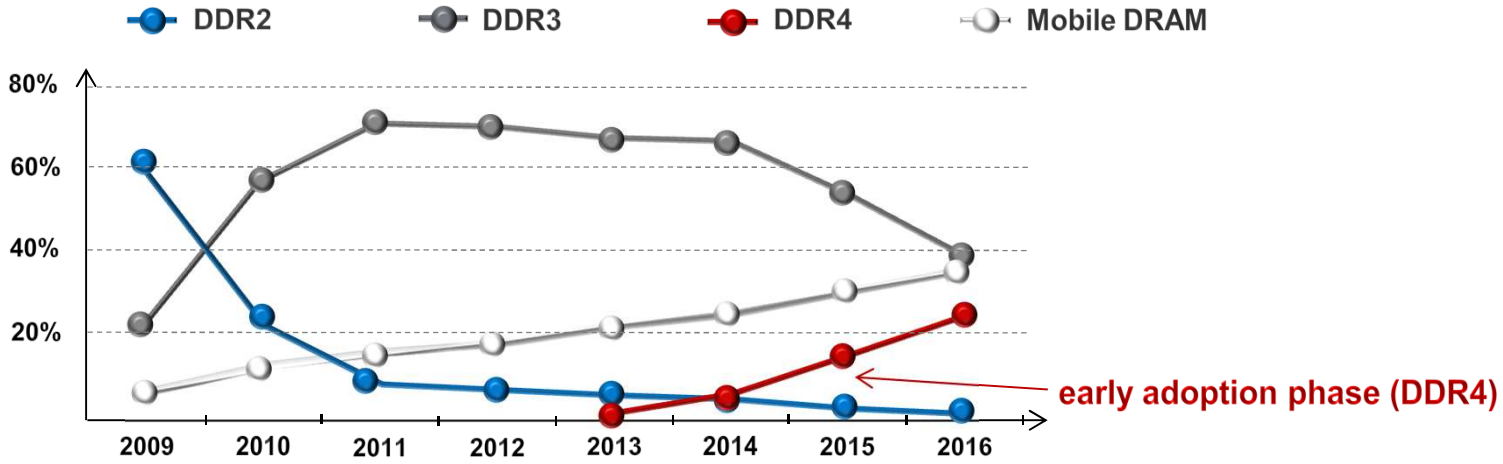
Next Gen Requirements	ALL Programmable Solutions
Connected	Any-to-Any Connectivity
Secure & Safe	Multi-Level Security/Safety
Software Defined	SDNet Environment
Virtualized	SDAccel Environment
Analytics	SDSoC Environment
Video Everywhere	Video IP
Multi-Processing	Zynq MPSoC
Scalable Acceleration	UltraScale

Trends

- Memory
- Transceiver
- PCB
- SoC
- Development Technologies

DRAM Memory Trends: Low Power and Greater Bandwidth…*And What it Means for FPGAs*

- **Low Power: Mobile DRAM (LPDDRx) experiencing rapid adoption**
  - Becoming mainstream with proliferation of tablets and smart phones
  - Proportion of PC DRAM is declining in comparison
  - Currently not dominant w/FPGAs (used in hand held defense, consumer)
- **High Bandwidth: DDR4 adoption will first be driven by server market**
  - Set for adoption in certain high performance FPGA markets
  - DDR4 the last in the series, no sign of DDR5 yet
  - ***Not scaling*** for ultra-high bandwidth applications (e.g., 400G applications)

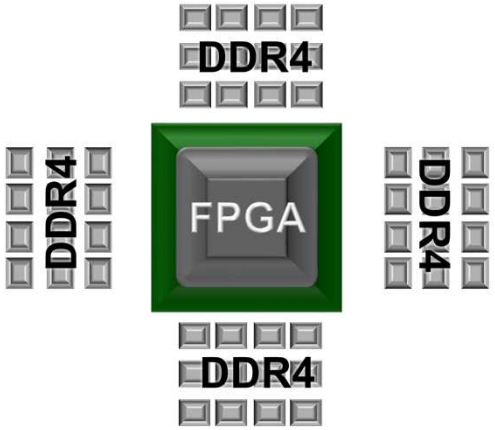


Source: Industry Research

Parallel Memory Struggling to Meet Ultra-High Bandwidth Demand: Motivation for Serial Memory

- **Parallel data rates are not increasing as fast as transceiver line rates**
  - Signal integrity challenges at higher line rates
- **Wider parallel I/O solutions lead to board design and packaging challenges**

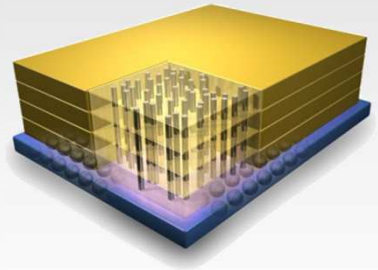
400 Gb/s Packet Buffer Example
(Requires 48 devices; 1,248 FPGA I/Os)



- FPGA pin limitation
- Increased board space
- More complexity

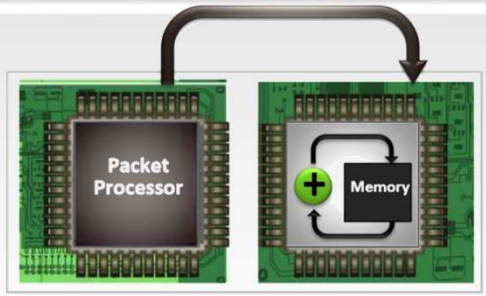
Transceivers provide the bandwidth and pin efficiency for next generation memory technology

Going Serial: Serial Memory Entering the Market



Hybrid Memory Cube (HMC)
by Micron

- **Stacked DRAM, replaces DDR**
- **High bandwidth for packet buffering**
- **Gen2 (10G, 12.5G, 15G) sampling now**
- **Gen3 (15G, 30G) in 2015**



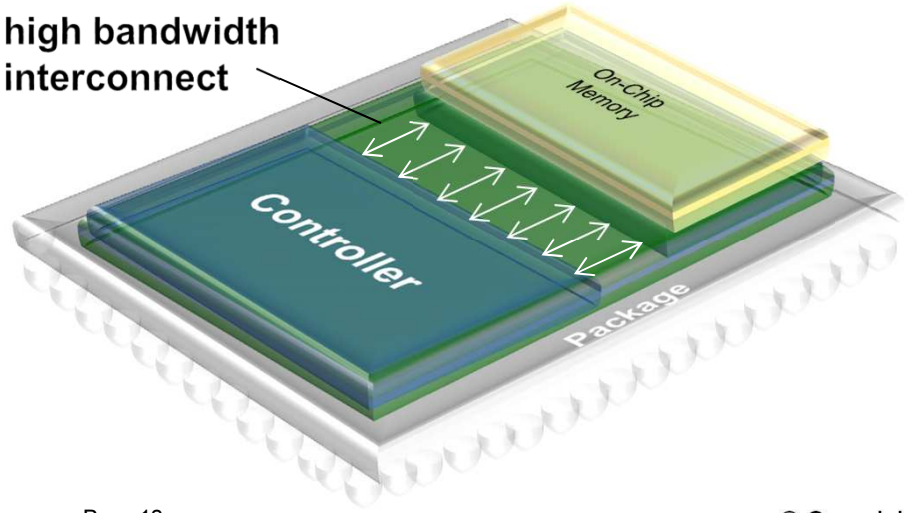
Bandwidth Engine
by MoSys

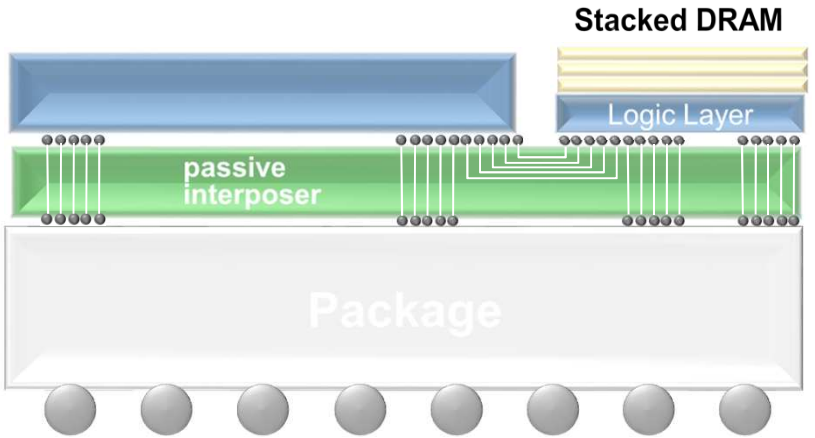
- **1T-SRAM-based, replaces QDR/RLDRAM**
- **High transaction rates for control functions**
- **Supports 10G, 12.5G, 14G, 15.6G**
- **Available now**

Emerging Technology: On-Package 3D IC

High Bandwidth at Lower Power

- **Memory die inside package with massively parallel connections**
- **High Bandwidth Memory (HBM) defined by JEDEC**
- **Offers high bandwidth *at low power* (limited I/O power consumption)**
- **Dependent on cooperation between companies for integration**

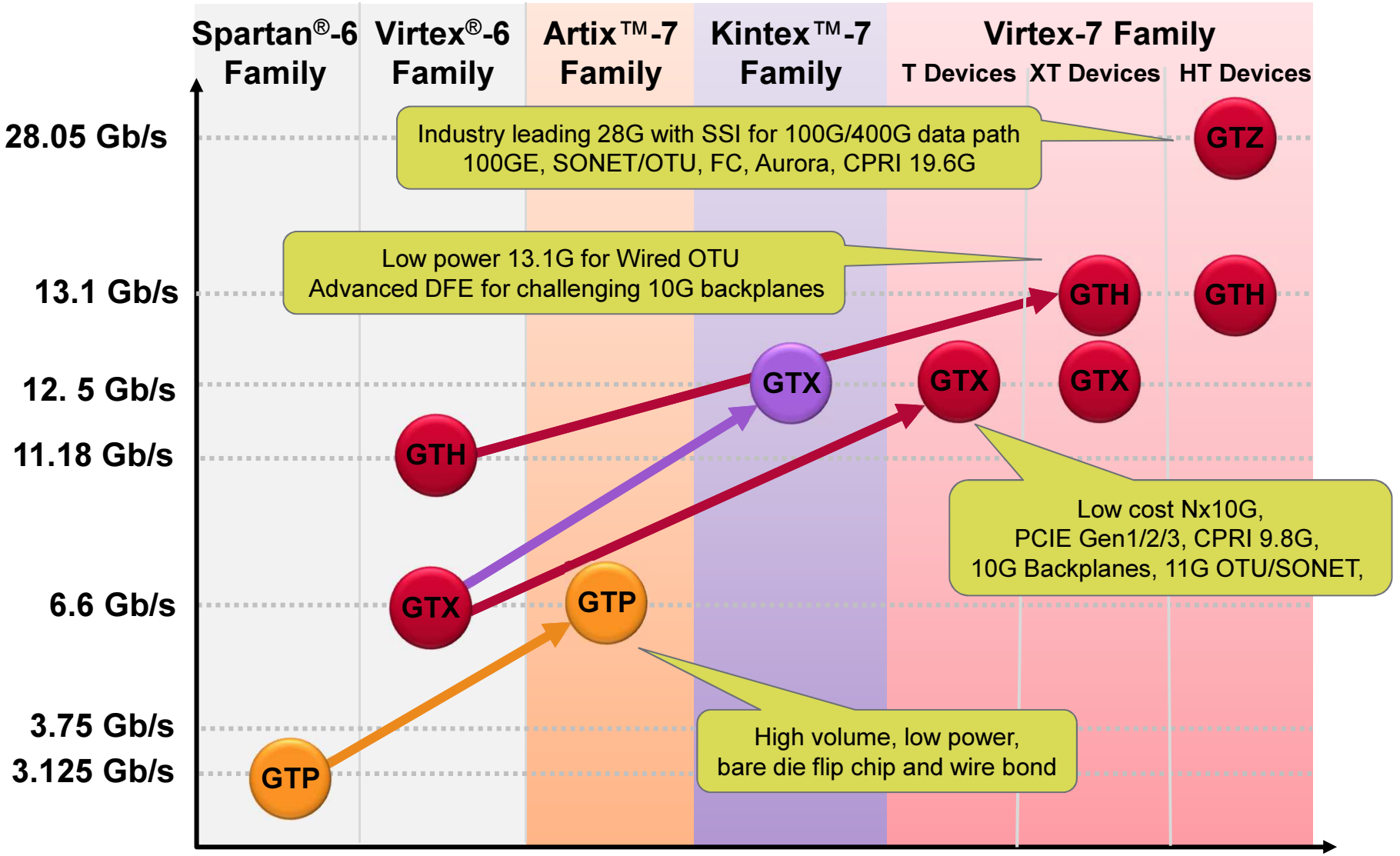




Trends

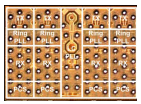
- Memory
- Transceiver
- PCB
- SoC
- Development Technologies

7 Series Transceiver Roadmap - 40nm => 28nm



Xilinx Transceivers since 2010

7 Series 28nm GTX (12.5Gb/s)



A Wide Common-Mode Fully-Adaptive Multi-Standard 12.5Gb/s Backplane Transceiver in 28nm CMOS

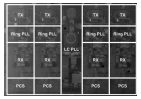
Jafar Savoj, Kenny Hsieh, Parag Upadhyaya, Fu-Tai An, Ade Bekele, Stanley Chen, Xuewen Jiang, Kang Wei Lai, Chi Fung Poon, Aman Sewani, Didem Turker, Karthik Venna, Daniel Wu, Bruce Xu, Elad Alon*, Ken Chang
Xilinx, Inc., San Jose, CA, *U.C. Berkeley, Berkeley, CA

Abstract—This paper describes th… upport a wide frequency range and

2012 VLSI circuit symposium

7 Series 28nm GTH (13.1Gb/s)

- PCIe Gen3 and 10G KR Compliant

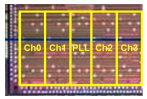


Design of High-Speed Wireline Transceivers for Backplane Communications in 28nm CMOS

Jafar Savoj, Kenny Hsieh, Parag Upadhyaya, Fu-Tai An, Jay Im, Xuewen Jiang, Jalil Kamali, Kang Wei Lai, Daniel Wu, Elad Alon*, Ken Chang
Xilinx, Inc., San Jose, CA, *U.C. Berkeley, Berkeley, CA

2012 Custom Circuits Integrated Conference

7 Series 28nm GTP (6.6Gb/s)



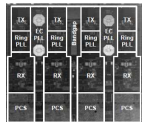
A Low-Power 6.6-Gb/s Wireline Transceiver for Low-Cost FPGAs in 28nm CMOS

Jafar Savoj, Kenny Hsieh, Fu-Tai An, Michael Buckley, Jay Im, Xuewen Jiang, Anup Jose, Vassili Kireev, Kang Wei Lai, Hien Pham, Didem Turker, Daniel Wu, Ken Chang

2012 Asian Solid-States Circuits Conference
Invited to JSSC

UltraScale 20nm GTH (16.3Gb/s)

- PCIe Gen3 and 10G KR Compliant



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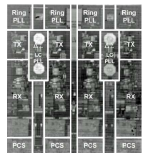
Xilinx, Inc., San Jose, CA, *U.C. Berkeley, Berkeley, CA

2014 Custom Circuits Integrated Conference
Invited to JSSC

UltraScale 20nm GTY (32G)

- 28G backplane capable



3.3 A 0.5-to-32.75Gb/s Flexible-Reach Wireline Transceiver in 20nm CMOS

Parag Upadhyaya, Jafar Savoj, Fu-Tai An, Ade Bekele, Anup Jose, Bruce Xu, Daniel Wu, Didem Turker, Hesam Aslanzadeh, Hiva Hedayati, Jay Im, Siok-Wei Lim, Stanley Chen, Toan Pham, Yohan Frans, Ken Chang

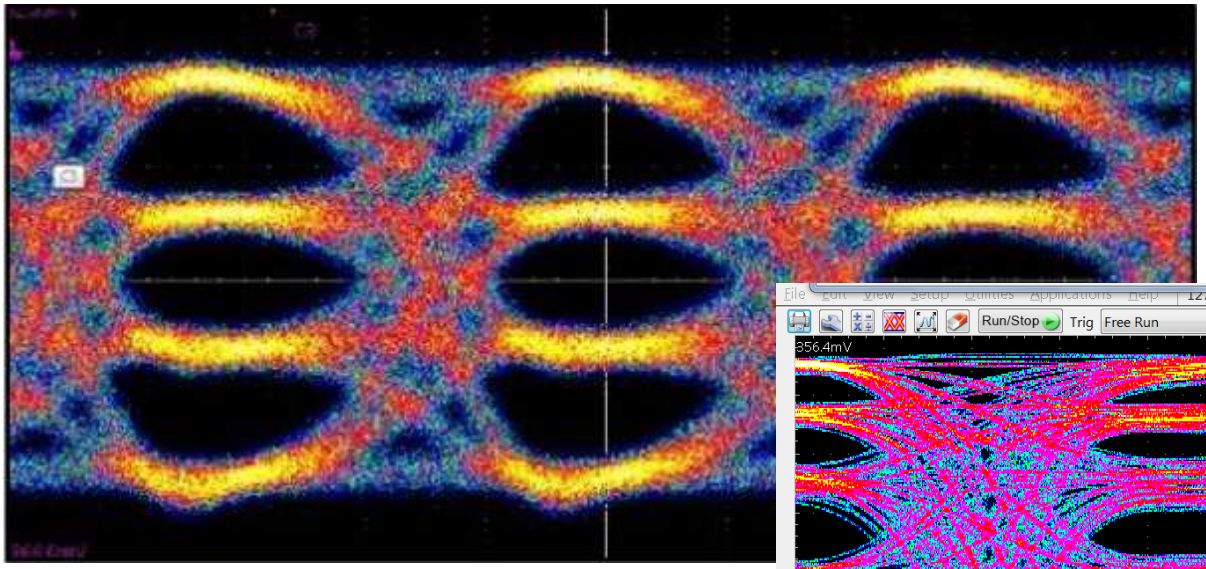
Xilinx, San Jose, CA

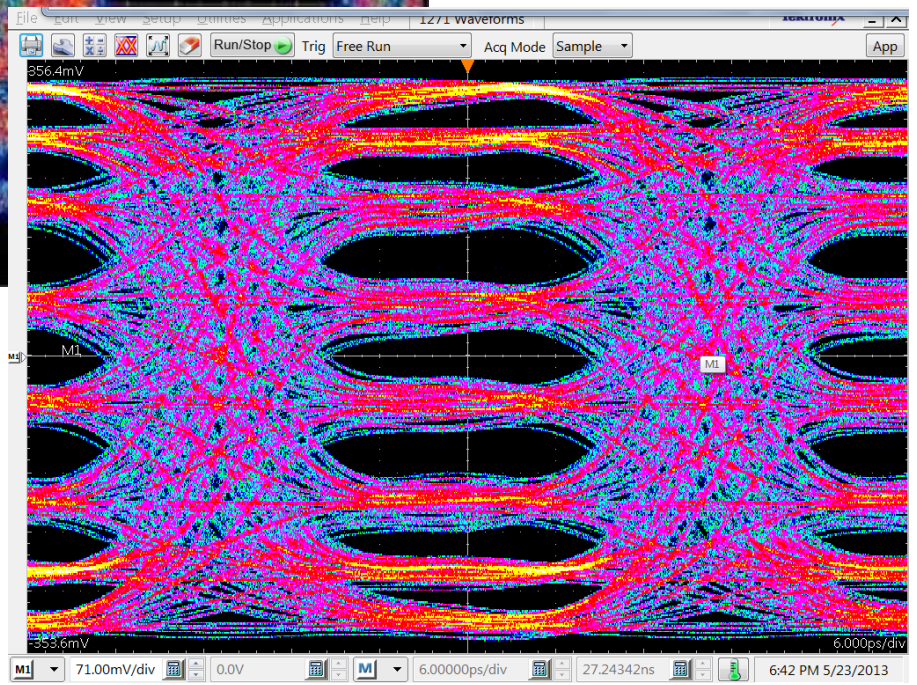
2015 International Solid-States Circuits Conference

2 transceivers in UltraScale+ 16nm FinFet

- GTH (16.3G): T/O in June 2015
- GTY (32G): T/O in Oct 2015

What's coming next: PAM4, PAM8, etc.





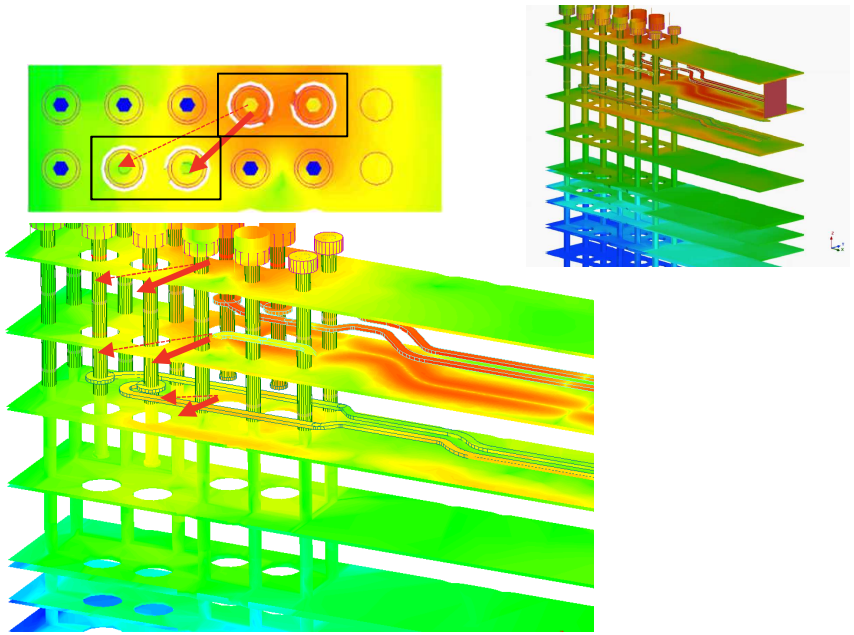
Stop increasing frequency,
Increase number of signal levels!

Trends

- Memory
- Transceiver
- PCB
- SoC
- Development Technologies

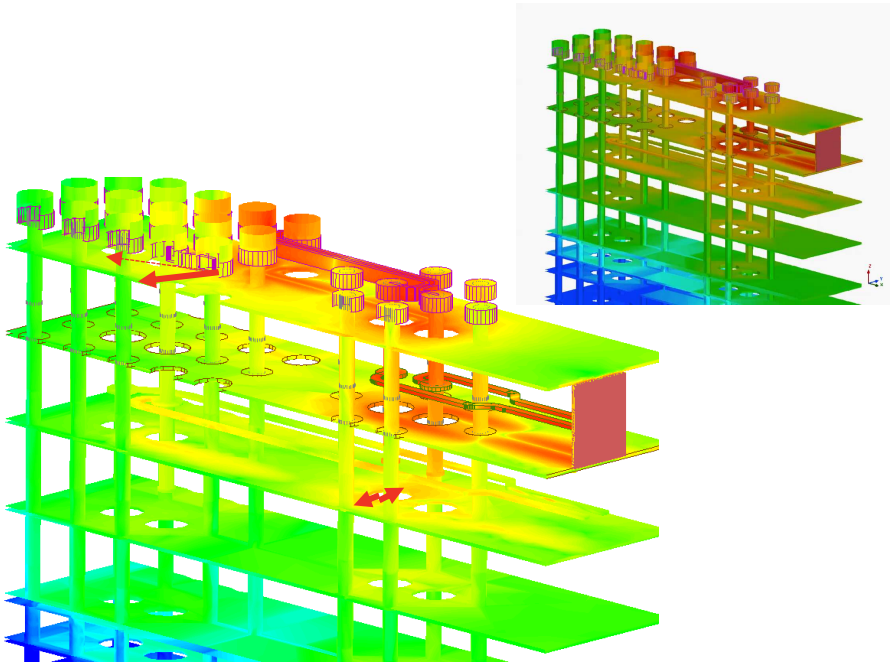
PCB Design and Simulation gets more demanding

Case1: Stripline Escapes



Coupling is existing in the all layers of aggressor vias. Current induced in victim is clearly different for P and N traces with distance. Therefore, coupling is differential and cannot take advantage of common mode rejection.

Case10: DIFF MS Shield



Coupling is existing above top layer and victim signal layer by GSSG diff vias. The coupling above top layer is same with case1 and small portion of it. Current induced in victim layer by GSSG via is equivalent in P & N legs. Therefore induced noise is reduced by common mode rejection.

Trends

- Memory
- Transceiver
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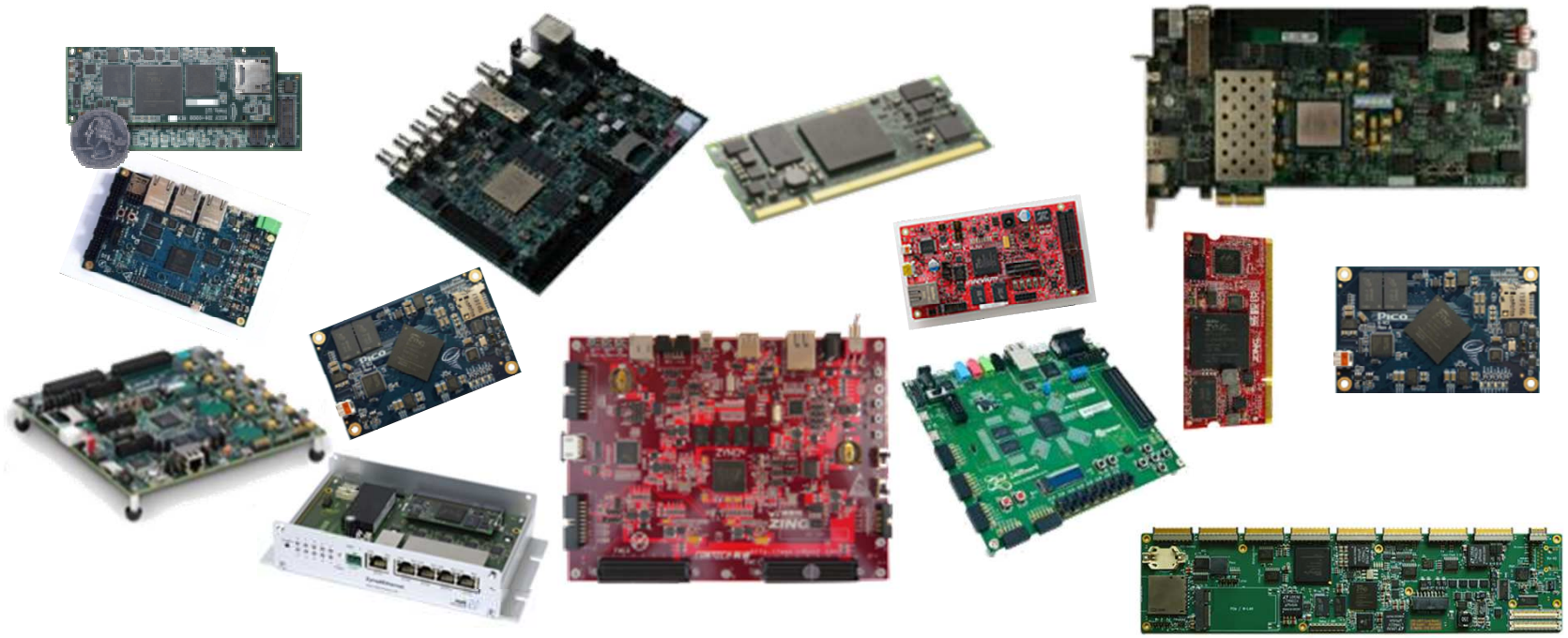
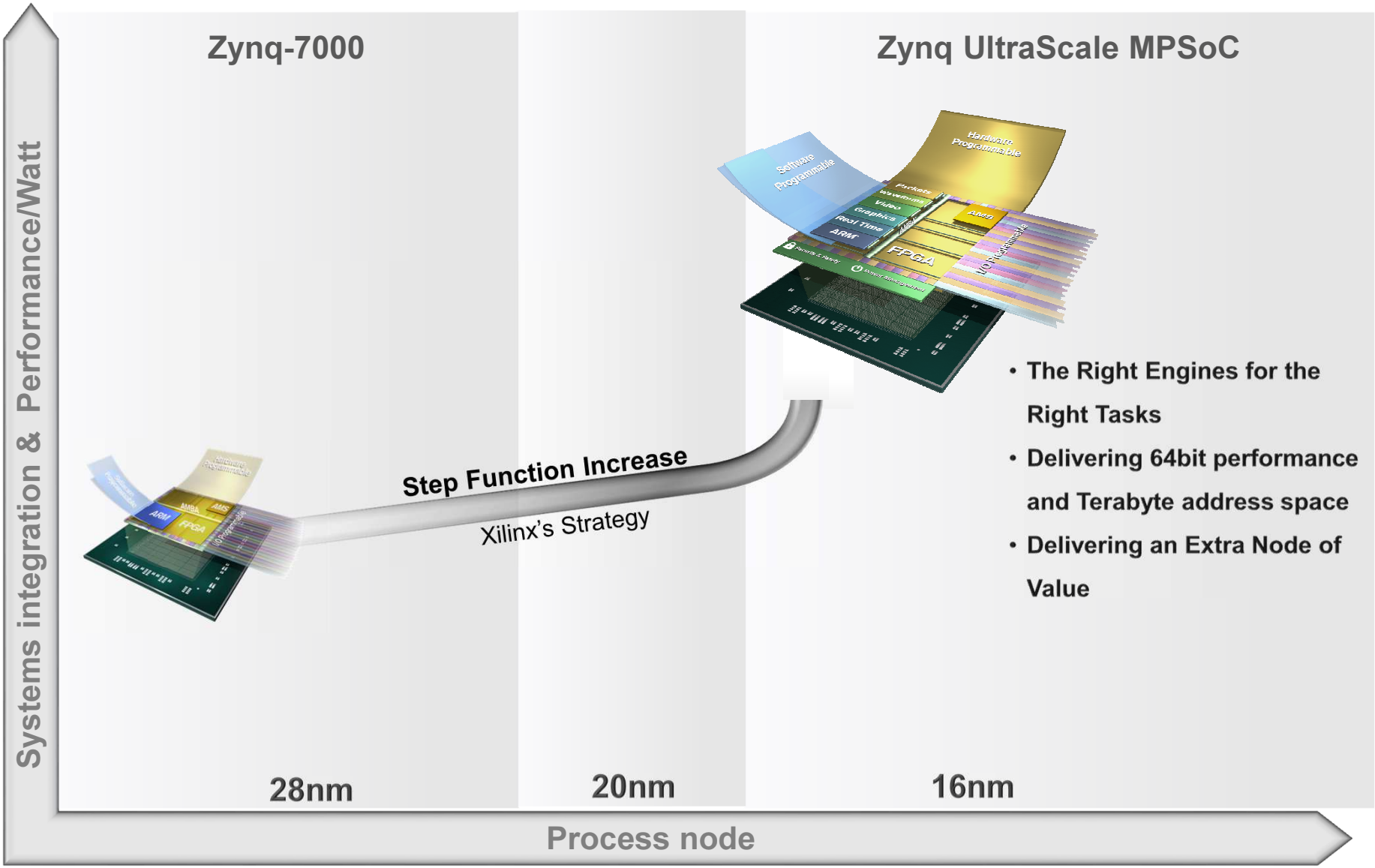
Zynq 7000 – A big success story



- **Wide distribution of Zynq®-7000 All Programmable SoC based boards/kits**
  - 13,000+ boards/kits shipped between Xilinx and Avnet
- **25+ Development Boards and SoM's from Xilinx and its partners**
  - Application & Market Specific Boards

Next Step: From Zynq 7000 to Zynq MPSoC

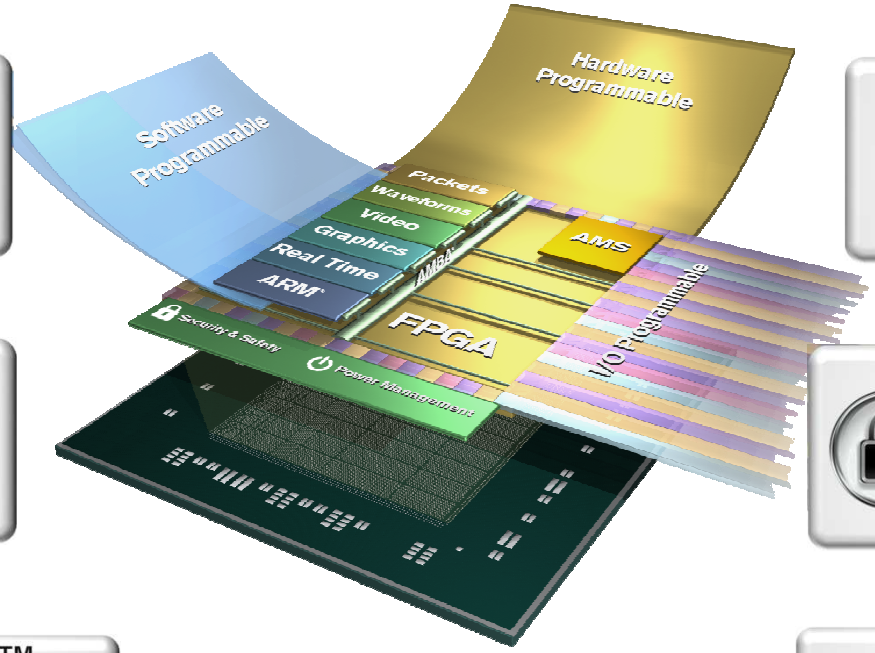


Zynq® UltraScale+™ System Features

Application Processors
ARM Quad-Core Cortex-A53

Power Management
Multiple Power Domains
Power Gated Islands

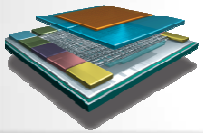
Real-Time Processors
ARM Dual-Core Cortex-R5



Safety & Reliability
IEC61508, ISO26262
System Isolation &
Error Mitigation, Lockstep

Graphics Processor
ARM Mali-400MP

Security
Information Assurance,
Trust Anti-Tamper, TrustZone
Key and Vault Management



UltraScale+™ FPGA Logic
UltraRAM, PCIe®
Gen4, 100G Ethernet

Video CODECs
H.265/264

High Speed Peripherals
USB 3.0, PCIe Gen 2,
SATA3.0, DisplayPort

Trends

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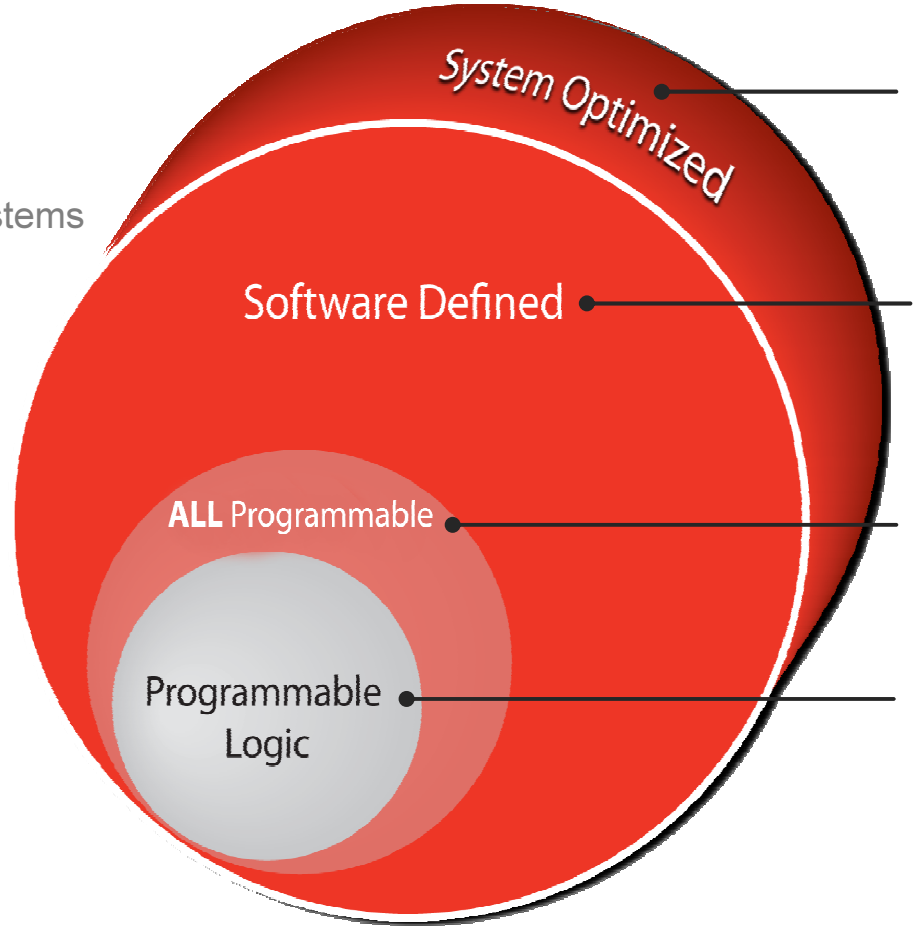
Setting the Course for the Next 5 Years

Goal: 5X Potential Users in 5 Years

- SDx SW-defined Systems
- Zynq MPSoCs

- HLS SW-defined HW
- Zynq SoCs

- FPGAs
- RTL to Bitstream



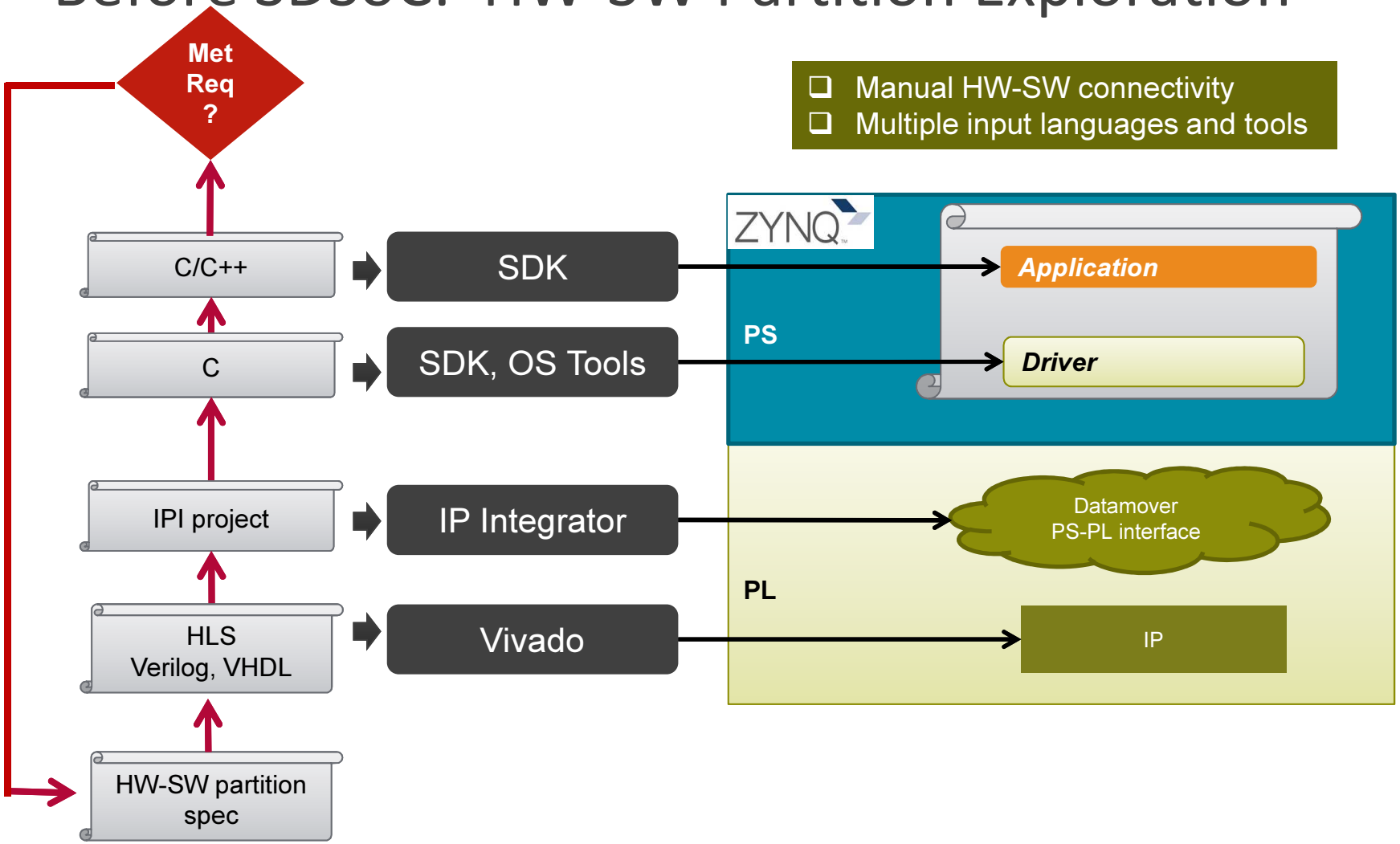
For Highest Growth Megatrends

>250,000 SW Engineers

1000s of SoC Teams with SW *and* HW Engineers

>50,000 HW Engineers

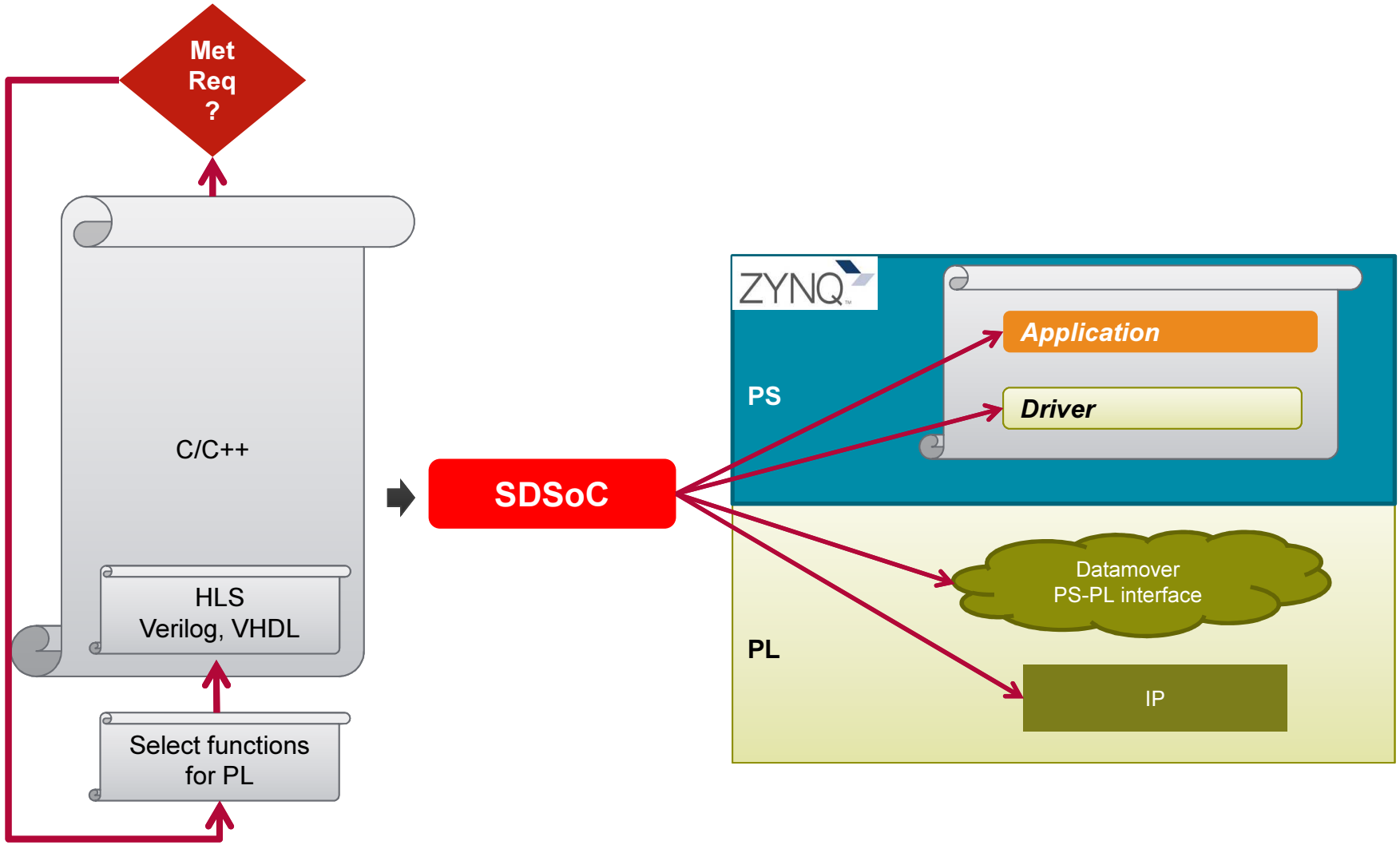
Before SDSoC: HW-SW Partition Exploration



- Manual HW-SW connectivity
- Multiple input languages and tools

Involving multiple discipline to explore architecture

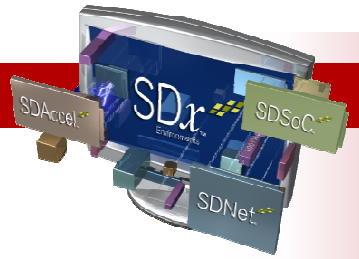
After SDSoC: Automatic System Generation



C/C++ to System in hour, days

All Programmable Abstractions

Xilinx



SW Application Developer

Open & Integrated Development Stack

HW Designer

C, C++ Linux / FreeRTOS / Bare Metal	C, C++, OpenCL x86 PCIe based applications
SDSoC Environment ASSP-like Embedded Flow Auto HW acceleration of SW	SDAccel Environment Algorithmic Synthesis Area / Perf Optimization
VIVADO HLS Develop in Weeks not Months (>1000 users) Over 100X Faster Verification than RTL	
VIVADO Foundation for integrated development stack AXI / IP Integrator / IP Packager	

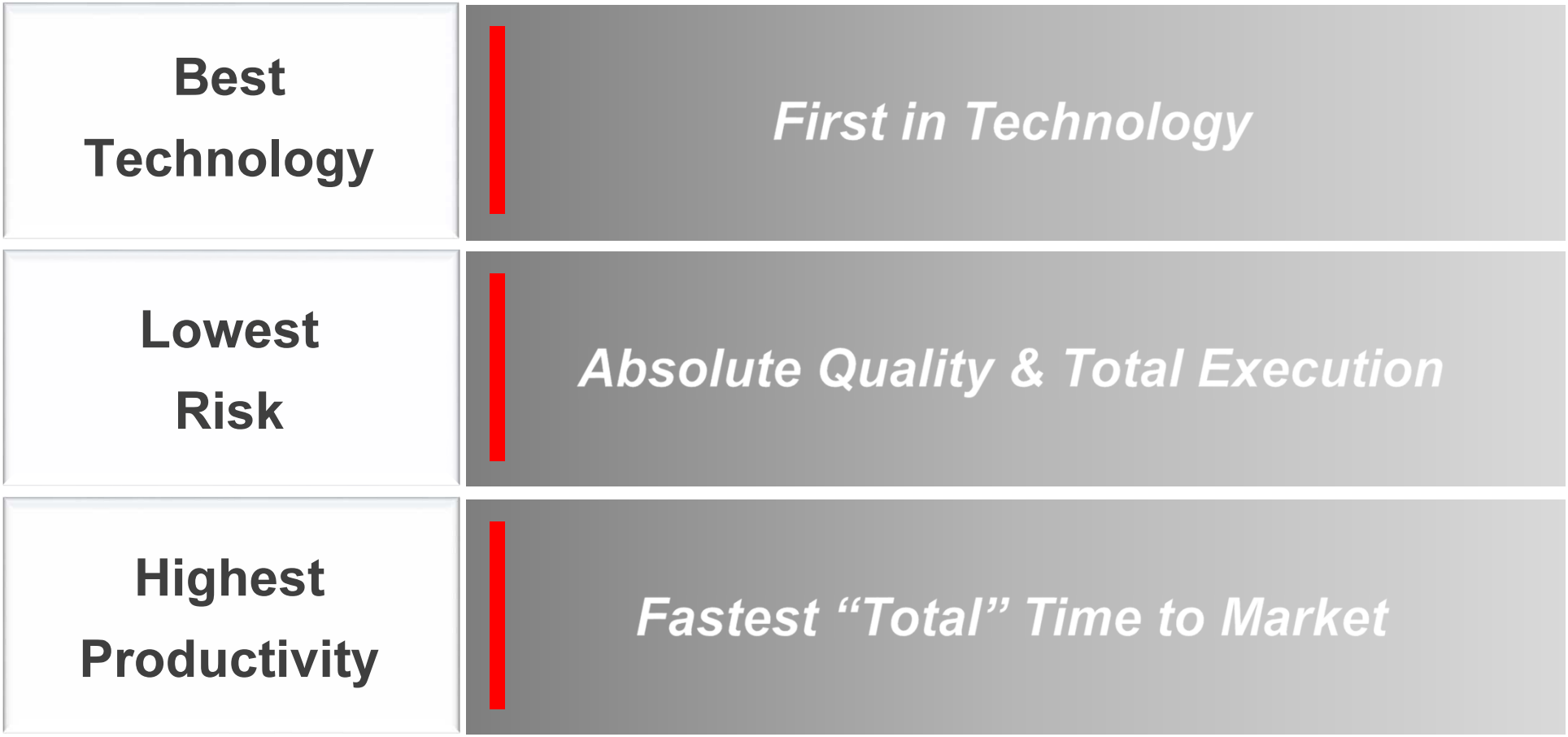
Delivering at All Levels of Abstraction

Business & Roll-Out Status Update

ALL PROGRAMMABLE

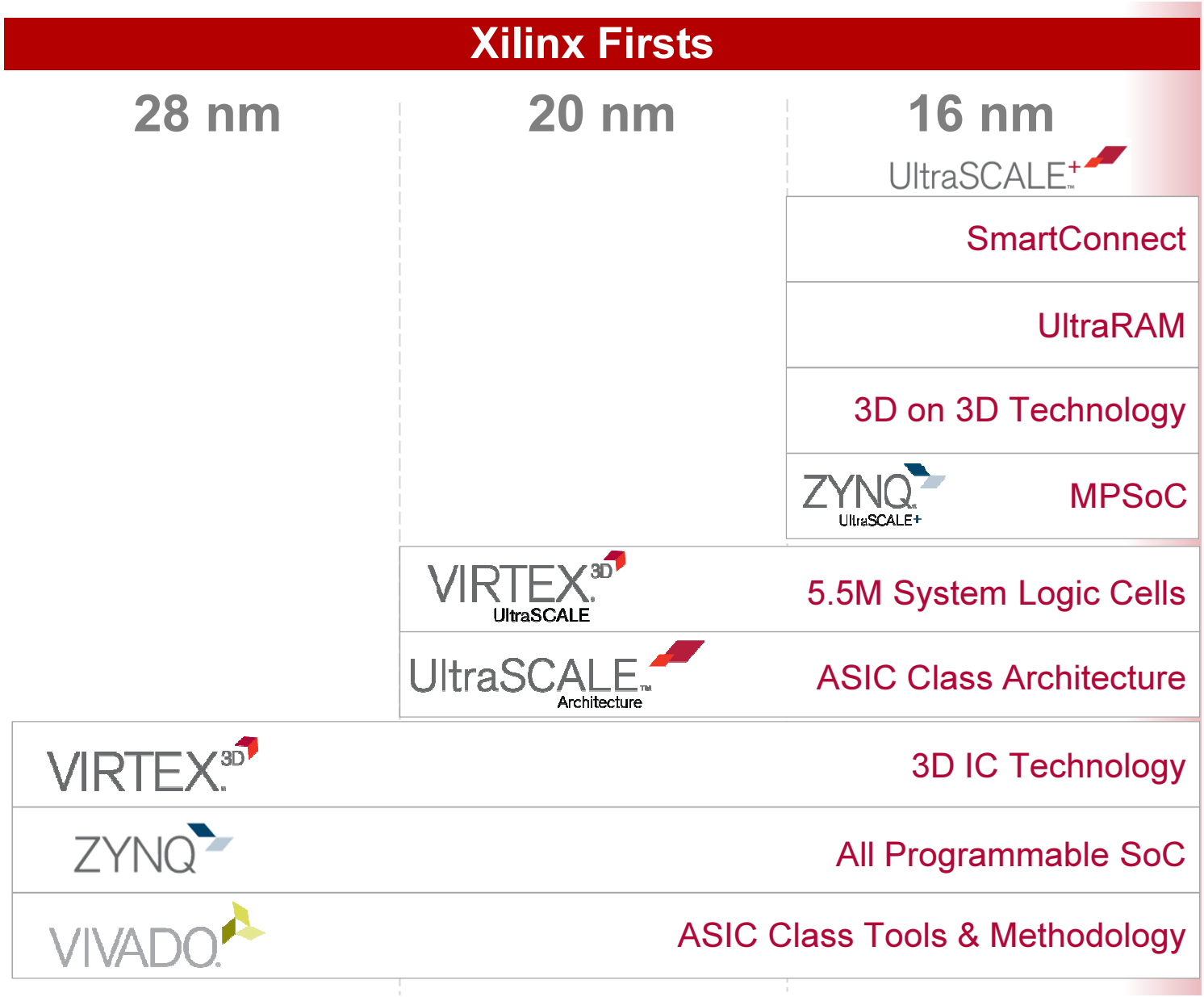
CPU, GPU, NPU, SoC Limitations

Delivering More Compelling Value



Staying a Generation Ahead of Our Competition
. . So You Can Stay Ahead of Yours

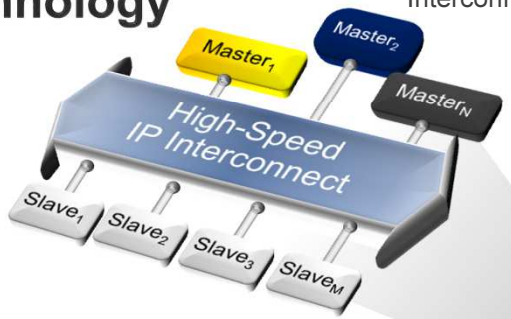
Delivering Multi-Node Technology Leadership



Technology Firsts with UltraScale+

SmartConnect Technology

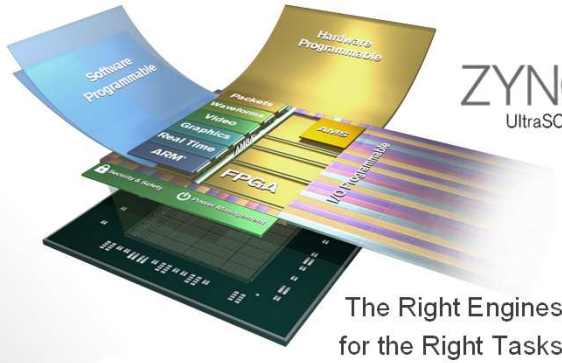
Intelligent Interconnect



Unmatched Flexibility & Efficiency

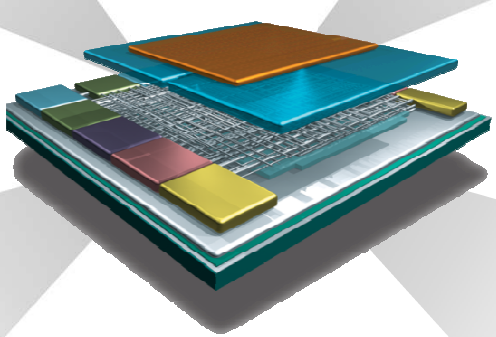
UltraSCALE+

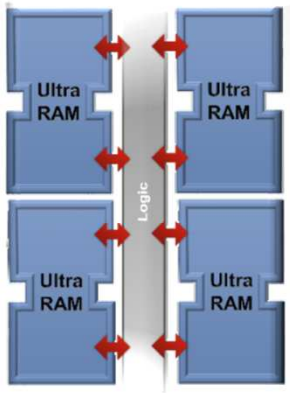
MPSoC



The Right Engines for the Right Tasks

Unmatched Systems Integration



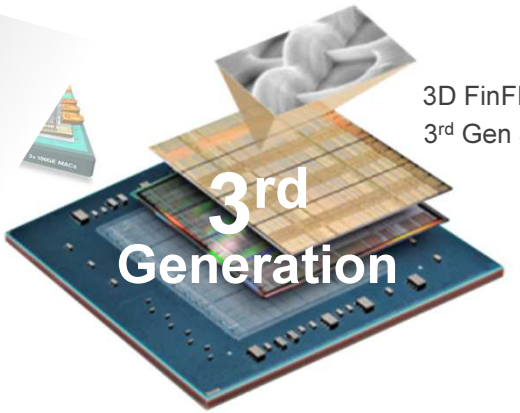


UltraRAM

Up to 432 Mb

Unmatched Density, Performance & Power Efficiency

3D on 3D



3D FinFET on 3rd Gen 3D IC

Unmatched Integration & Bandwidth/Watt

XILINX ALL PROGRAMMABLE

Delivering More Compelling value

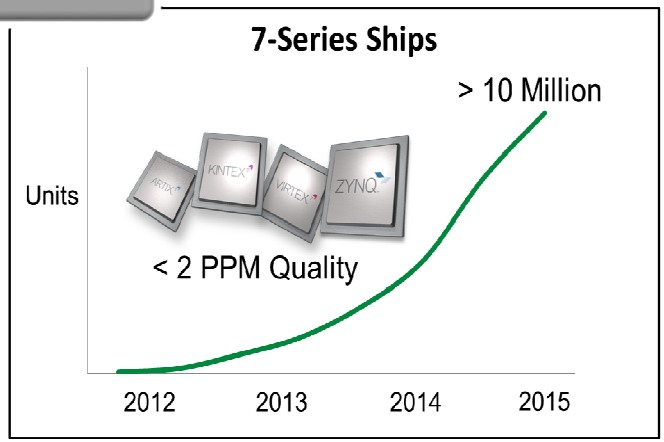
Best Technology	• Multi-node Technology Leadership • Broadest Portfolio • Best Performance / Watt
Lowest Risk	***Absolute Quality & Total Execution***
Highest Productivity	***Fastest "Total" Time to Market***

Staying a Generation Ahead of Our Competition
. . So You Can Stay Ahead of Yours

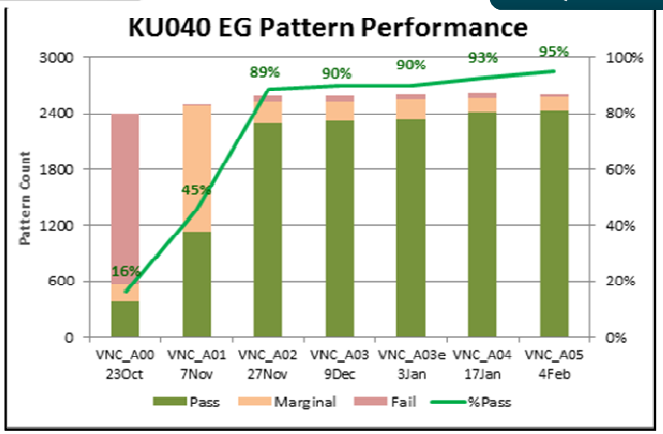
Proven New Product Introduction Methodology

- **5th Gen Product Introduction Methodology**
  - Scales to meet new demands at each node
- **Superior process modeling**
  - 2nd Gen process performance learning vehicles
- **4 Phase Verification & Characterization**
  - Early issue identification & resolution

28nm **Highest Production Quality**



20nm **Quality from Day 1** **Production Q4'14**



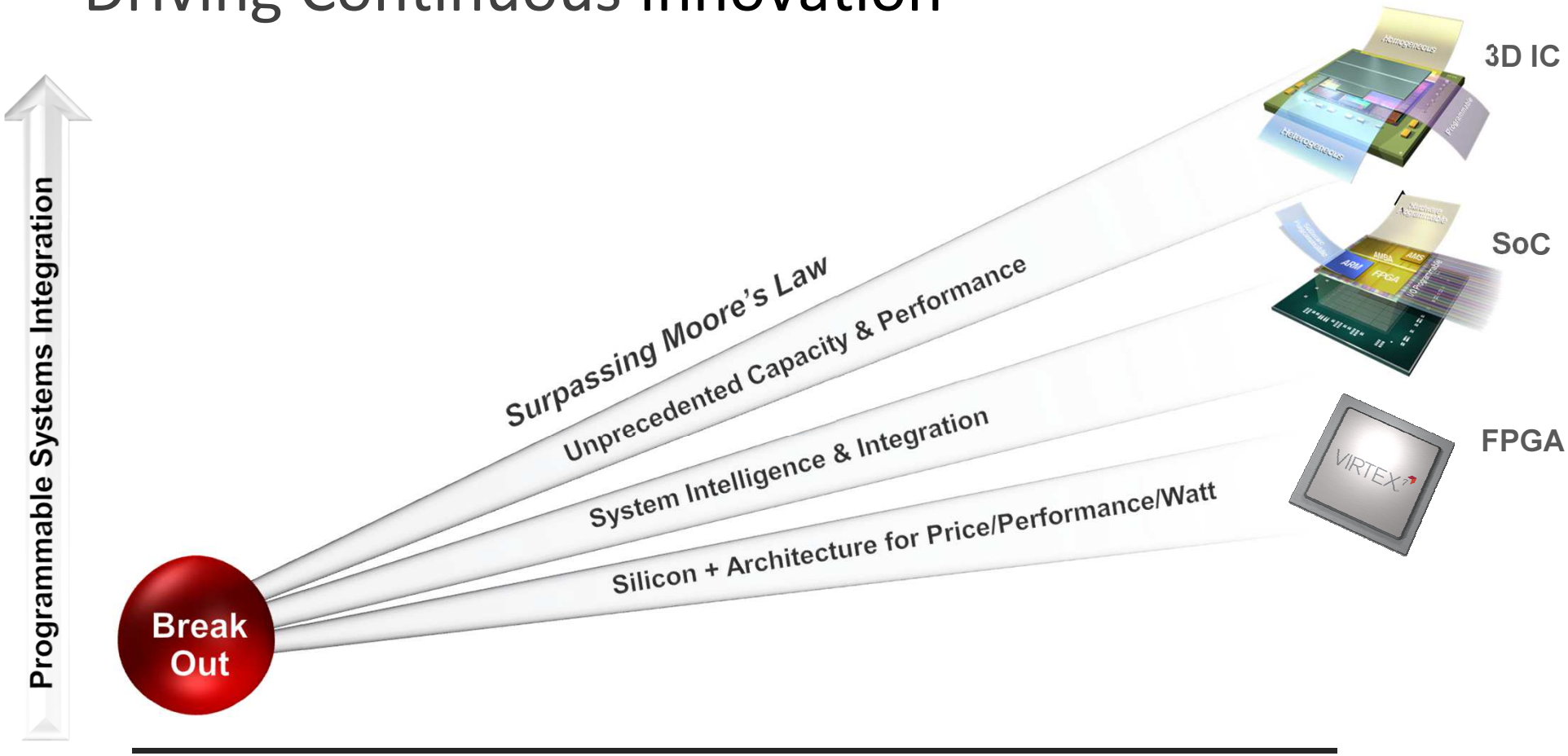
A Proven Formula for Delivering Absolute Quality

Delivering More Compelling value

Best Technology	• Multi-node Technology Leadership • Broadest Portfolio • Best Performance / Watt
Lowest Risk	• Proven New Product Introduction • Highest Initial & Production Quality • Delivering On Time & On Spec
Highest Productivity	***Fastest "Total" Time to Market***

Staying a Generation Ahead of Our Competition
. . So You Can Stay Ahead of Yours

Driving Continuous Innovation

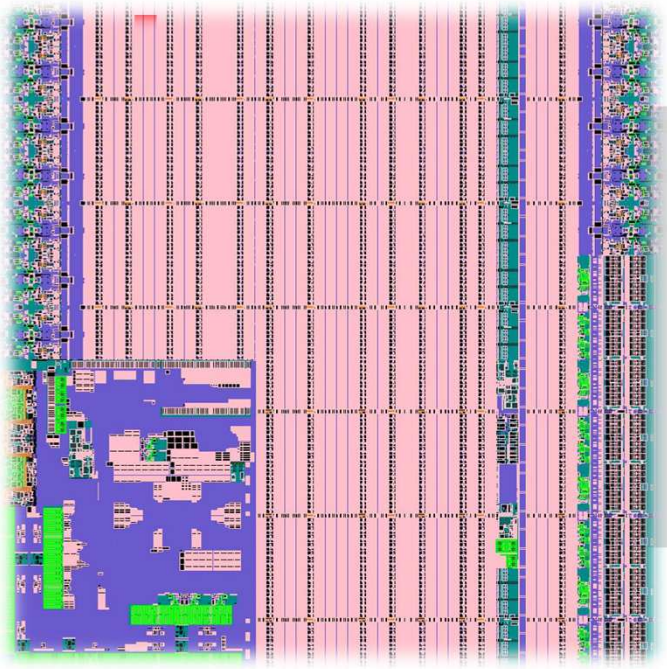


Tools	VIVADO	UltraFAST Design Methodology	SDx	
Architecture	**7 Series**	**UltraScale™ Architecture**		
Process	**28HPL**	**20SoC**	**16FinFET+**	**7nm**

16nm: Industry's First 14/16nm MPSoC Tapeout

Zynq UltraScale+ Lead Device – ZU9EG

Taped Out On-time in Q2



UltraScale+ Portfolio set out to deliver…

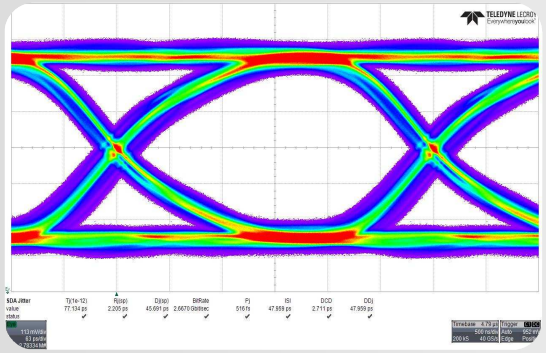
- ✓ 2X-5X System Performance/Watt
- ✓ Unmatched System Integration & Intelligence
- ✓ Highest Levels of Security and Safety

And Now Devices Are Back…

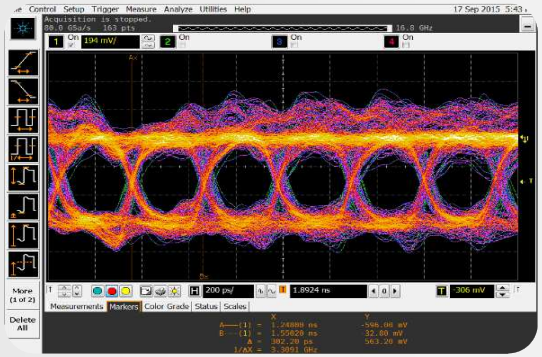
Logic Fabric Up & Running in Record Time

Parallel I/O

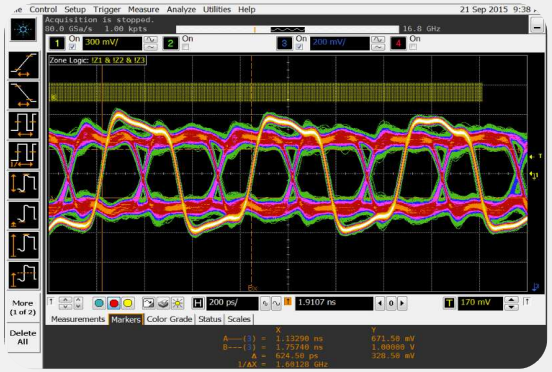
General I/O Right at Bring-Up with Eye Wide-Open



DDR4 at 2,667 Mb/s Error-Free in 5 Minutes

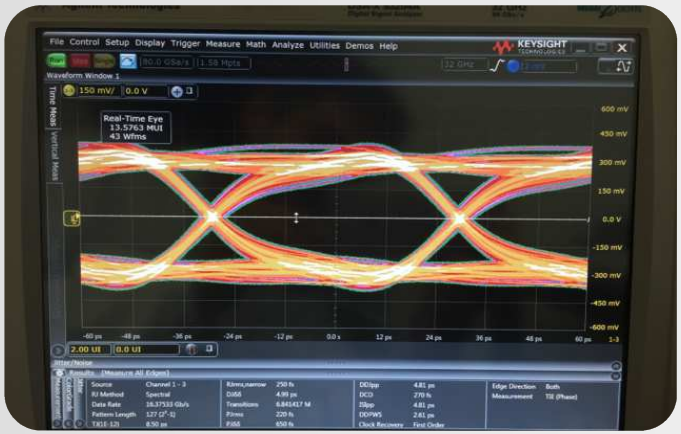


DDR4 at 2,667 Mb/s Error-Free with Noise on Day 4

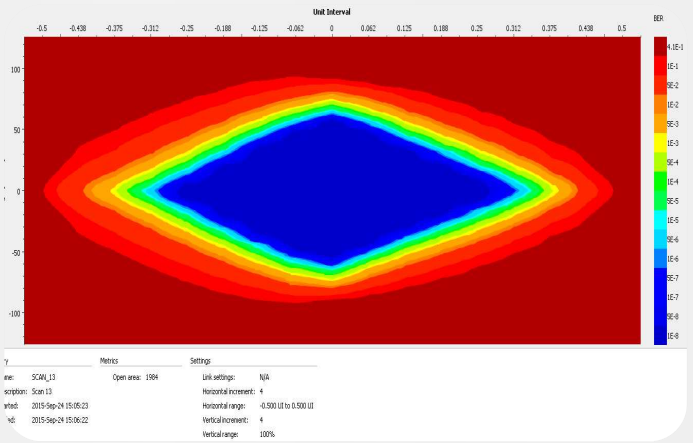


Serial I/O

GTH TX at 1 16.375 Gb/s on Day 1



GTH RX at 16.375 Gb/s on Day 2



16nm

Zynq® UltraScale+™ MPSoCs

			Smarter Control and Vision					Smarter Network					
		Device Name[1]	ZU2EG	ZU3EG	ZU4EV	ZU5EV	ZU7EV	ZU6EG	ZU9EG	ZU15EG	ZU11EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB										
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core										
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz										
		Memory	L2 Cache 64KB										
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC										
		Static Memory Interfaces	NAND, 2x Quad-SPI										
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet										
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO										
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains										
		Security	RSA, AES, and SHA										
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor										
PS to PL Interface			12 x 32/64/128b AXI Ports										
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	504	469	600	747	653	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	461	429	548	682	597	847	1,045
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.2	6.9	8.8	11.3	9.1	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	11.0	25.1	32.1	26.2	21.1	28.0	34.6
		UltraRAM (Mb)	-	-	14.0	18.0	27.0	-	-	31.5	22.5	28.7	36.0
	Integrated IP	DSP Slices	240	360	728	1,056	1,728	1,973	2,520	3,528	2,928	1,590	1,968
		Video Codec Unit (VCU)	-	-	1	1	1	-	-	-	-	-	-
		PCI Express® Gen 3x16 / Gen4x8	-	-	2	2	2	-	-	-	4	4	5
		150G Interlaken	-	-	-	-	-	-	-	-	2	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	1	2	4
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1
	Speed Grades	Extended[2]	-1 -2L -3					-1 -2L -3					
		Industrial	-1 -1L -2					-1 -1L -2					

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (T) = 0°C to 110°C).

Zynq® UltraScale+™ MPSoCs

PS I/Os(1), 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os
PS-GTR 6Gb/s, GTH 16.3Gb/s, GTY 32.75Gb/s

Pkg Footprint(2)	Dimensions (mm)	Smarter Control and Vision					Smarter Network					
		ZU2EG	ZU3EG	ZU4EV	ZU5EV	ZU7EV	ZU6EG	ZU9EG	ZU15EG	ZU11EG	ZU17EG	ZU19EG
A484(3)	19x19	169, 24, 52 4, 0, 0	169, 24, 52 4, 0, 0									
A625(3)	21x21	169, 24, 156 4, 0, 0	169, 24, 156 4, 0, 0									
C784(3)	23x23	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
B900	31x31			214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0						
C900	31x31						214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0			
B1156	35x35						214, 120, 208 4, 24, 0	214, 120, 208 4, 24, 0	214, 120, 208 4, 24, 0			
C1156	35x35					214, 48, 312 4, 24, 0				214, 48, 312 4, 24, 0		
B1517	40x40									214, 72, 416 4, 16, 0	214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40					214, 48, 416 4, 24, 0				214, 48, 416 4, 32, 0		
C1760	42.5x42.5									214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5										214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45										214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
3. These packages are only offered in 0.8mm ballpitch. All other packages are offered in 1.0mm ball pitch.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Kintex® UltraScale+™ FPGAs

			General-Purpose Devices			Signal Processing Optimized Devices		
	Device Name	KU3P	KU7P	KU11P	KU15P	KU5P	KU9P	KU13P
Logic	System Logic Cells (K)	256	504	653	1,143	475	600	747
	CLB Flip-Flops (K)	234	461	597	1,045	434	548	683
	CLB LUTs (K)	117	230	299	523	217	274	341
Memory	Max. Distributed RAM (Mb)	3.8	6.2	9.1	9.8	6.7	8.8	11.3
	Total Block RAM (Mb)	5.1	11.0	21.1	34.6	16.9	32.1	26.2
	UltraRAM (Mb)	18.0	27.0	22.5	36.0	18.0	0	31.5
Integrated IP	DSP Slices	1,056	1,728	2,928	1,968	1,824	2,520	3,528
	Video Codec Unit	1	1	0	0	0	0	0
	PCIe® Gen3 x16 / Gen4 x8	2	2	4	5	1	0	0
	150G Interlaken	0	0	2	4	0	0	0
	100G Ethernet w/RS-FEC	0	0	1	4	1	0	0
I/O	Max. Single-Ended HD I/Os	96	96	96	96	72	96	96
	Max. Single-Ended HP I/Os	208	416	416	572	208	208	208
	GTH 16.3Gb/s Transceivers	16	24	32	44	0	28	28
	GTY 32.75Gb/s Transceivers	0	0	20	32	16	0	0
Speed Grades	Extended	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2
	Footprint[1,2]	Dimensions (mm)	HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s					
Packaging	B784	23x23[3]	96, 208, 16, 0					
	B676	27x27				72, 208, 0, 16		
	C676	27x27	96, 208, 16, 0	96, 208, 16, 0				
	D900	31x31		96, 312, 16, 0	96, 312, 16, 0			
	E900	31x31					96, 208, 28, 0	96, 208, 28, 0
	D1156	35x35			96, 416, 16, 0	96, 520, 16, 0		
	E1156	35x35		96, 416, 24, 0	96, 416, 24, 0			
	E1517	40x40			96, 416, 32, 20	96, 416, 32, 24		
	A1760	42.5x42.5				96, 416, 44, 32		
	E1760	42.5x42.5				96, 572, 32, 24		

Notes:
1. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
2. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product* Overview.
3. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.

Virtex® UltraScale+™ FPGAs

	Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P
Logic	System Logic Cells (K)	862	1,314	1,724	2,586	2,684	3,578
	CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,454	3,272
	CLB LUTs (K)	394	601	788	1,182	1,227	1,636
Memory	Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	38.7	51.6
	Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5
	UltraRAM (Mb)	90.0	132.2	180.0	270.0	324.0	432.0
Integrated IP	DSP Slices	2,280	3,474	4,560	6,840	8,928	11,904
	PCIe® Gen3 x16 / Gen4 x8	2	4	4	6	3	4
	150G Interlaken	3	4	6	9	6	8
	100G Ethernet w/ RS-FEC	3	4	6	9	9	12
I/O	Max. Single-Ended HP I/Os	520	832	832	832	624	832
	GTY 32.75Gb/s Transceivers	40	80	80	120	96	128
Speed Grades	Extended	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3	-1 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2

	Footprint[1,2]	Dimensions (mm)	HP I/O, GTY 32.75Gb/s					
Footprint Compatible with 20nm UltraScale Devices	C1517	40x40	520, 40					
	F1924[3]	45x45					624, 64	
	A2104	47.5x47.5		832, 52	832, 52	832, 52		
		52.5x52.5[4]						832, 52
	B2104	47.5x47.5		702, 76	702, 76	702, 76	624, 76	
		52.5x52.5[4]						702, 76
	C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96	
		52.5x52.5[4]						416, 104
	A2577	52.5x52.5				448, 120	448, 96	448, 128

Notes:
1. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
2. All packages are 1.0mm ball pitch.
3. GTY transceiver up to 16.3Gb/s. Refer to data sheet for details.
4. These 52.5x52.5mm packages have the same PCB ball footprint as the 47.5x47.5mm packages and are footprint compatible.