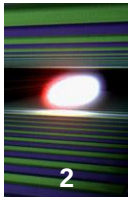
European XFEL Detector and DAQ related hardware and firmware developments

4th MicroTCA Workshop for Industry and Research

Bruno Fernandes
Advance Electronics Group

Agenda



Overview

- Hardware Environment
- FPGA Development environment
- High-Speed Digitizers
- High level FPGA Application development
- Other Developments

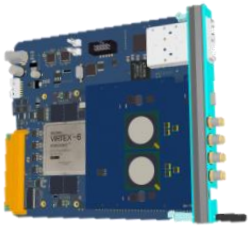
FPGA Development environment

FPGA Development

- Board firmware development
- Custom RTM/PCBs deveopment
- Development of custom propose FPGA Algorithms/Modules

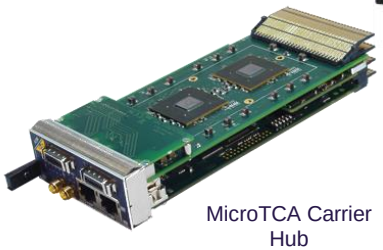
Clock & Control RTM
(University Collage London)

DAMC2 – Universal digital AMC (DESY)



High-Speed Digitizer Family
(Signal Processing Devices Sweden AB)

Timing System
(Stockholm University / DESY)



MicroTCA Carrier Hub
(N.A.T.)

High-performance DSP and FPGA board
(DMCS/DESY)

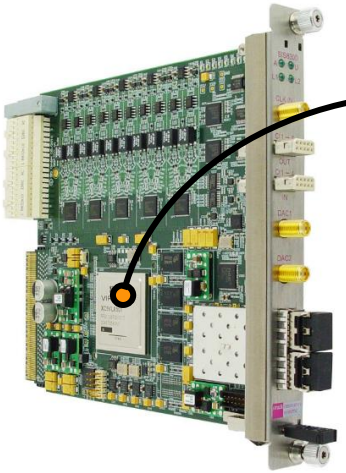
SIS8300 – ADC AMC
(Struck Innovative Systems)

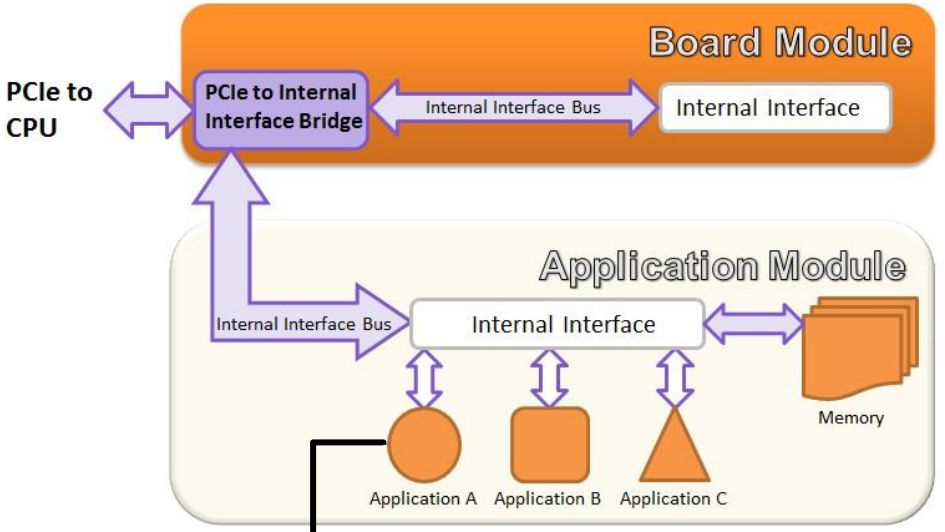
VHDL

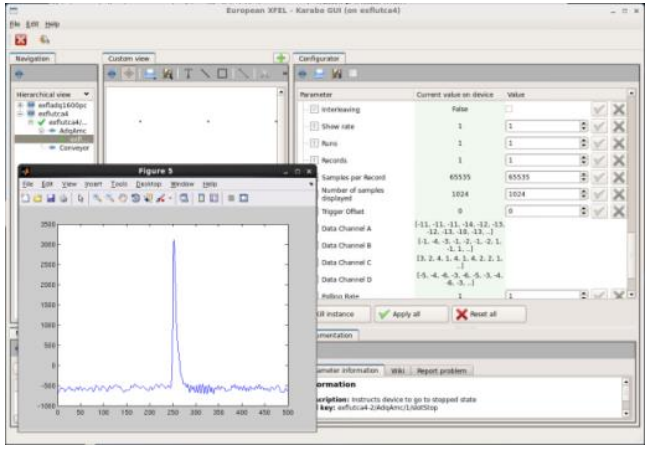
MATLAB SIMULINK

OpenSPL

FPGA Development environment







VHDL Register Definition

Application A:

…

"Constant Input": Register, Read Only, 14 bits, Floating-Point, 5 bit Fractional, "It's just an Example";

…

MAP/XML Description

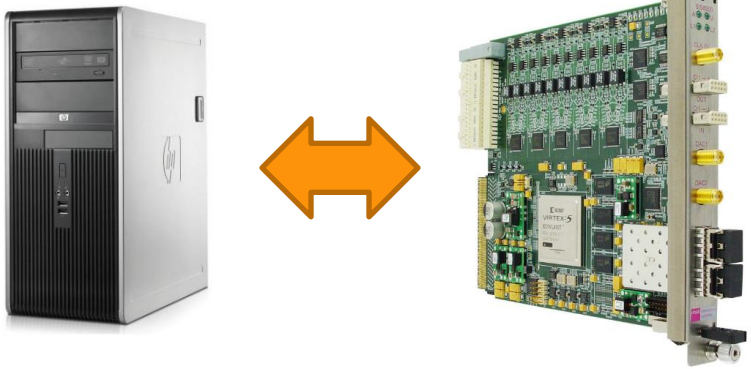
FPGA Development environment

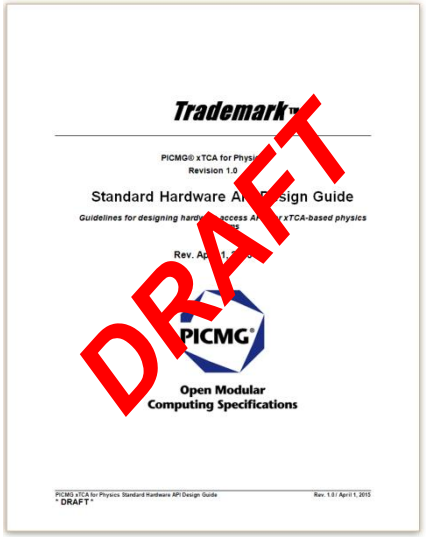
Standard Hardware API (with PICMG group)

- Provide reading of basic information about the Board and implemented Applications
- No knowledge of registers are required
- Software can check compatibility
- Definition for Interrupt handling
- Standard Modules definition (DMA)

PICMG®

Open Modular Computing Specifications

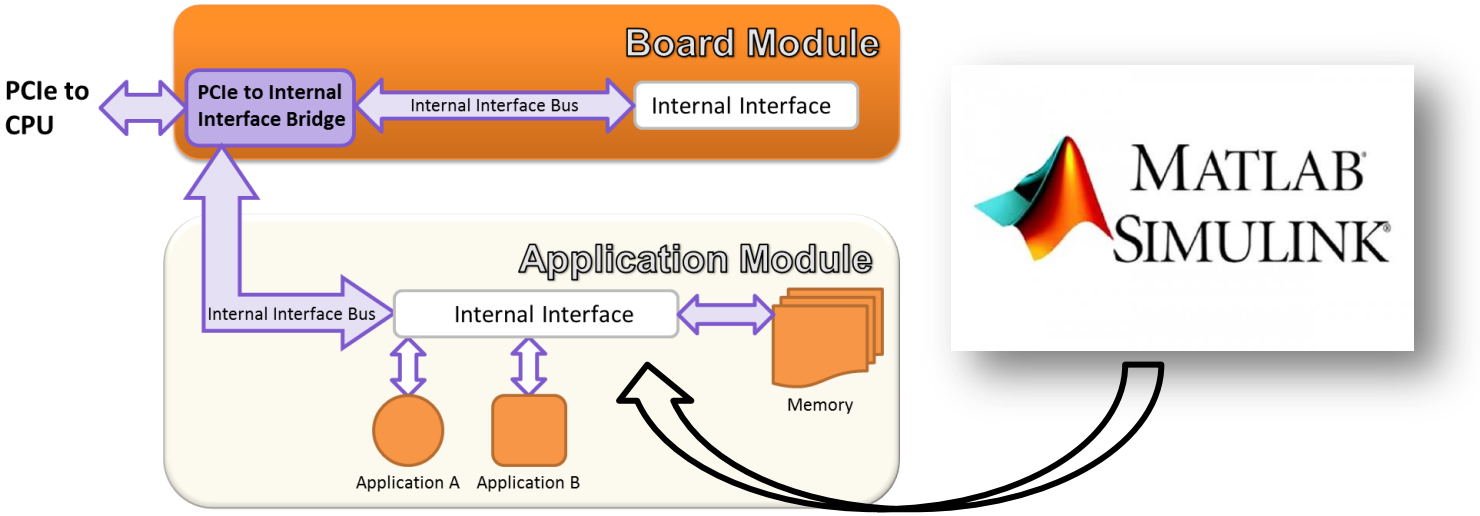




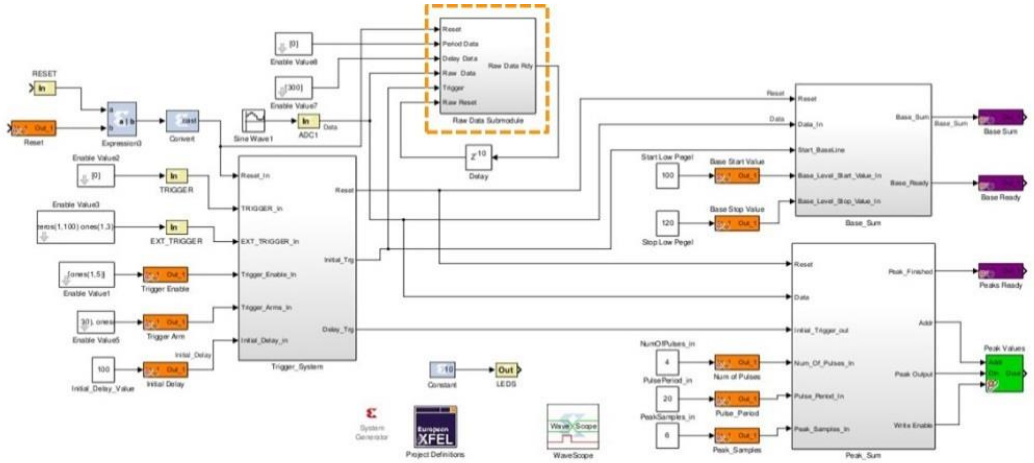
High level FPGA Application development

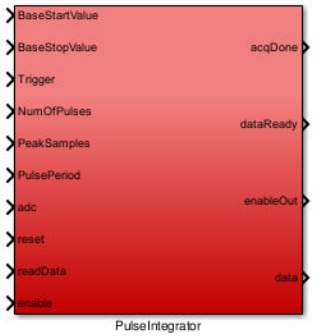
Application development in Simulink

- Graphical environment allows for **people unfamiliar with HDL**
- **Automatically setups the design environment** for the target board and available features (Ports and Generics)
- Possible to define user **registers and memories** and logic to communicate via the chosen Bus protocol
- Easy to **port and distribute applications** to other projects/boards
- Integration of **Matlab** allows for powerful test environments



High level FPGA Application development





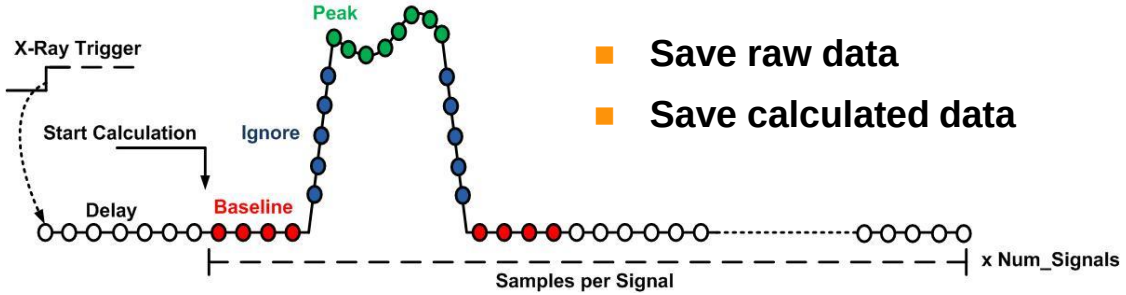
Standalone module of the application

MAP FILE

XML FILE

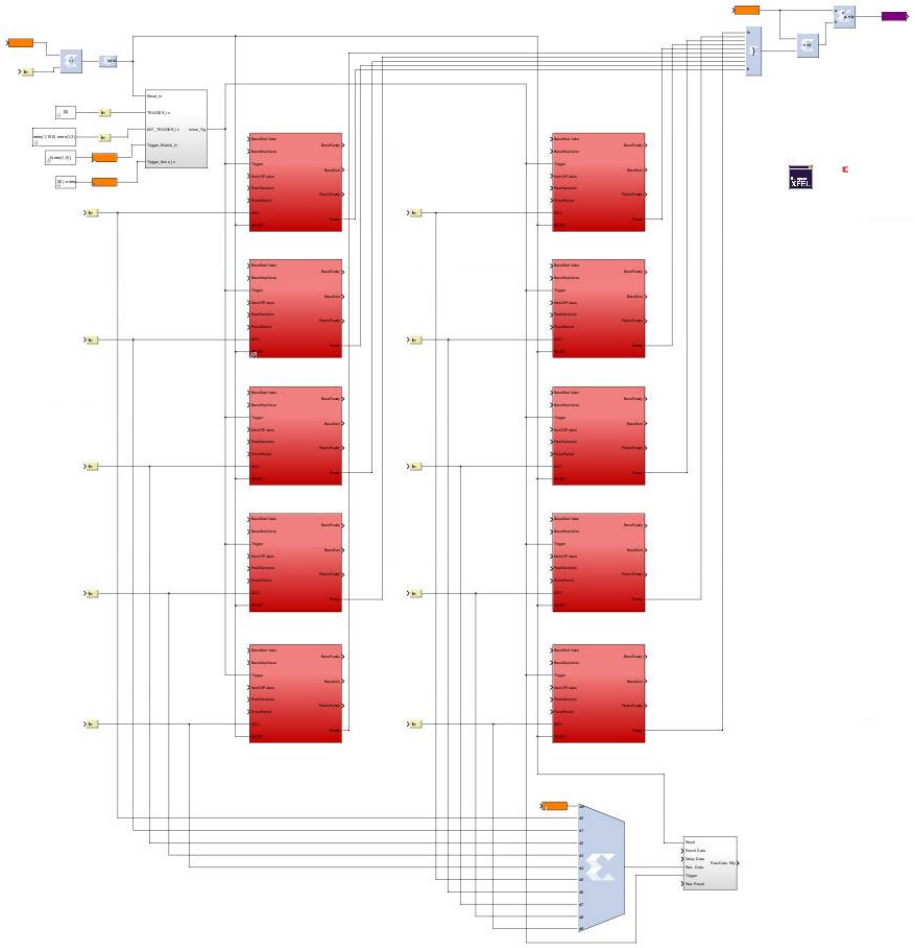
User Registers and Memories Description

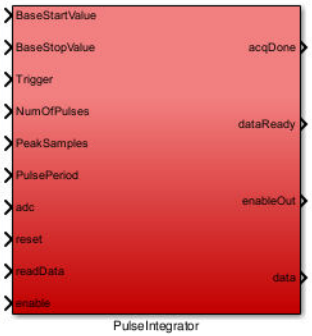
Pulse Integrator Application



- **Save raw data**
- **Save calculated data**

High level FPGA Application development





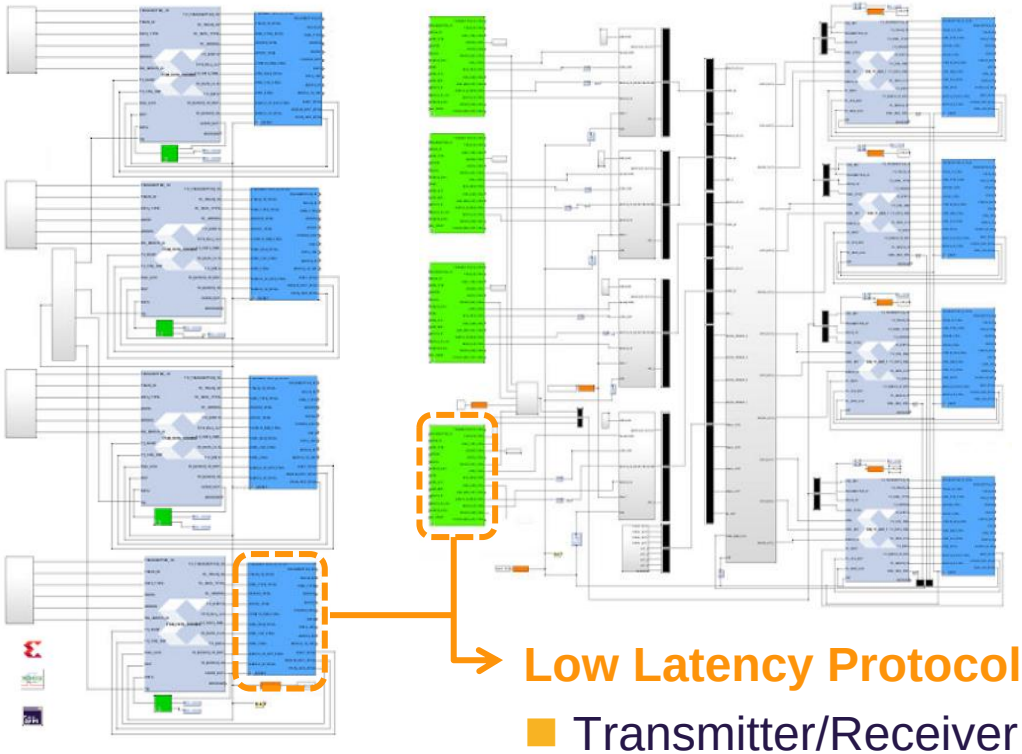
Standalone module of the application

Pulse Integrator Application for 10 ADC Channels

High level FPGA Application development

VETO Source

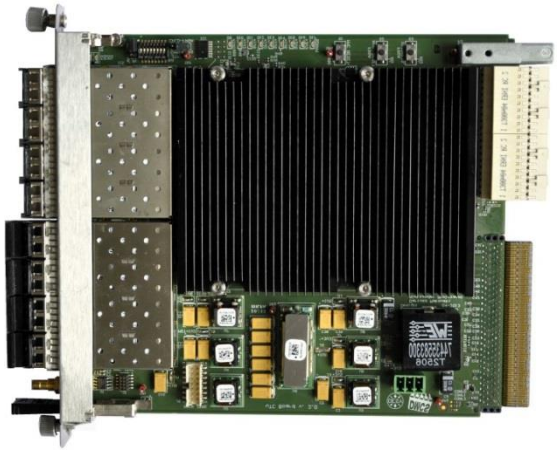
VETO Unit



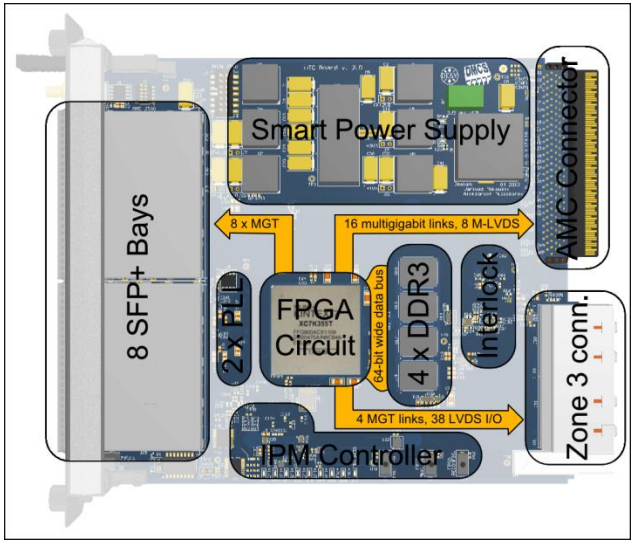
Low Latency Protocol Interface

- Transmitter/Receiver interface to XFEL custom Protocol
- Protocol is implemented using FPGAs GTX Transceiver (SFP board connector)
- Block simulates hardware behavior in the Simulink environment

High level FPGA Application development



DESY DAMC-TCK7



Data Processing and Telecommunication Module DAMC-TCK7

- To be used as a VETO unit
- Board firmware provided by DESY
- Integration with the XFEL Simulink Framework using the available VETO unit module

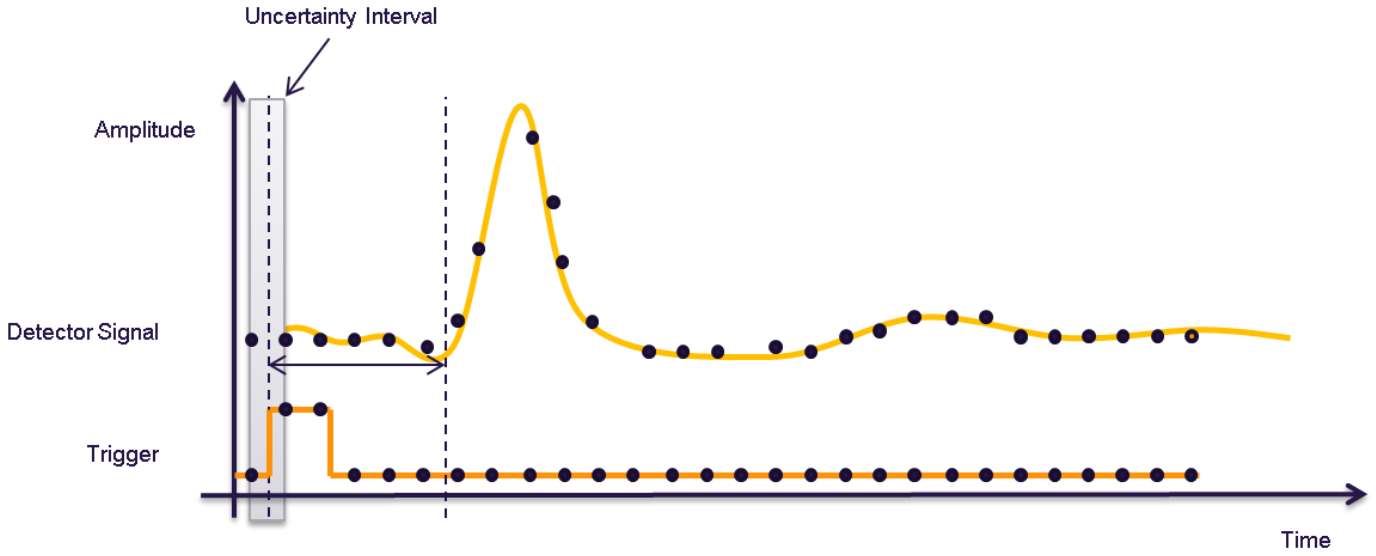
High-Speed Digitizers

Digitizers with high speed ADCs (2/4/8 MSPS) accompanied with a Xilinx FPGA are used in XFEL for online data processing.

- SP-Device ADQ412

SAMPLE RATE OPTIONS				
OPTION	STD.	–3G	–4G	
4 CHANNELS MODE				
Number of channels	4	4	4	
Sampling rate	1	1.8	2	GSPS
Analog bandwidth	2	2	2	GHz
SFDR @149MHz	63	63	63	dBc
SNR @149MHz	57	57	55	dB
2 CHANNELS MODE				
Number of channels	2	2	2	
Sampling rate	2	3.6	4	GSPS
Analog bandwidth	1.3	1.3	1.3	GHz
SFDR @149MHz	60	60	63	dBc
SNR @149MHz	55	55	55	dB

User logic architecture



TDC Core

Improved trigger precision

Zero Suppression

Removes baseline level to from signal

Energy Calculation

Integrates signal area with offset removal

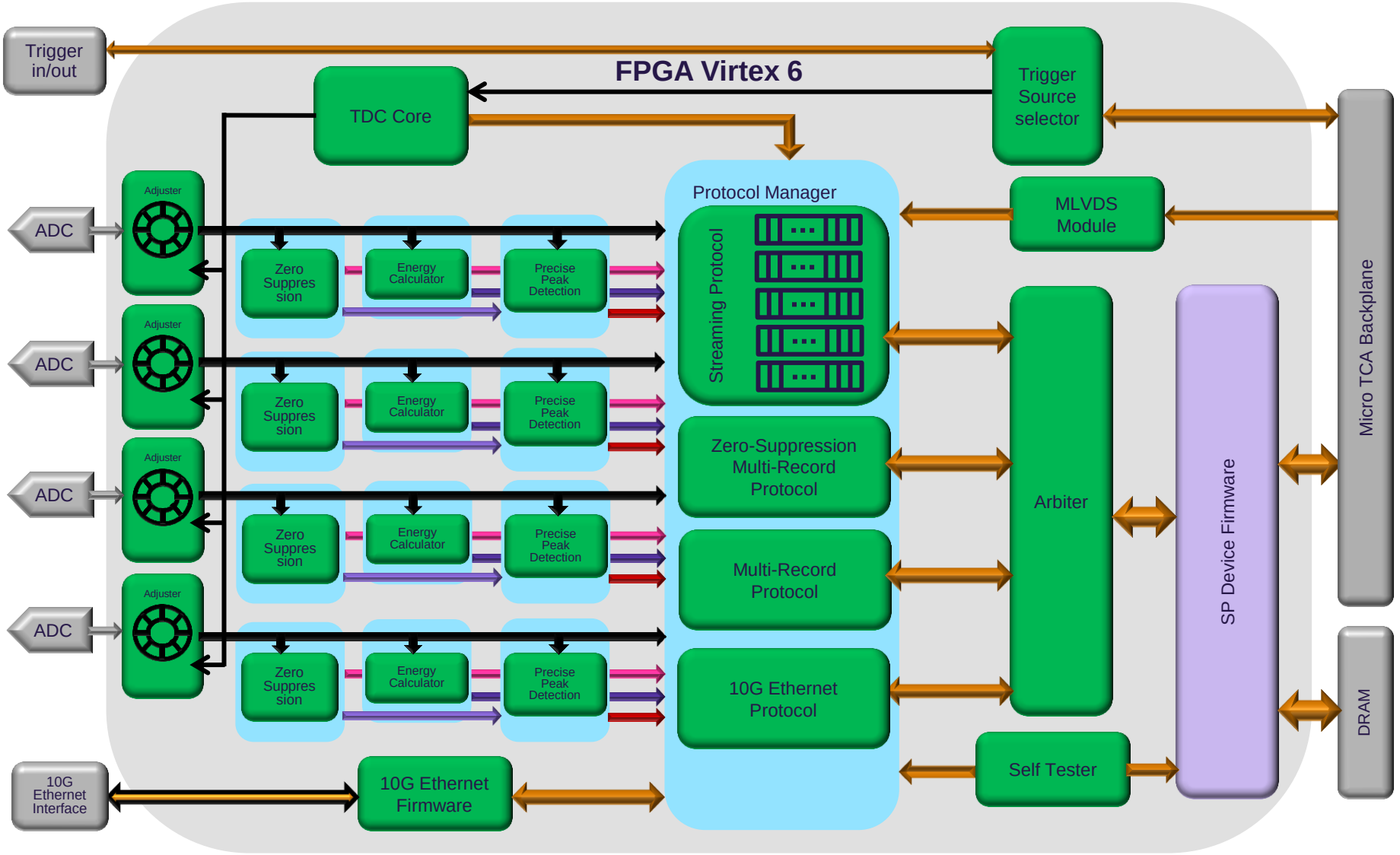
Precise peak detection

Detects peak interval for each pulse

Each Algorithm:

- used in 2/4 Channel mode
- has own protocol packet
- can be disable on firmware

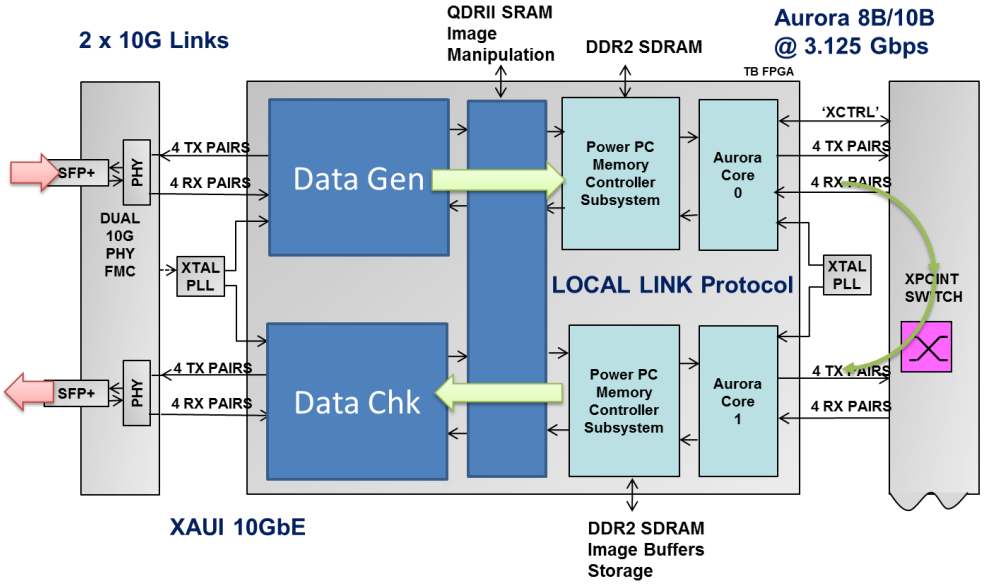
User logic architecture



Further Developments

Train Builder - ATCA board with 5 FPGAs used to reorder the image data

- 4 FMCs where a quadrant of the image is receive
- Each FMC is connect to a FPGA which processes the data
- A 5th FPGA control the Xpoint Switch (data) and also clock and trigger distribution

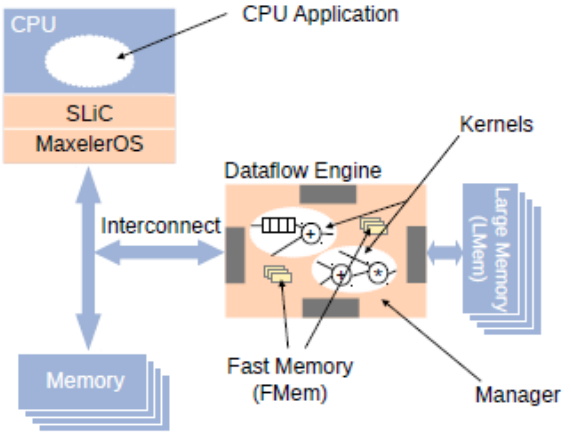


Other Developments

Maxeler Solution

- Custom boards with CPUs and FPGAs
- High level FPGA development, based on Dataflows engines
- “A dataflow application consists of CPU code (describe in C) and large amount of data running in dataflow engines.”
- Boards interfaces are taken care by the IDE

MAXELER Technologies
MAXIMUM PERFORMANCE COMPUTING



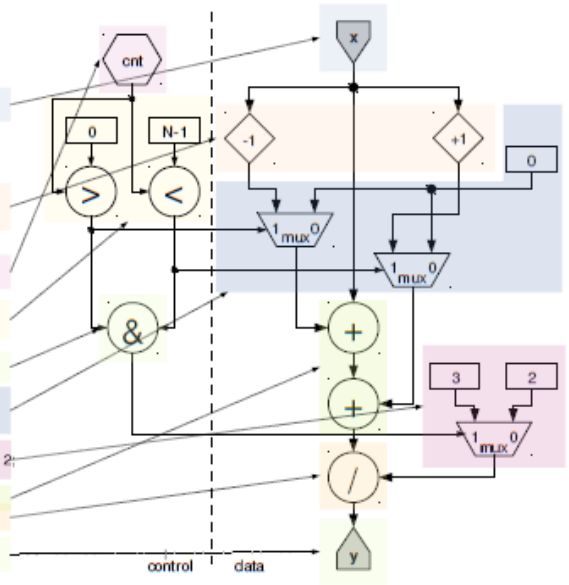
OpenSPL

European XFEL

Other Developments

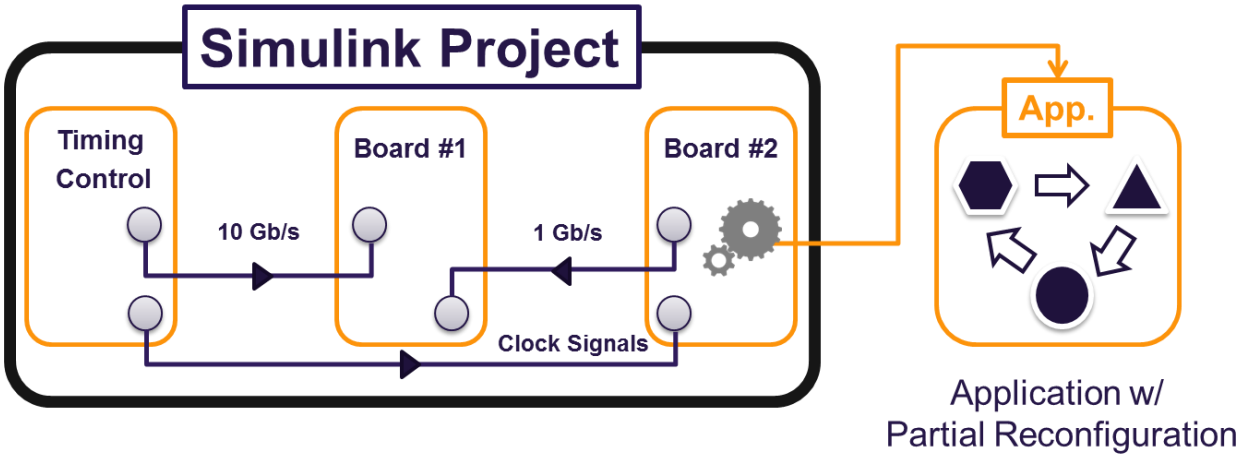
- MAX4N with 3 QSFP ports with data rate of 40 Gbps
- FPGA **Altera** Stratix V
- 10 Gbps Ethernet IP Core includes MAC

```
class MovingAverageKernel extends Kernel {

    MovingAverageKernel(KernelParameters parameters) {
        super(parameters);

        // Input
        DFEVar x = io.input("x", dfeFloat(8, 24));

        DFEVar size = io.scalarInput("size", dfeUInt(32));

        // Data
        DFEVar prevOriginal = stream.offset(x, -1);
        DFEVar nextOriginal = stream.offset(x, 1);

        // Control
        DFEVar count = control.count.simpleCounter(32, size);

        DFEVar aboveLowerBound = count > 0;
        DFEVar belowUpperBound = count < size - 1;

        DFEVar withinBounds = aboveLowerBound & belowUpperBound;

        DFEVar prev = aboveLowerBound ? prevOriginal : 0;
        DFEVar next = belowUpperBound ? nextOriginal : 0;

        DFEVar divisor = withinBounds ? constant.var(dfeFloat(8, 24), 3) : 2;

        DFEVar sum = prev + x + next;
        DFEVar result = sum / divisor;

        io.output("y", result, dfeFloat(8, 24));
    }
}
```



Next steps

- Explore the possibility of the Maxeler solution
- FPGA development environment to new SHAPI standard
  - VHDL source files
  - Simulink framework
- Simulink Workshop XFEL/DESY
  - Introduce non-FPGA developers to XFEL Simulink framework



- Establishing Jenkins tool for automatic f/w image generation
- Use Redmine for FPGA development

Thank you for your attention.