A versatile MicroTCA timing system used at the European XFEL

Christoph Stechmann

4th MicroTCA Workshop for Industry and Research

9th – 10th December 2015





Agenda

Evolution of DESY LINAC timing systems

- Advantages (by using MicroTCA)
- Hardware implementation
 - NAMC-psTimer parameters
 - Timing system setup in XFEL / FLASH / REGAE
 - Rear Transition Module Types
- Software implementation
 - Example 1: Struck SIS8300 clock & trigger configuration
 - Example 2: Use for checking/verifying backplane signals



Evolution of DESY LINAC timing systems





Advantages

FPGA implementation

- configuration done through PCIe
- remotely upgradable via PCIe or IPMI
- Connection to other components through backplane
 - using PCIe CPU interrupt
 - using TCLKA/B low jitter clocks
 - using MicroTCA.4 Bus architecture clocks/triggers
- Hot-Plug capable
- Once configured it keeps running on ist own
 - CPU may be maintained/rebooted/replaced without trigger/clock interuption



NAMC-psTimer Parameters

double-width AMC (with optional RTM)

receives/transmits 1 - 1.3GHz optical timing signal via independent infrastructure

may run as receiver Stand-Alone with onboard PLL Stand-Alone with external clock

Trigger/bunch pattern/FPGA clocks outputs via

3x RJ45 front connectors (2 triggers per connector) LVDS signal level / TTL with external hardware
8x on μTCA backplane (MLVDS bus on port 17-21)
9x on optional RTM – LVDS & TTL level or optical

Low jitter clock output via

3x RJ45 front connectors TCLKA/TCLKB and crosspoint switch on MCH

flexible routing of backplane connections Rx/Tx 17–20 to FPGA and Front connectors



NAMC-psTimer

INCLES









Christoph Stechmann | A versatile MicroTCA timing system used at the European XFEL | 9th Dec 2015 | Page 6

Timing system setup in XFEL / FLASH / REGAE

Star topology

- One timing master, synchronized by Master Oscillator
 - Also connected to machine protection system
- Master oscillator clock is recovered on each receiver
- No limitation in number of receivers
 - each receiver can forward signal to another system
- Timing information is (de-)coded in onboard FPGA
 - System keeps running even when CPU/network fails
 - Timing System Specification can be implemented in user hardware design (already done by PSI)
- > Receivers can be added/removed during runtime



Rear transition module types

- > Type 1: daughter-board RTM (available)
 - Up to 9 * output of optical timing signal for other systems, cable length and drift compensated per output channel
- > Type 2: TTL Trigger RTM (available)
 - Up to 9 * TTL level trigger output on LEMO connector
 - 2 * high-precision output with rise-/fall-delay in steps of 100ps
- > Type 3: optical Trigger RTM (available)
 - Up to 9 * optical trigger output on ST connector



- Each crate contains one CPU AMC
- x2timer server running on that CPU
- > One server can manage several x2timer AMCs via PCIe
- Configurable remotely via DOOCS / Ethernet
- > x2timer hardware generates CPU interrupts that may be used for other parts of the system, e.g. sampling of ADC channel, data aquisition, etc.



Example 1: Struck ADC clk & trigger

SlaveTiming.xml XFELDIAG/TIMER/DI3011/	
Triggers & Clocks Expert Info Drift Compensation RTM MPS & Interlock BlockDiagr.	XFEL.DIAG/TIMER/DI3011/
CPU Interface Macro Pulse Number: 922483215 Error: CPU Interrupts: I Enable Delay: 200000 Rate: 100.0 ms *16 ns = 3.2ms RTM backpt. front M 0 - 12 - 12 - 12 - 12 - 12 - 12 - 12 - 1	RTM Triggers VCC 5V out Enable RTM TRG7 Trigger 0 0 s RTM TRG7 Trigger 0 0 s RTM TRG7 Trigger 0 0 s RTM TRG7 VCC 5V out Enable RTM TRG7 PGA Clock 1 0 s RTM TRG7 PGA Clock 1 0 s RTM TRG7 DC Kicker Clock 4.5Mt2 RTM TRG7 Trigger 0 0 s RTM TRG7 RTM TRG7 R
Front Triggers 0 1 2 3 Imputs 15 15 15 Imputs 16 2.735m s 0 1 Imputs 16 2.735m s 0 0 1 Imputs 16 2.735m s 0 0 0 Imputs 16 0 0 0 0 0 Imputs 0 0 0 0 0 0 0	PLL Backplane Clocks & Triggers enable Port: Backt TRGI D-Clock 108MHz 109 Mhz clock for MPS 17 T Controls Backt TRG2 Data 108MHz 108 Mhz data for MPS 17 T Backt TRG2 Data 108MHz 108 Mhz data for MPS 17 T Backt TRG2 Data 108MHz 108 Mhz data for MPS 18 R
VCC 5V out Enable FRONT.TRGS FPGA Clock 3 2.622µs FRONT.TRGS FPGA Clock 3 2.622µs Crk 2 8 4 VCC 5V out Enable FRONT.TRGS FPGA Clock 1 0 s FRONT.TRGS FPGA Clock 1 0 s Trigger for DaMon sigmaz electronics Trigger for DaMon sigmaz electronics	BACK.TRG4 Trigger 116 5.021m s 2 18 T FPGA MUX BACK.TRG5 0 19 R 19 R BP 17R BACK.TRG5 0 0 S 19 T BP 17R BACK.TRG5 19 G 0 S 19 T BACK.TRG5 Trigger 0 0 S 20 R BACK.TRG5 Trigger 0 0 S 20 T
	TcikA TcikB







Example 1: Struck ADC clk & trigger





Example 2: verify signals on backplane bus

SlaveTiming.xml XFEL.RF/TIMER/XHMT/	
Triggers & Clocks Expert Info Drift Compensation RTM MPS & Interlock BlockDiagr.	XFEL.RF/TIMER/XHM1/
CPU Interface Macro Pulse Number: 922492965 Error: Delay CPU Interrupts: Image: CPU Interrupts: Delay: 400000: The set is the	RTM Triggers VCC SV out Enable Trigger 116 4.699m s RTM.TRG Trigger Modulator A1.11 RTM.TRG Madro Pulse Number Modulator A1.11 RTM.TRG Trigger 116 5.234m s VCC SV out Enable Trigger Plate Number Modulator A1.11 fma delay VCC SV out Enable Trigger 16 373.274 µ s Trigger 16 373.274 µ s fma delay RTM.TRG Mod/Kly 115kbaud fma delay WodKly 119kbaud Madro Pulse Number RF Station Interfock GUN.11 fma delay VCC SV out Enable Madro Pulse Number RF Station Interfock GUN.11 fma delay RTM.TRG5 Trigger 16 373.274 µ s fma delay VCC SV out Enable Madro Pulse Number RF Station Interfock GUN.11 fma delay VCC SV out Enable Madro Pulse Number Modulator GUN.11 fma delay Mod/Kly 115kbaud fma delay fma delay Mod/Kly 115kbaud fma delay fma delay Macro Pulse Number Modulator GUN.11 fma delay fma delay
Front Triggers VCC 5V out Enable PRONT.TRGS Trigger 0 0 s FRONT.TRGS Trigger 0 0 s Clk 3 1 T	Trigger 116 4.074m s Trigger RF Station Interlock GUN11 Backplane Clocks & Triggers enable Port: Backtregi 0 0 17 R Backtregi 0 0 17 T Backtregi 0 0 18 R
VCC 5V out Enable FRONT.TRG Trigger 0 0 0 s not connected FRONT.TRG Trigger 0 0 0 s not connected FRONT.TRG Trigger 0 0 0 s not connected FRONT.TRG Trigger 16 0 s not connected 1 v	BACKTRGA Trigger 0 0 s 18 T Propriet BACKTRGA Trigger 0 0 S 19 R 19 R BACKTRGS Trigger 0 0 S 19 R BACKTRGS Trigger 0 0 S 19 R BACKTRGS Trigger 0 0 S 20 R BACKTRGS Trigger 0 0 S 20 T

