A versatile MicroTCA timing system used at the European XFEL

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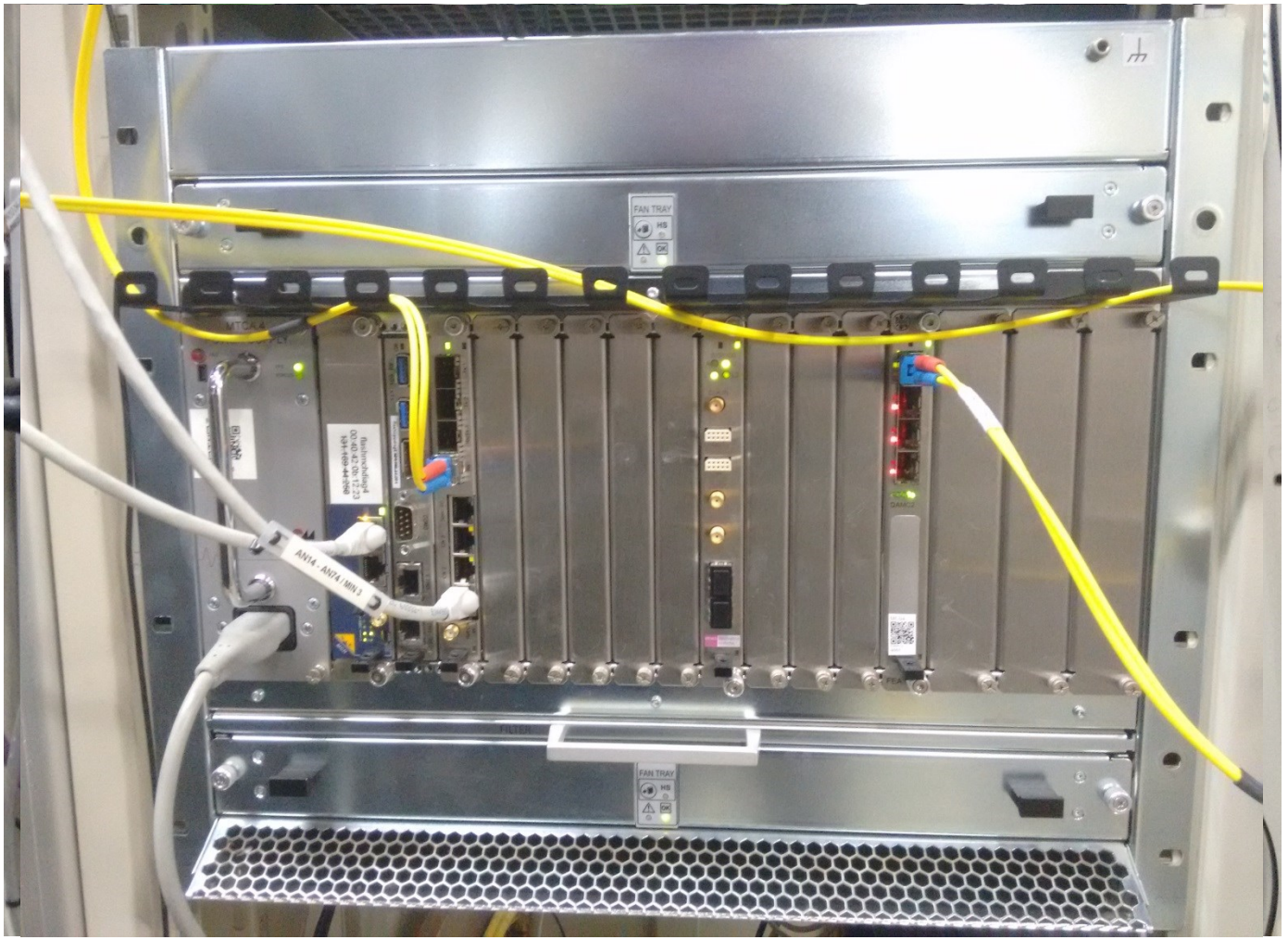
HELMHOLTZ ASSOCIATION

DESY

Agenda

- Evolution of DESY LINAC timing systems
  - Advantages (by using MicroTCA)
- Hardware implementation
  - NAMC-psTimer parameters
  - Timing system setup in XFEL / FLASH / REGAE
  - Rear Transition Module Types
- Software implementation
  - Example 1: Struck SIS8300 clock & trigger configuration
  - Example 2: Use for checking/verifying backplane signals

Evolution of DESY LINAC timing systems



Advantages

- FPGA implementation
  - configuration done through PCIe
  - remotely upgradable via PCIe or IPMI
- Connection to other components through backplane
  - using PCIe - CPU interrupt
  - using TCLKA/B – low jitter clocks
  - using MicroTCA.4 Bus architecture – clocks/triggers
- Hot-Plug capable
- Once configured it keeps running on ist own
  - CPU may be maintained/rebooted/replaced without trigger/clock interuption

NAMC-psTimer Parameters

- double-width AMC (with optional RTM)
  - receives/transmits 1 - 1.3GHz optical timing signal via independant infrastructure

    may run as
    receiver
    Stand-Alone with onboard PLL
    Stand-Alone with external clock

  - Trigger/bunch pattern/FPGA clocks outputs via

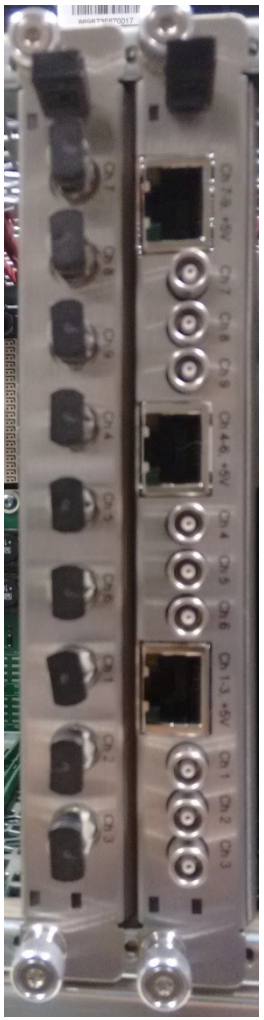
    3x RJ45 front connectors (2 triggers per connector)
    LVDS signal level / TTL with external hardware
    8x on µTCA backplane (MLVDS bus on port 17-21)
    9x on optional RTM – LVDS & TTL level or optical

  - Low jitter clock output via

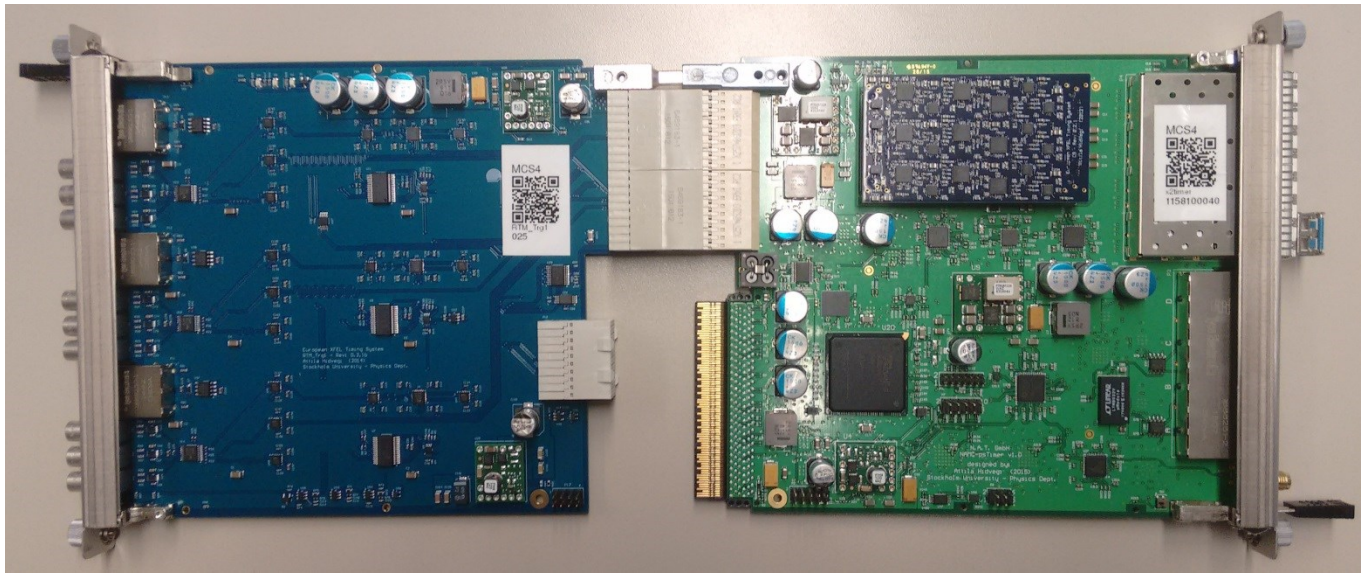
    3x RJ45 front connectors
    TCLKA/TCLKB and crosspoint switch on MCH

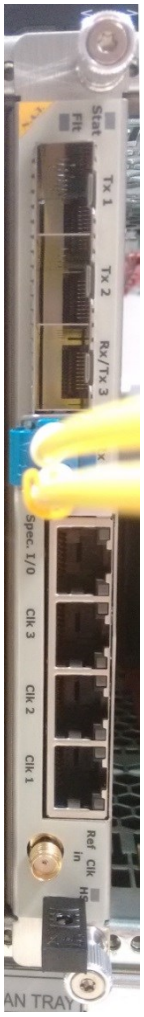
  - flexible routing of backplane connections Rx/Tx 17–20 to FPGA and Front connectors

NAMC-psTimer



RTM AMC





Timing system setup in XFEL / FLASH / REGAE

- Star topology
- One timing master, synchronized by Master Oscillator
  - Also connected to machine protection system
- Master oscillator clock is recovered on each receiver
- No limitation in number of receivers
  - each receiver can forward signal to another system
- Timing information is (de-)coded in onboard FPGA
  - System keeps running even when CPU/network fails
  - Timing System Specification can be implemented in user hardware design (already done by PSI)
- Receivers can be added/removed during runtime

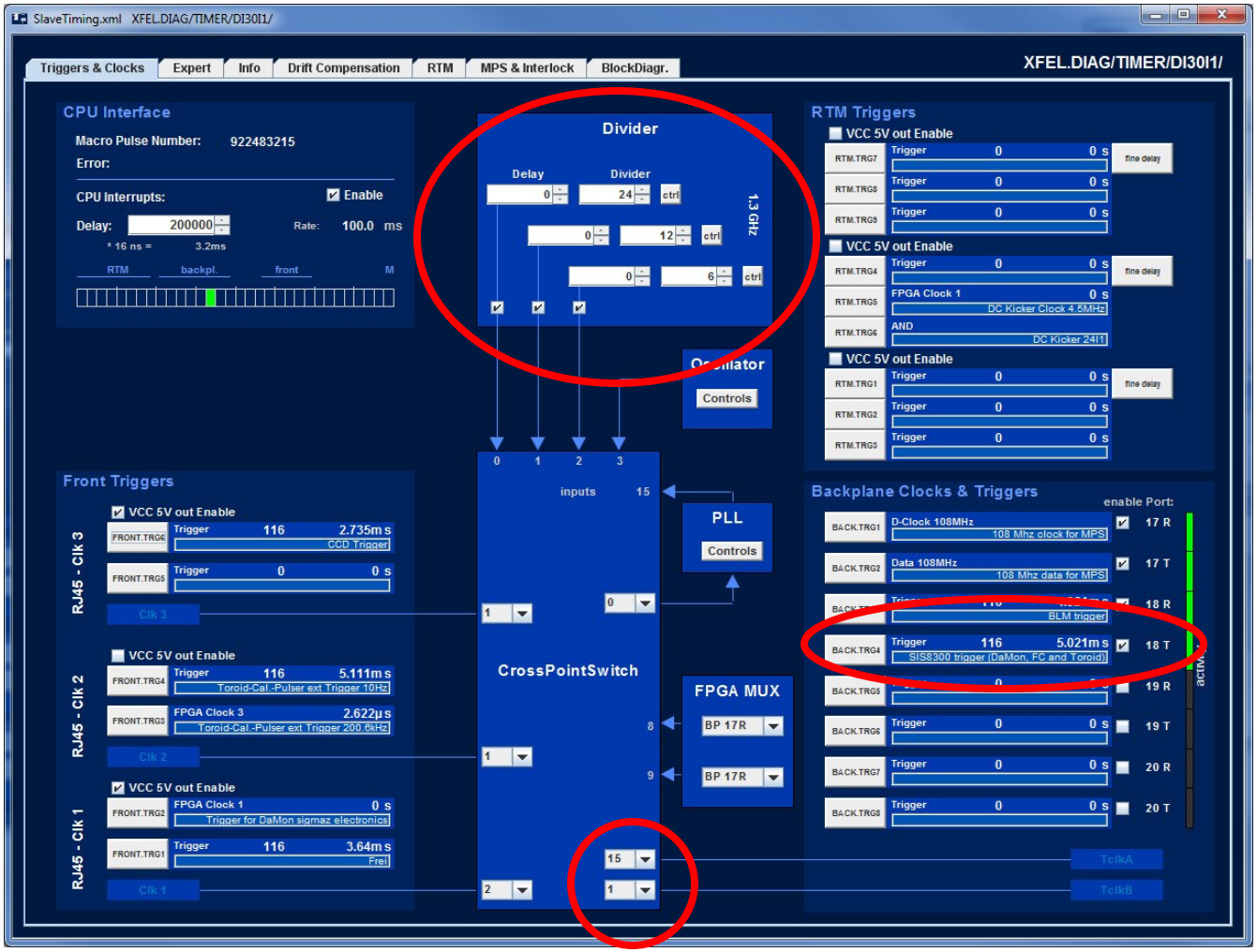
Rear transition module types

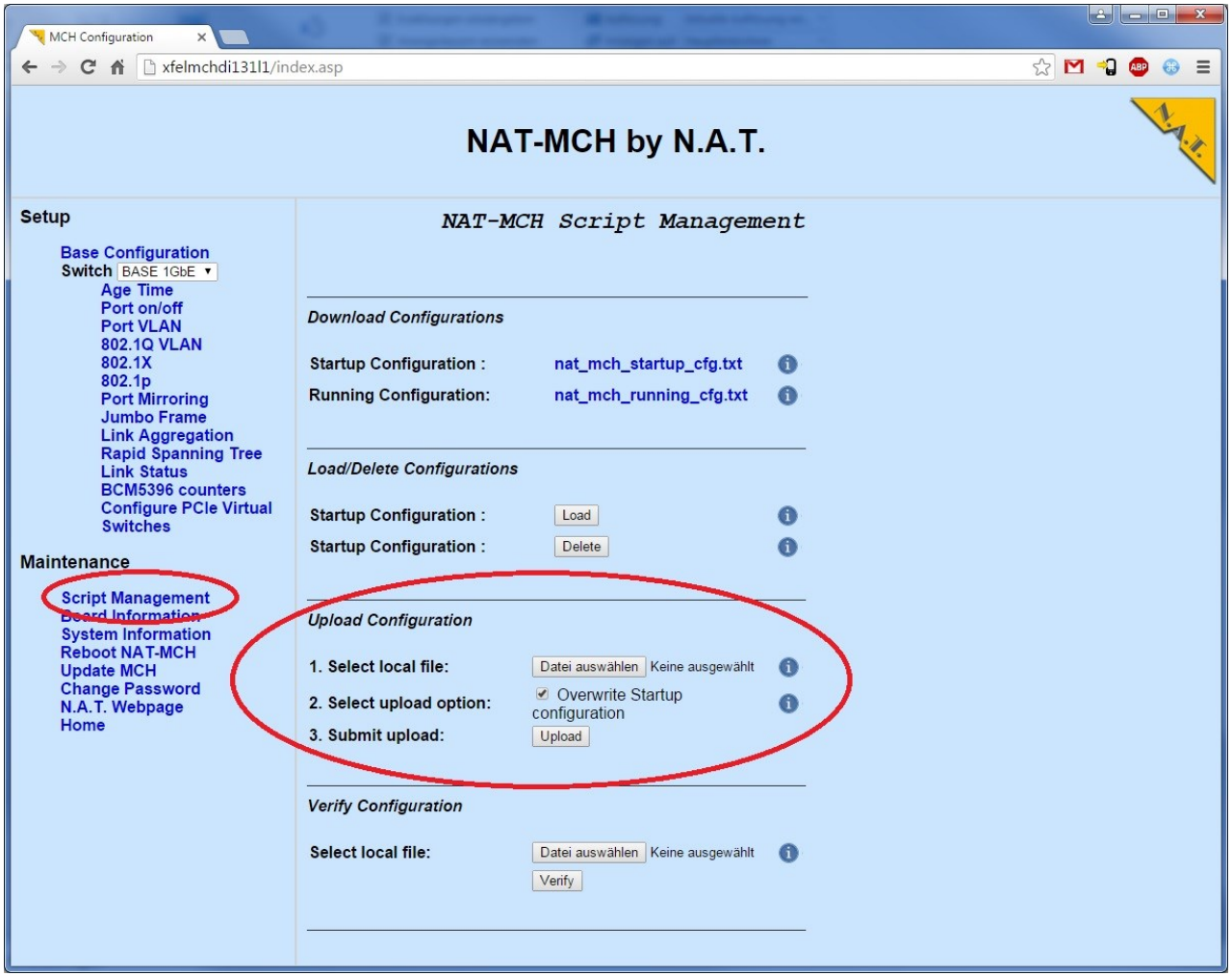
- Type 1: daughter-board RTM (available)
  - Up to 9 * output of optical timing signal for other systems, cable length and drift compensated per output channel
- Type 2: TTL Trigger RTM (available)
  - Up to 9 * TTL level trigger output on LEMO connector
  - 2 * high-precision output with rise-/fall-delay in steps of 100ps
- Type 3: optical Trigger RTM (available)
  - Up to 9 * optical trigger output on ST connector

Software implementation

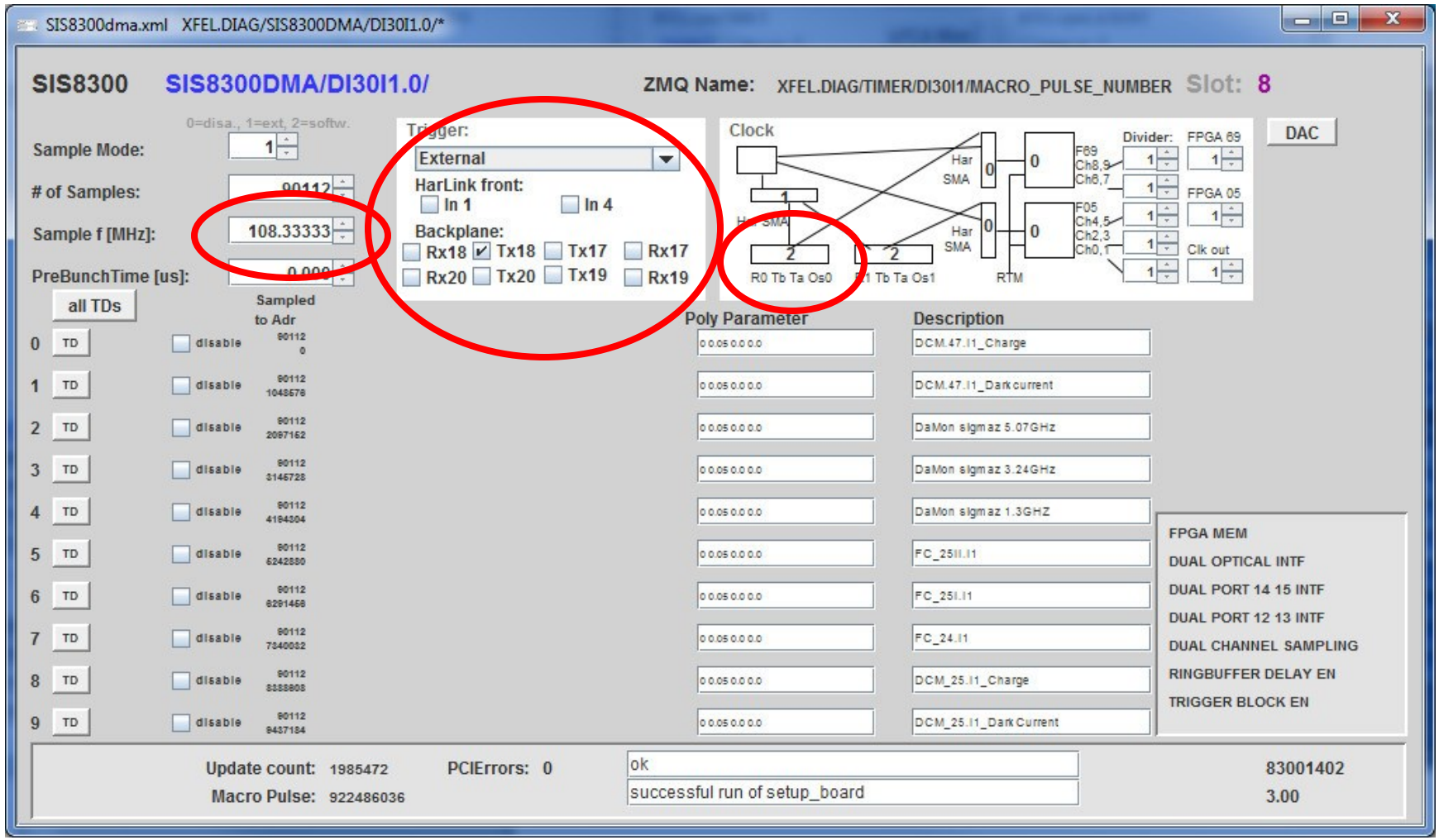
- Each crate contains one CPU AMC
- x2timer server running on that CPU
- One server can manage several x2timer AMCs via PCIe
- Configurable remotely via DOOCS / Ethernet
- x2timer hardware generates CPU interrupts that may be used for other parts of the system, e.g. sampling of ADC channel, data aquisition, etc.

Example 1: Struck ADC clk & trigger




MCH Configuration
xfelmchdi131l1/index.asp
NAT-MCH by N.A.T.
Setup
Base Configuration
Switch BASE 1GbE
Age Time
Port on/off
Port VLAN
802.1Q VLAN
802.1X
802.1p
Port Mirroring
Jumbo Frame
Link Aggregation
Rapid Spanning Tree
Link Status
BCM5396 counters
Configure PCIe Virtual Switches
Maintenance
Script Management
Board Information
System Information
Reboot NAT-MCH
Update MCH
Change Password
N.A.T. Webpage
Home
NAT-MCH Script Management
Download Configurations
Startup Configuration : nat_mch_startup_cfg.txt
Running Configuration: nat_mch_running_cfg.txt
Load/Delete Configurations
Startup Configuration : Load
Startup Configuration : Delete
Upload Configuration
1. Select local file: Datei auswählen Keine ausgewählt
2. Select upload option: Overwrite Startup configuration
3. Submit upload: Upload
Verify Configuration
Select local file: Datei auswählen Keine ausgewählt
Verify

Example 1: Struck ADC clk & trigger



Example 2: verify signals on backplane bus