RTM Modules for waveform digitization

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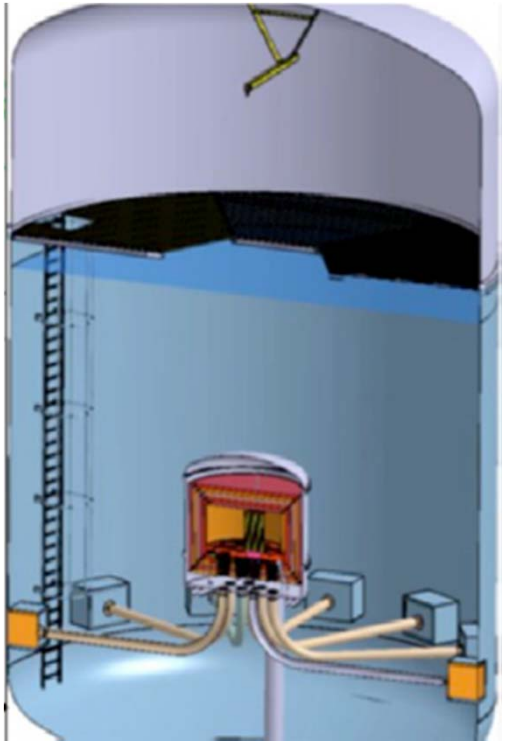
EURECA **Muon Veto**



- About 100 8-inch PMTs total
- Coincidence trigger on groups of PMTs
- PMT signals are recorded with high time resolution
- a few hundreds ns waveform length
- zero dead time

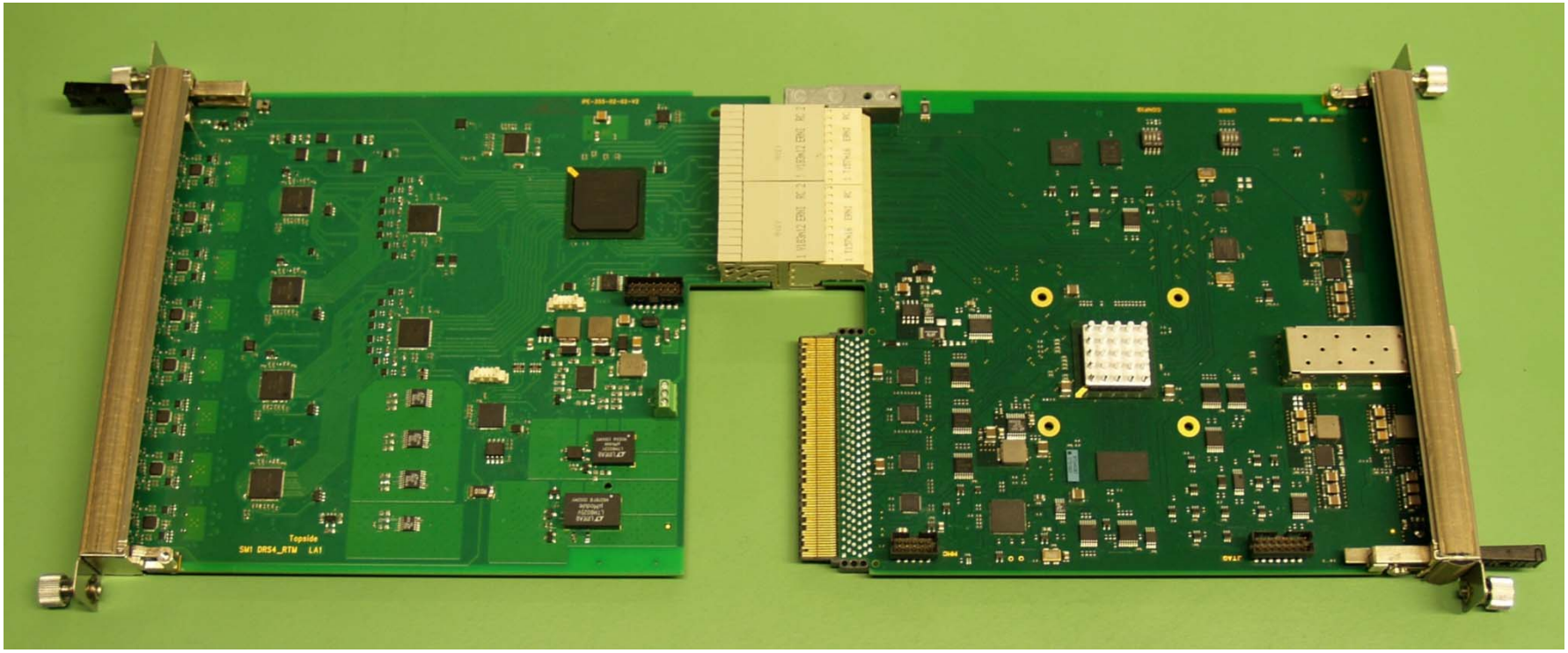
The water tank will be the shielding for any neutron and gamma activity and will act as an active shield for cosmic muons.

DRS4-RTM

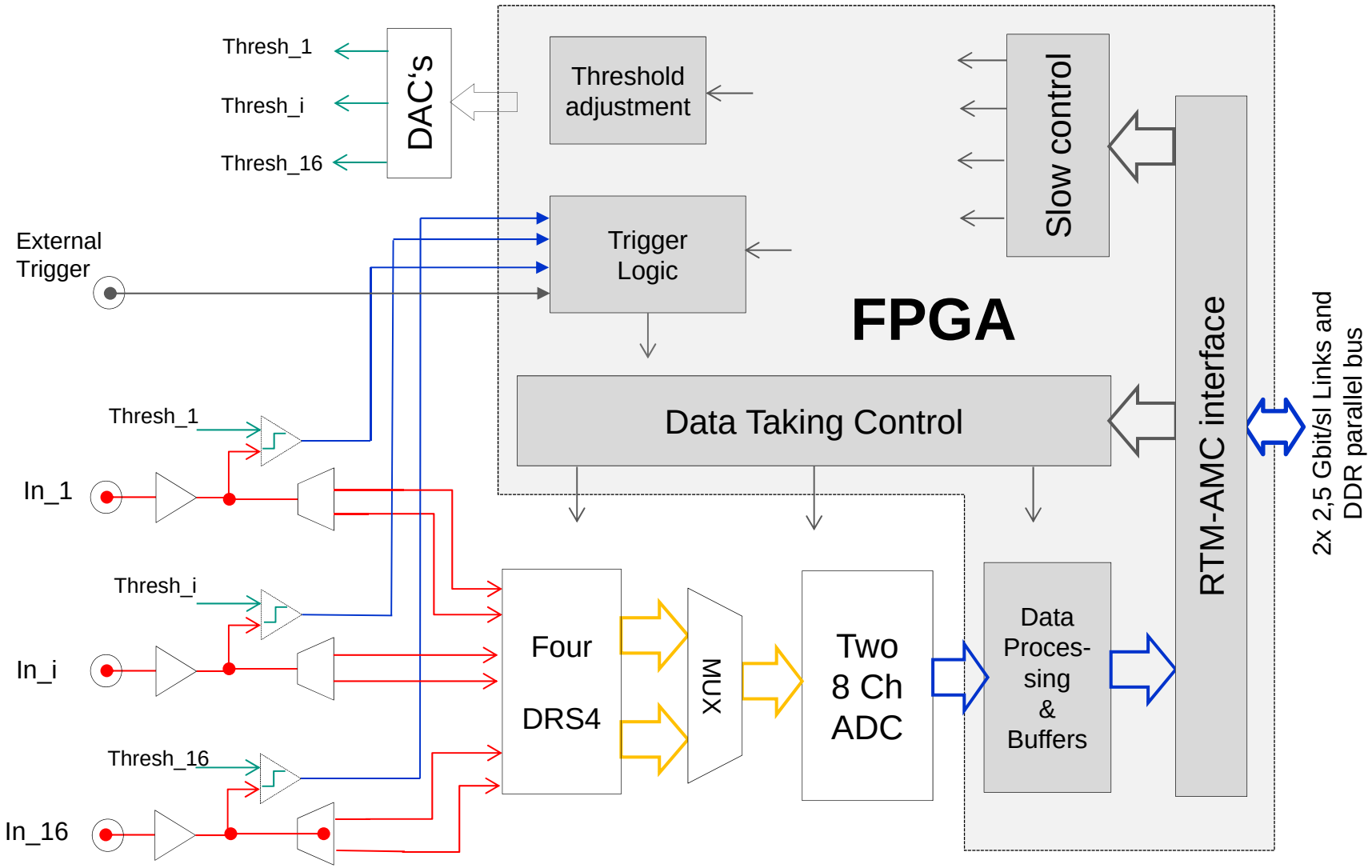
- 16 channels
- 0,7 .. 5 GHz sampling rate
- 12-bit digitization
- 1024 samples
- Self triggering

TAMC651

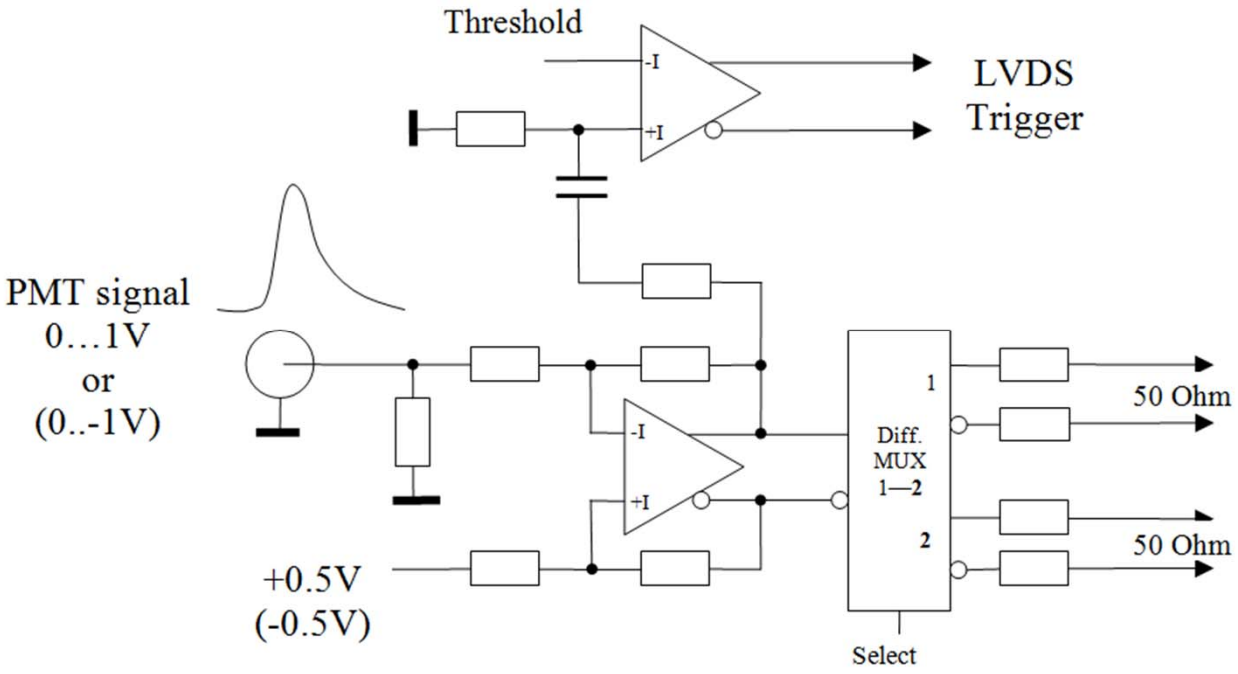
- FPGA
- SDRAM 128MB
- Gbit links to RTM
- PCIe

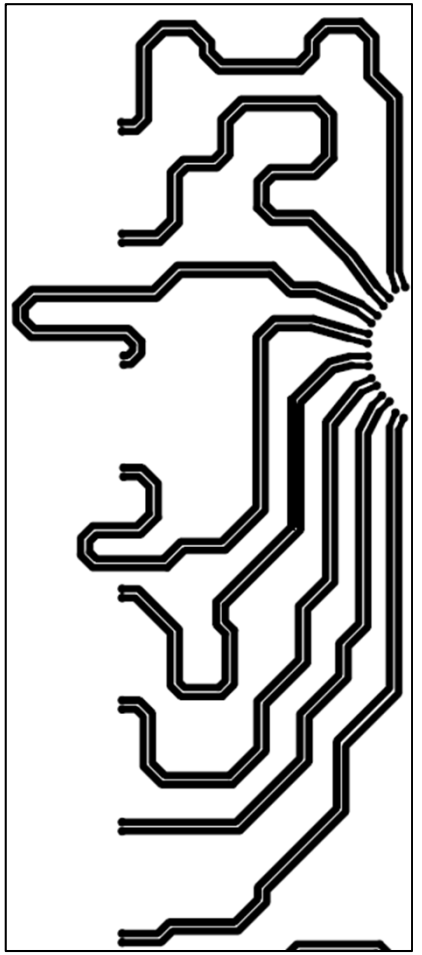


Block diagramm of the DRS4-RTM module



Analog Front End

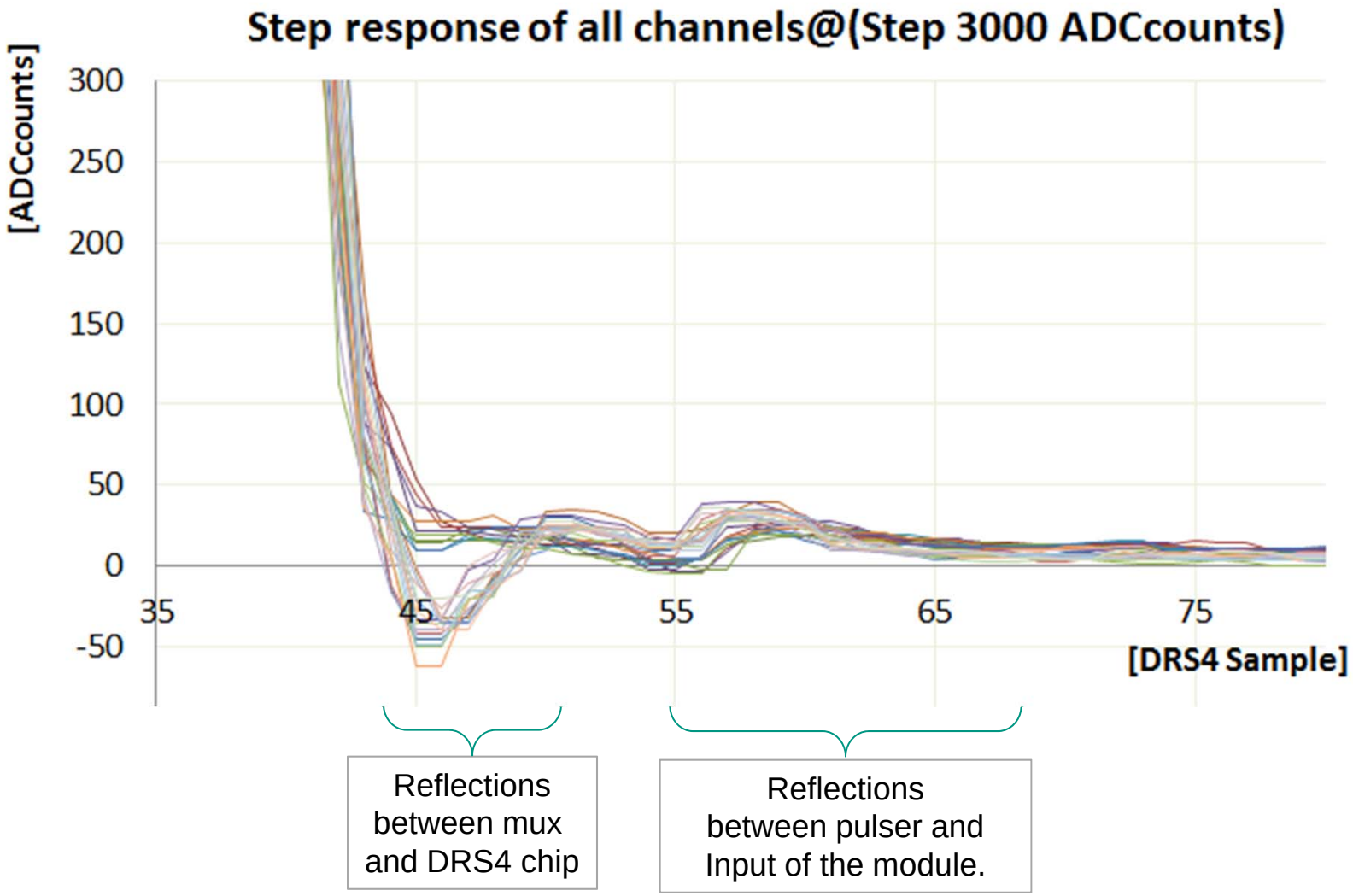




DRS4
Inputs

Transmission lines implemented
in an inner layer of PCB

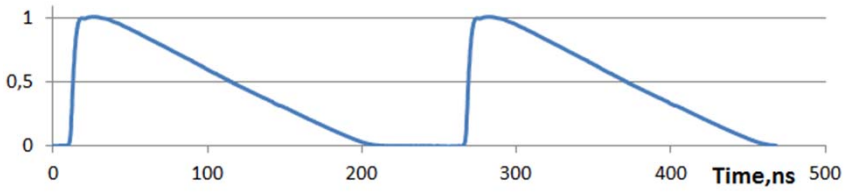
Distortion of signal edge (reflections ~1%).

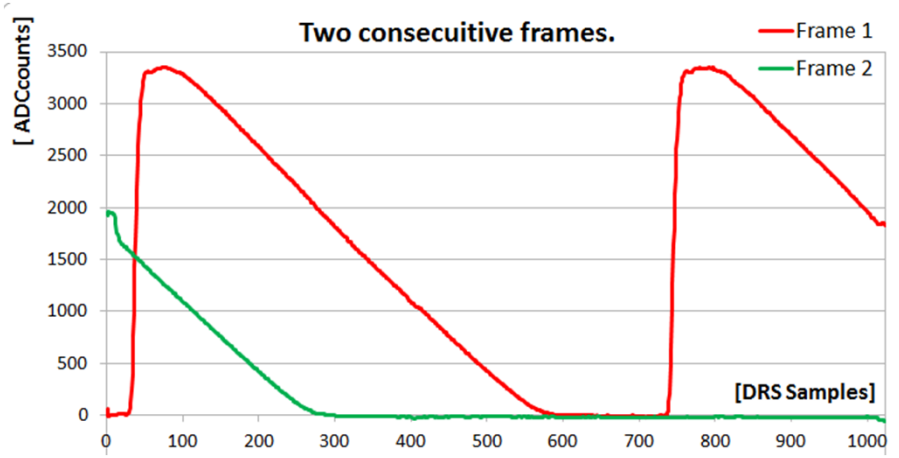


Dead time measurement.

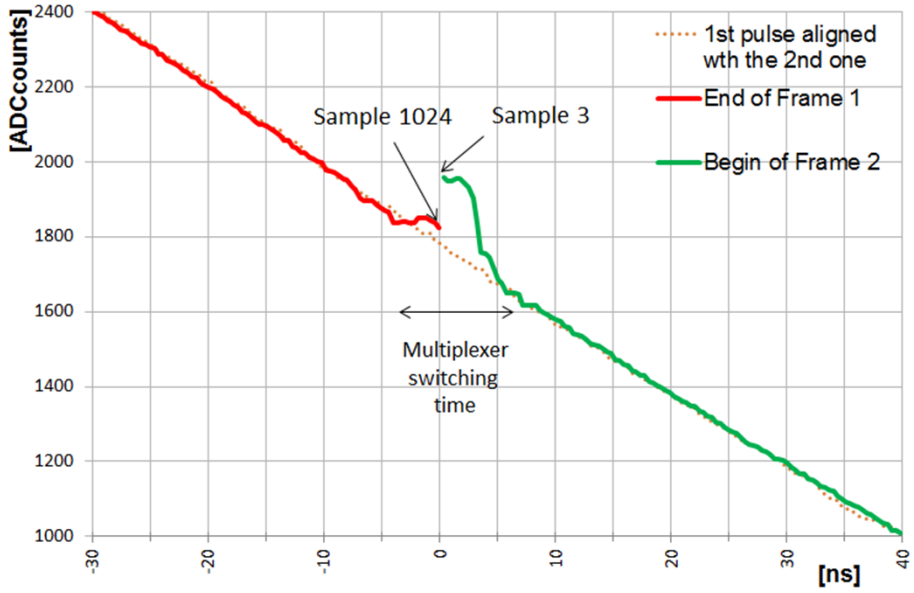
Dead time arises due to delays of analog miltiplexer in front of DRS4 chips.
Double saw pulse of total length 450ns is used.
DRS-4 frame is 371ns (sampling rate 2,76 GHz).

Dead time is about 10 ns



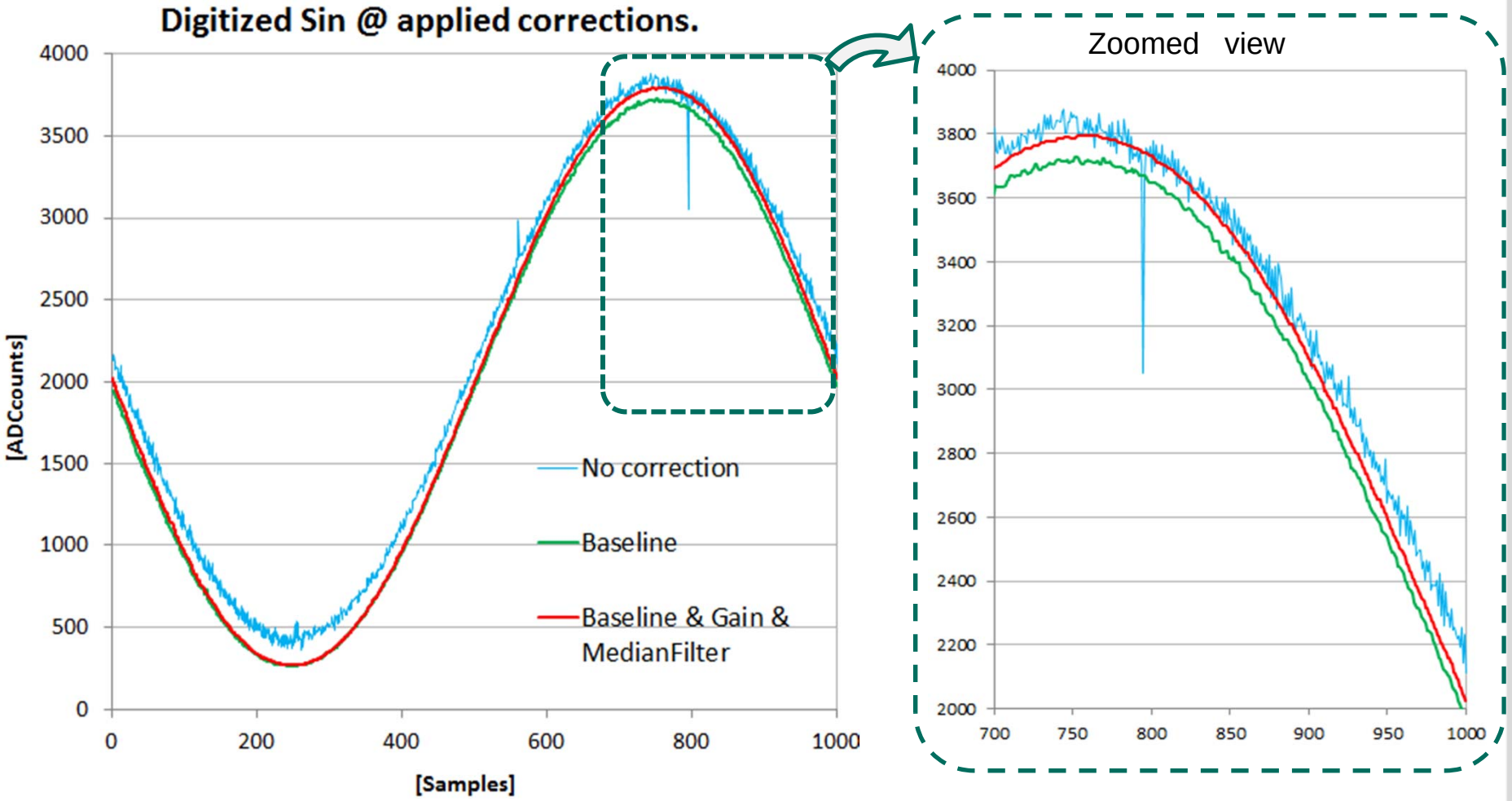


Saw pulses sampled in two consecuitive frames.

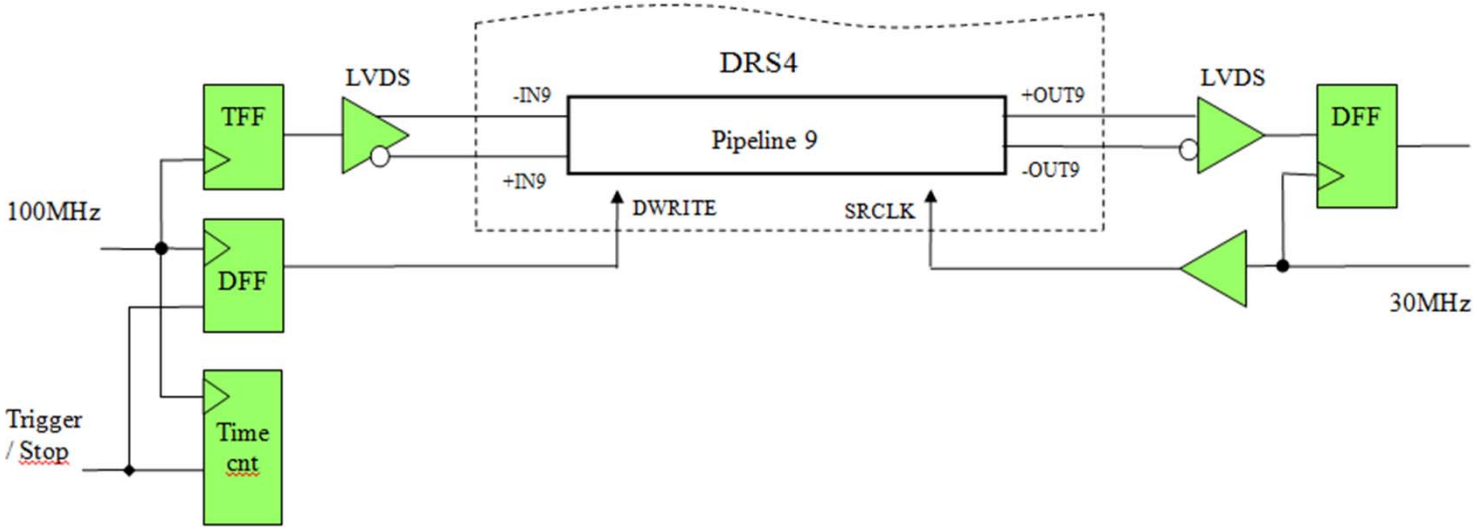


Corrections for Offset and Gain Nonuniformity.

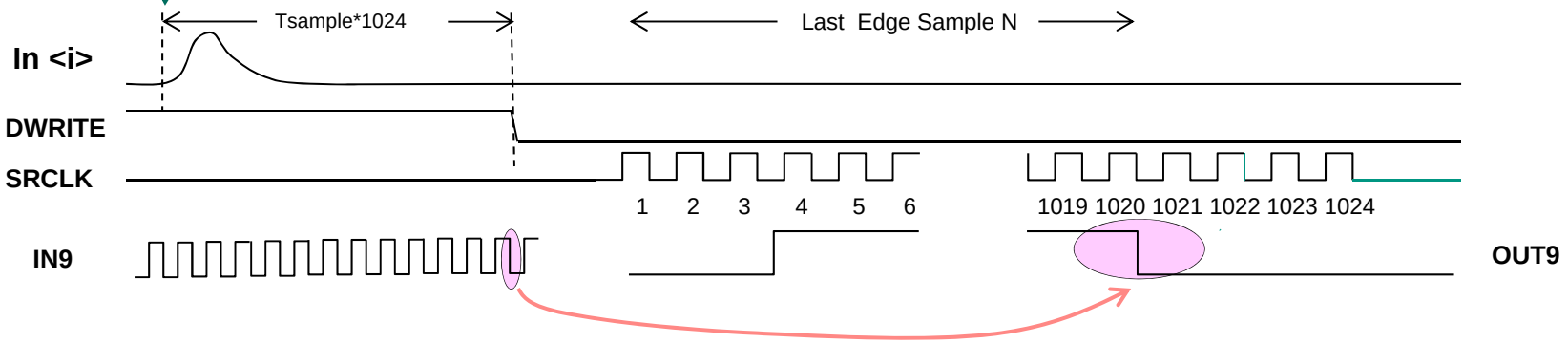
Residual nois after all corrections ~3 ADCcounts (rms).



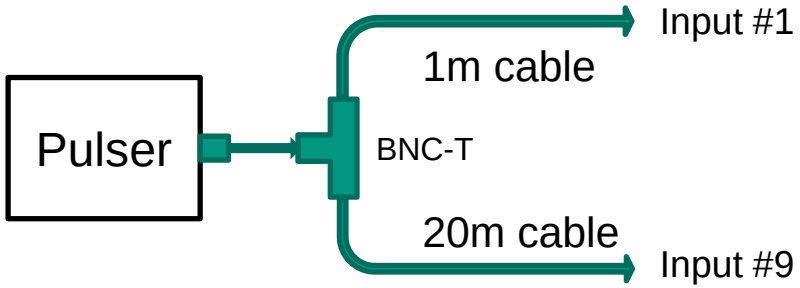
Timing of Digitized Waveform.

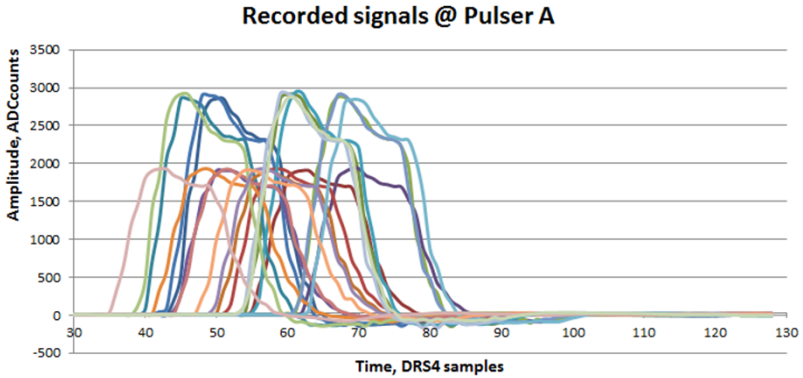


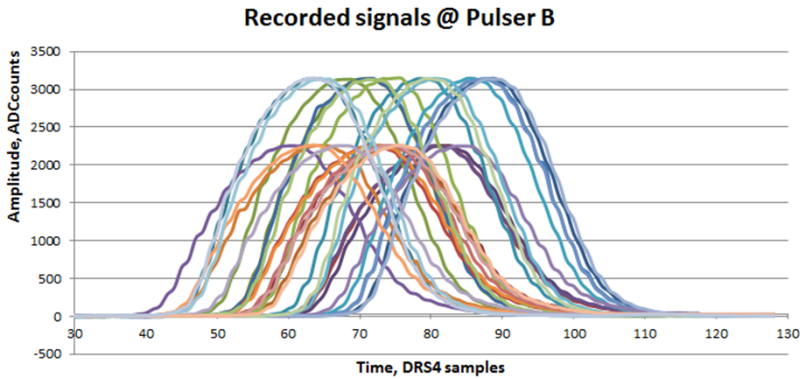
Time of Frame = (Time_Stamp) * 10ns – N * Sampling_Period



Timing Accuracy.







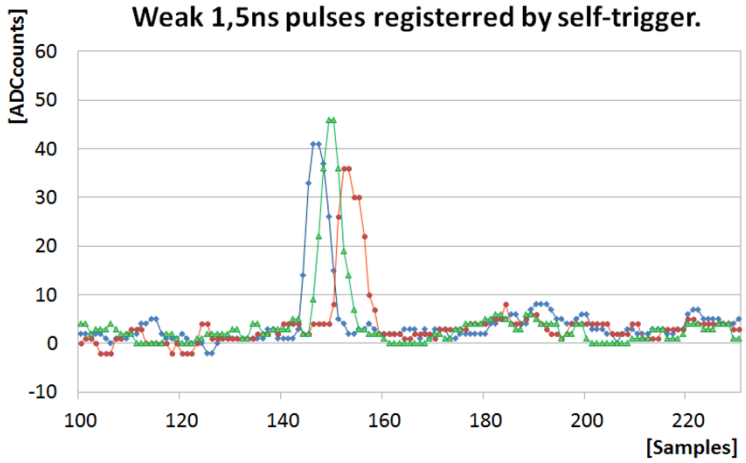
- Delay is specified by length of the cables
- Signals are fed to channels served by different DRS4 chips
- Individual self-triggering of the channels
- Two different pulsers were used
- Center of mass of the signals was calculated

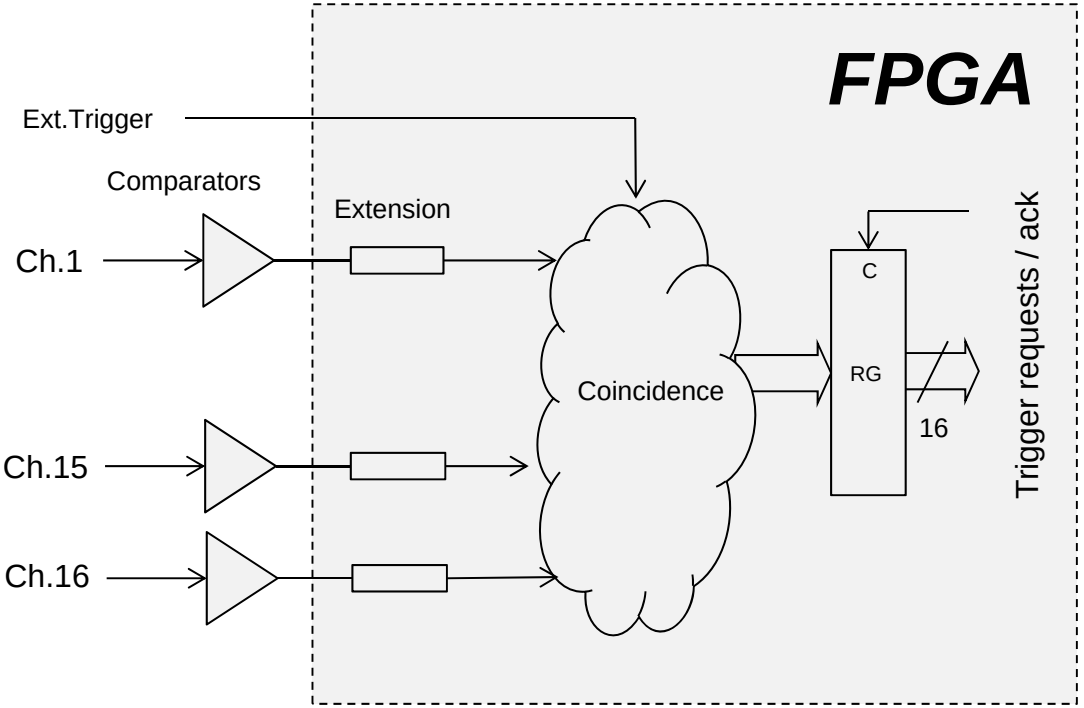
Delay @ 1m and 20m Cables
2,7GHz sampling rate

	Mean	**RMS error**
Pulser A	83,95 ns	**0,40 ns**
Pulser B	84,28 ns	**0,45 ns**

Trigger.

- Fast comparators with small hysteresis (3mV)
- Automatic threshold adjustment
- Trigger sensitivity ~10mV
- FPGA logic available for coincidence trigger logic
- Triggerred channels are read out





Zone3 Connector of the DRS4-RTM

Pinout is compatible to following AMC modules:

- **HGF-AMC**
- **TAMC651 (from TEWS)**

		A	B	C	D	E	F
J30	1	RTM_PWR	RTM_PWR	RTM_PS#	RTM_SDA	RTM_TCK	RTM_TDO
	2	RTM_PWR	RTM_PWR	RTM_MP	RTM_SCL	RTM_TDI	RTM_TMS
	3	CLK0_A2R+	CLK0_A2R-	CLK0_R2A+	CLK0_R2A-		
	4					B2	B2
	5	B2_cc	B2_cc	B2_cc	B2_cc	B2_cc	B2_cc
	6	B2	B2	B2	B2	B2	B2
	7	BR	B2	B2	B2	B2	B2
	8	BR	B2	B2	B2	B2	B2
	9	B2	B2	B2	B2	B2	B2
	10	B2	B2	B2	B2	B2_cc	B2_cc
J31	1	B1	B1	B1	B1	B1_cc	B1_cc
	2	B1	B1	B1	B1	B1_cc	B1_cc
	3	B1	B1	B1	B1	B1	B1
	4	B1	B1	B1	B1	B1	B1
	5	B1	B1	B1	B1	B1	B1
	6	B1	B1	B1	B1	B1	B1
	7						
	8						
	9	RCLK2_R2A+	RCLK2_R2A-	GL2_R2A+	GL2_R2A-	GL2_A2R+	GL2_A2R-
	10	RCLK1_R2A+	RCLK1_R2A-	GL1_R2A+	GL1_R2A-	GL1_A2R+	GL1_A2R-

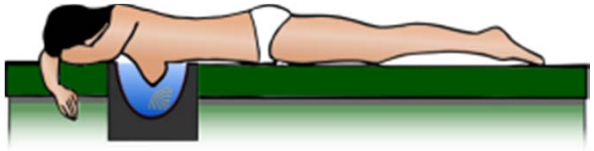
	LVDS or LVCMOS2V5 input/output
	LVDS input or LVCMOS input/output
	LVCMOS2V5 input/output

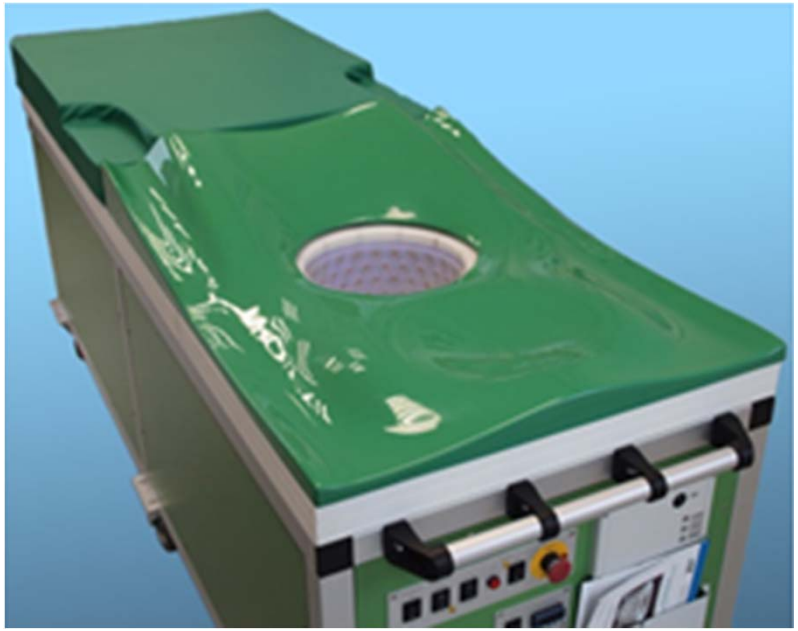
Key figures of the DRS4-RTM module.

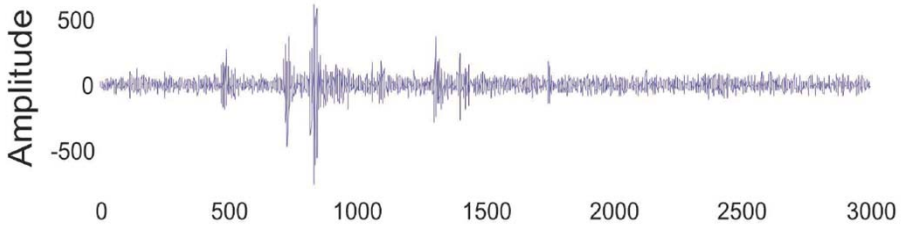
- 16 simultaneously digitized signals
- Input range (0..1V) or (-1V..0) or (-0,5V..+0,5V)
- 0,7 to 5 GHz sampling rate
- 12 bit digitization
- Bandwidth 300 MHz
- time error about one sampling period (rms)
- Noise level, 3 ADCcounts,
- 10 ns dead time
- Minimum signal amplitude of discriminators 10 mV
- data transfer rate
  - 480 MSample/s ADC to FIFO‘s
  - 125 MSamples/s per lane RTM to AMC board
- PCIe DMA transfer rate ~120MB/s

USCT

Karlsruher Institut für Technologie







MTCA.4 based DAQ requirements

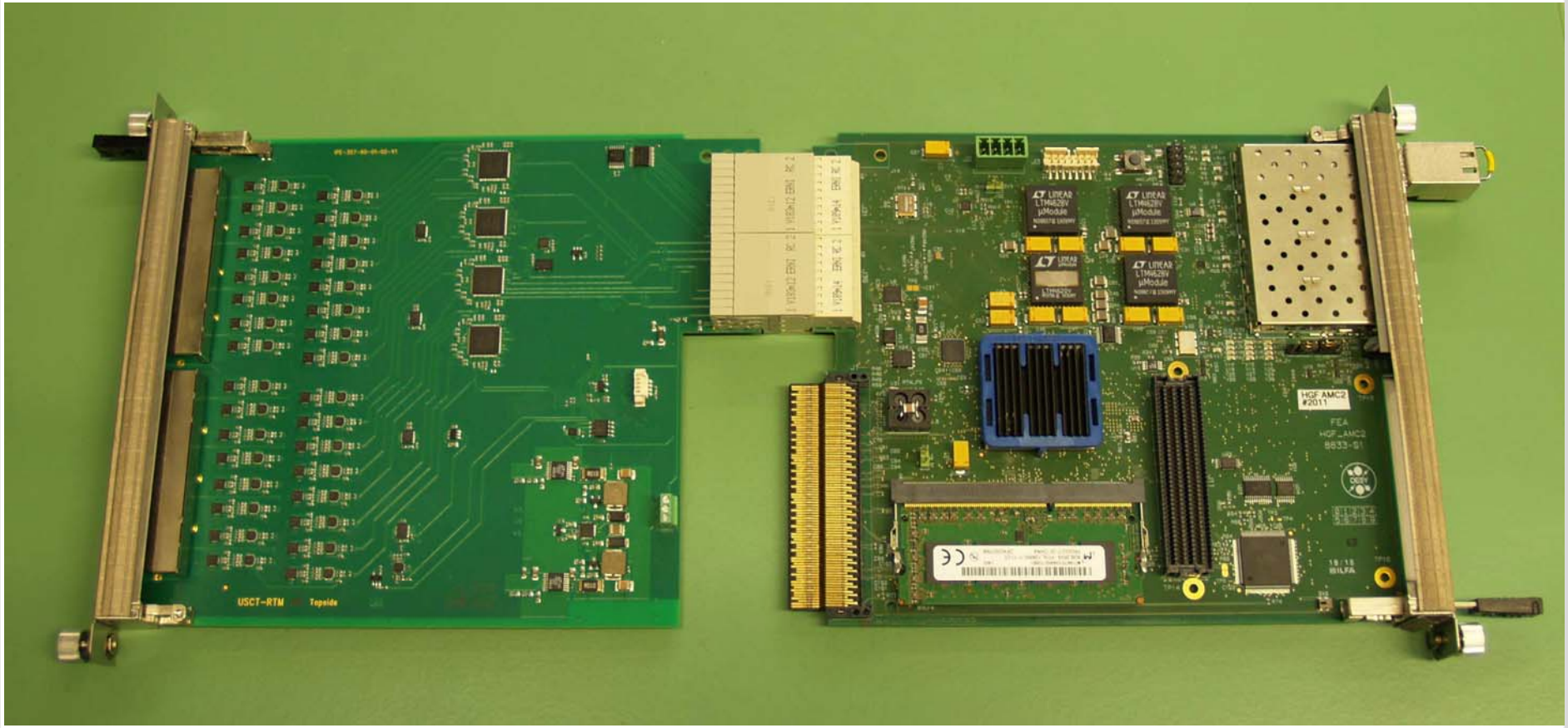
- waveform length 300us
- sampling rate 10 … 20MHz
- 384 digitization channels

ADC32-RTM

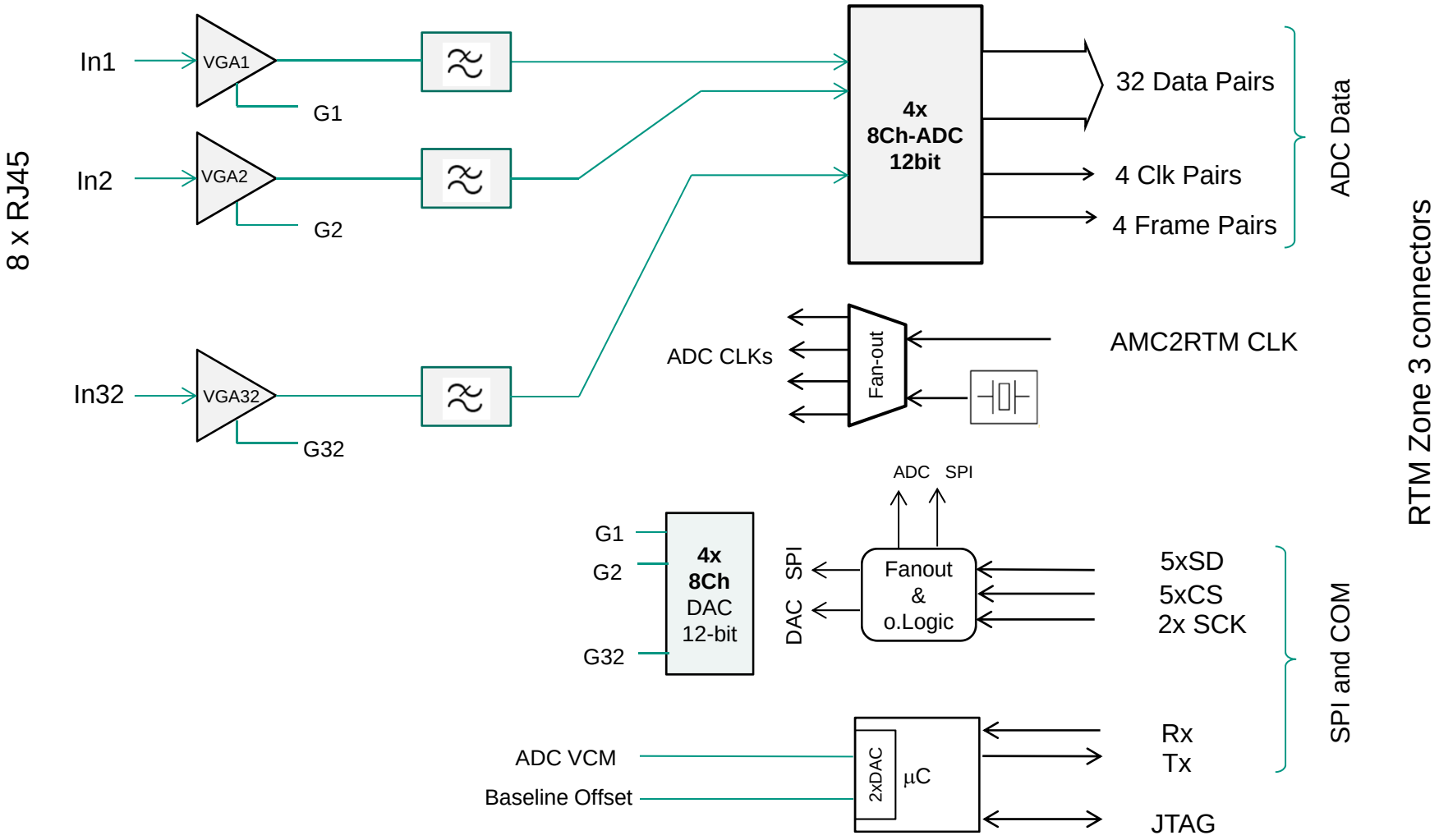
- 32 channels
- 12 bit @ 10..40 Mhz
- VGA 0..40 dB
- 5th order antializing filter

HGF-AMC

- Kintex-7
- 4x lanes PCIe
- 4x SFP+
- SODIMM 8GB
- FMC slot



Block Scheme of ADC32-RTM



Zone3 Connector of the ADC32-RTM

Pinout is compatible to **HGF-AMC**

		A	B	C	D	E	F
J30	1	RTM_PWR	RTM_PWR	RTM_PS#	RTM_SDA	RTM_TCK	RTM_TDO
	2	RTM_PWR	RTM_PWR	RTM_MP	RTM_SCL	RTM_TDI	RTM_TMS
	3	**CLK0_A2R+**	**CLK0_A2R-**			ADC3_08p	ADC3_08n
	4	COM_RX	COM_TX			ADC3_07p	ADC3_07n
	5	ADC4_07p	ADC4_07n	ADC4_08p	ADC4_08n	ADC3_06p	ADC3_06n
	6	ADC4_05p	ADC4_05n	ADC4_06p	ADC4_06n	ADC3_05p	ADC3_05n
	7	**ADC4_DCOp**	**ADC4_DCOn**	ADC4_04p	ADC4_04n	ADC3_04p	ADC2_03n
	8	ADC4_03p	ADC4_03n	ADC3_02p	ADC3_02n	ADC3_03p	ADC3_03n
	9	ADC4_01p	ADC4_01n	ADC4_02p	ADC4_02n	**ADC3_DCOp**	**ADC3_DCOn**
	10	**ADC4_FCOp**	**ADC4_FCOn**	ADC3_01p	ADC3_01n	**ADC3_FCOp**	**ADC3_FCOn**
J31	1	ADC2_07p	ADC2_07n	ADC2_08p	ADC2_08n	**ADC1_FCOp**	**ADC1_FCOn**
	2		ADC_SCK	ADC2_06p	ADC2_06n	DAC3_SD	DAC4_SD
	3	**ADC2_FCOp**	**ADC2_FCOn**	ADC_SD	ADC_CS	**ADC1_DCOp**	**ADC1_DCOn**
	4	ADC2_05p	ADC2_05n	ADC1_08p	ADC1_08n	DAC3_CS	DAC4_CS
	5	ADC2_03p	ADC2_03n	ADC2_04p	ADC2_04n	DAC_SC	
	6	**ADC2_DCOp**	**ADC2_DCOn**	ADC1_07p	ADC1_07n	DAC1_CS	DAC2_CS
	7	ADC2_02p	ADC2_02n	ADC1_05p	ADC1_05n	ADC1_06p	ADC1_06n
	8	ADC2_01p	ADC2_01n	ADC1_04p	ADC1_04n	DAC2_SD	DAC1_SD
	9					ADC1_03p	ADC1_03n
	10			ADC1_01p	ADC1_01n	ADC1_02p	ADC1_02n

Key figures of the ADC32-RTM module

- 32 differential inputs
- VGA gain 0 dB to 40 dB
- 12-bit digitization
- Sampling rate 10 to 40 MHz
- Noise level 0,8 LSB @ 0 dB, 2 LSB @ 20 dB, 5 LSB @ 40 dB (4 MHz filter)
- 5th order antialiazing filter 3 to 10MHz (assembling options)