New developments and designs for MTCA.4

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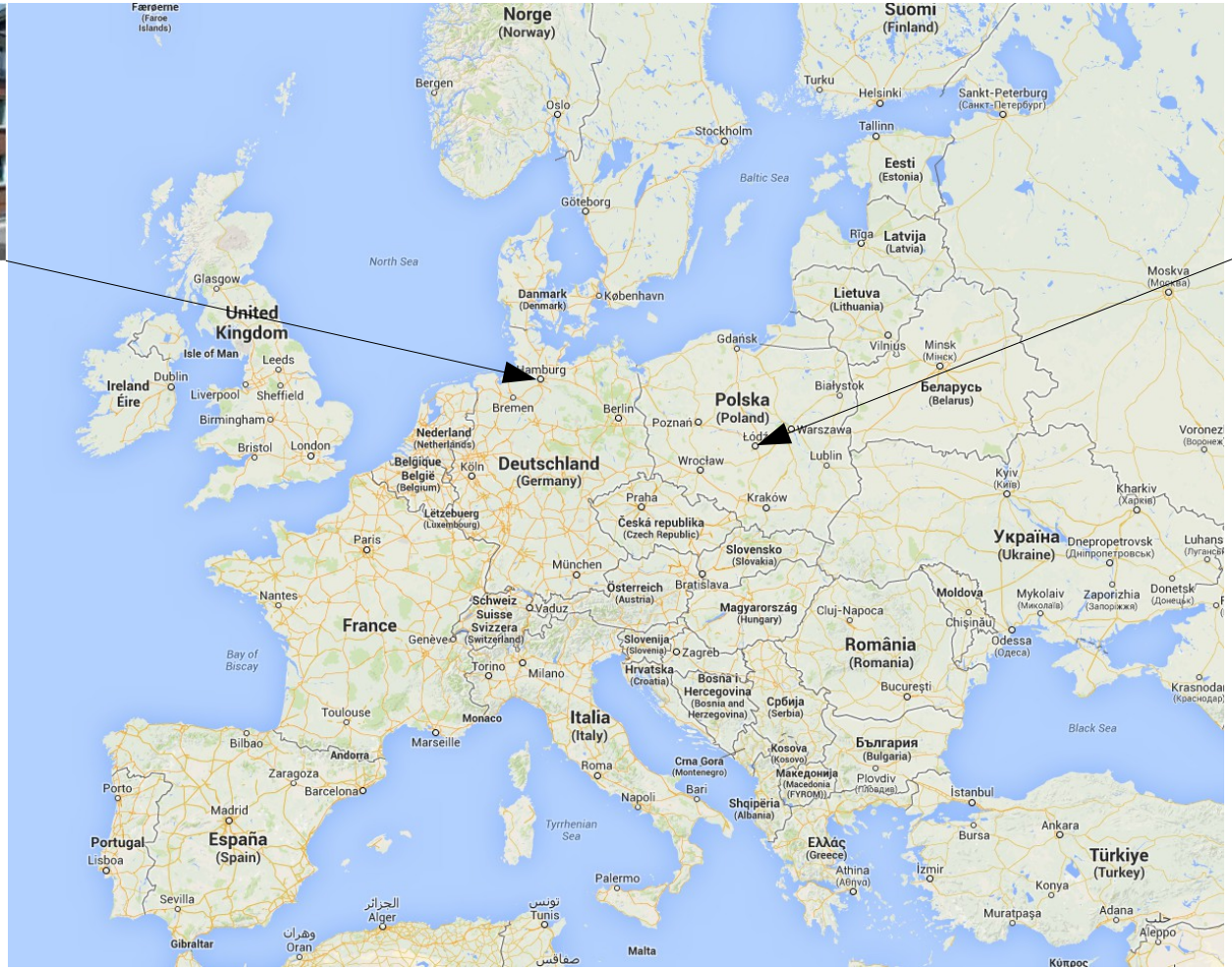

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Outlook

- Company profile
- Integrated systems
- Hardware development
- Software / firmware development

Company profile

Hardware Development:

- MTCA.4 boards
- ATCA boards
- Custom boards

Firmware/Software Development:

- FPGA firmware development based on VHDL and Verilog
- Drivers for Linux and Windows
- Platforms: PC, DSP, uC, ARM, SoC

Control Systems

- EPICS, DOOCS, LabView

System Integration

- Out of the box solutions and starter kits

Trainings

Company profile
Customers – scientific institutes

- CERN
- DESY, Germany
- SLAC National Accelerator Laboratory, USA
- RIKEN, Japan
- Oak Ridge National Laboratory, USA
- The University of Texas – Arlington, USA
- ITER, France
- IHEP, China
- MPI, Germany
- ESS, Sweden
- KIT, Germany
- UPV Valencia
- IFIN-HH Bucharest

Integrated Systems

The COTS delivered by different vendors are not always compatible to each other and can create a lot of problems. Based on our experience we can provide solutions to this problems.

We offer integrated systems in the following form factors:

- *MTCA.4*
- *ATCA*
- *PXIe*

Based on customer specification we help with component selection, installation and tests.

Integrated Systems
mTCA.4 - 1U

Main features:

- 2 x mTCA.4 slots (with RTM)
- 1 x AMC.1 slot (for CPU usage)
- PCIe operation without CPU (external uplink)
- Possibility to add RF back-plane
- Power supply (redundant)+cooling units
- Management board compatible with base MCH pin-out
- Configurable back-plane interconnections (all ports on mTCA.4 boards can be used)

Integrated Systems
mTCA.4 – startup kit

- Tested, ready to use DAQ system
- Configured OS (Linux), RT extension on request
- Linux drivers
- EPICS
- Set of application examples

User can modify / add functionality

Hardware Development

In our offer we have several boards developed based on requirements from different customers. We sell them as COTS as well as offer modifications if needed.

In addition to in-house developed hardware we are offering the hardware based on licenses provided by DESY and CERN.

Hardware Development

AMC/RTM

- EAMC-D102
- ERTM-D102
- EAMC-FMC400
- EAMC-FMC500 (DESY)
- EAMC-FMC270
- EAMC-TIM1
- ERTM-RFI8
- ERTM-PTZ4 (DESY planned)

FMC Mezzanines

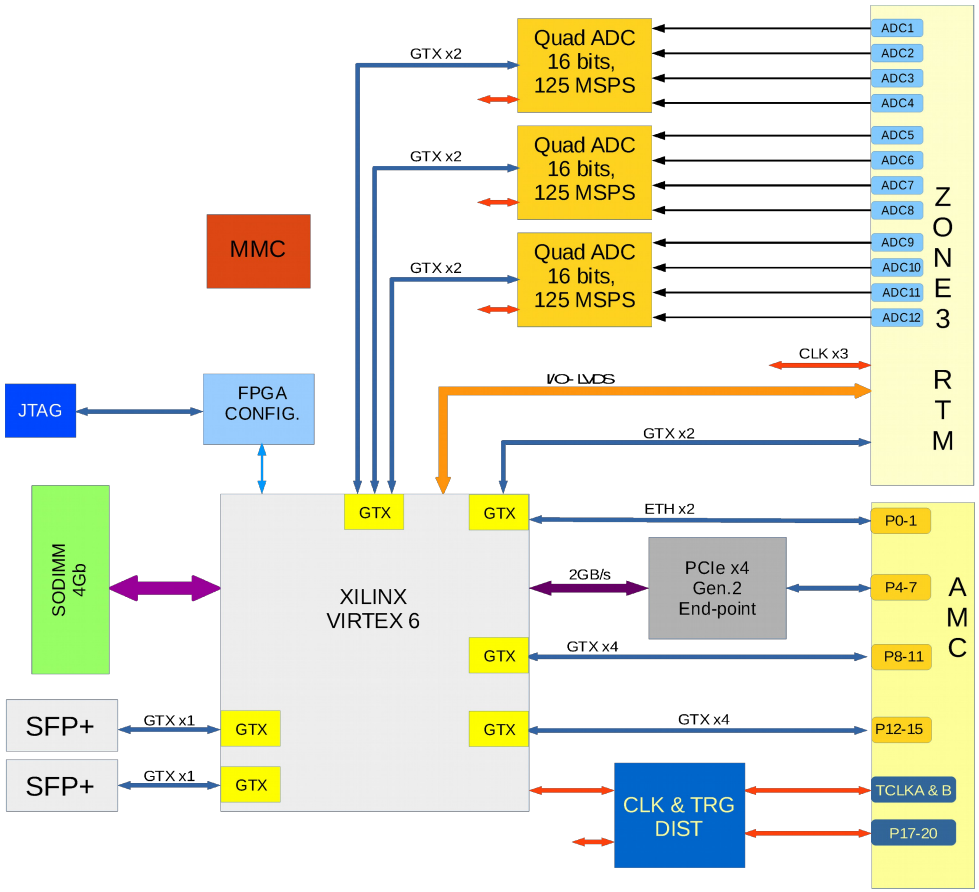
- EFMC-D041
- EFMC-D081
- EFMC-D082
- EFM-DST01
- EFMC-DIO1

Hardware Development
EAMC-D102

- XC6VLX130T 128000 Logic Cells, 20 GTX transceivers
- ADC: AD9656 - 16-Bit, 125Msps AC & DC
- DAC: MAX5878 - 16-Bit, 250Msps, High-Dynamic-Performance, Dual DAC
- SODIMM socket for memory extension
- Integrate low jitter clock distribution with tunable delays
- mTCA.4 compliant
- PCIE Gen 2 x4 (independent FPGA)

RTM connection:
- analog input channels: 12
- analog output channels: 2

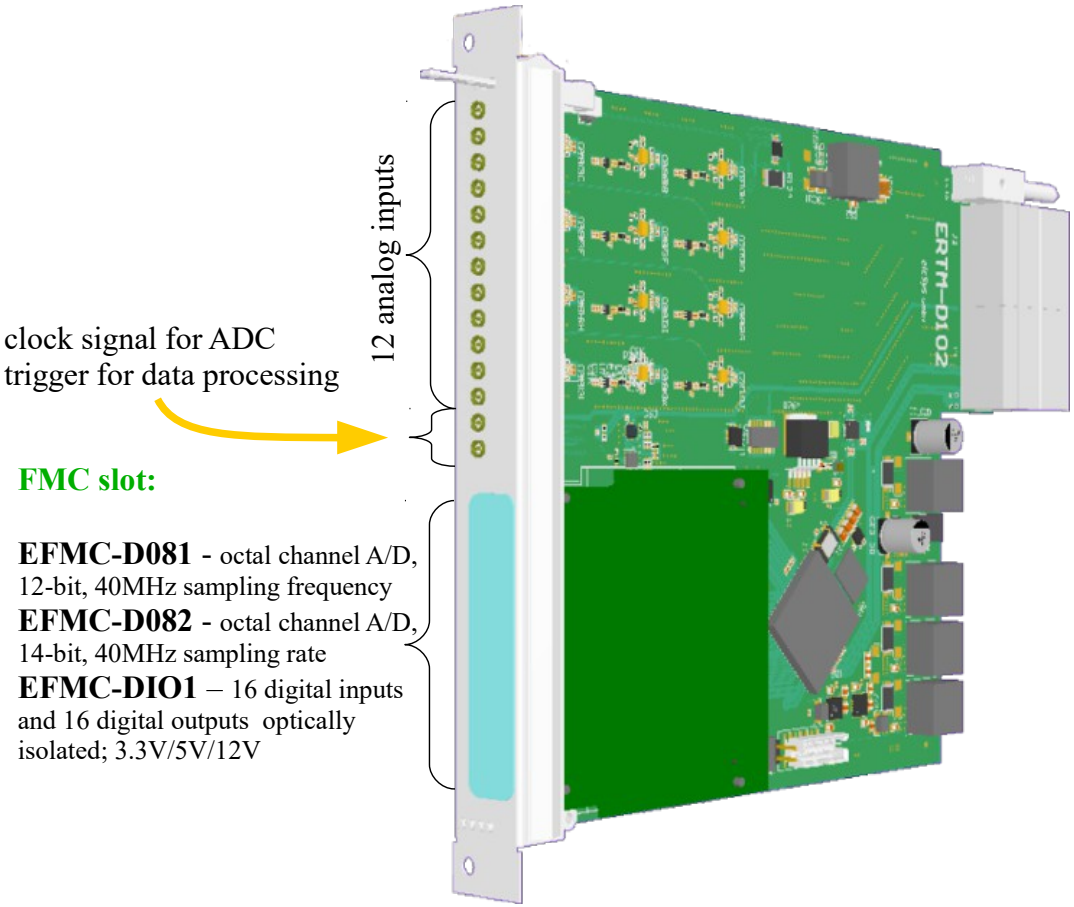
Hardware Development
EAMC-D102



- XC6VLX130T 128000 Logic Cells, 20 GTX transceivers
- 12 ch.16-bit, 125Msps AC & DC
- SODIMM socket for memory extension
- Integrate low jitter clock distribution with tunable delays
- mTCA.4 compliant
- **Hardware PCIE Gen 2 x4 endpoint**

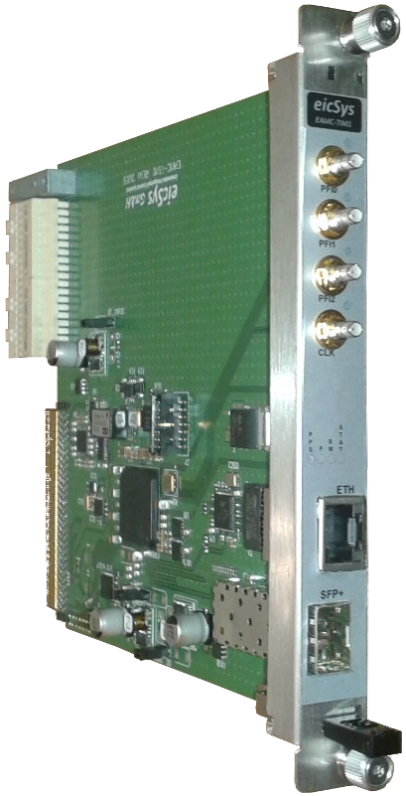
RTM connection:
- analog input channels: 12
- analog output channels: 2
- clocks, management

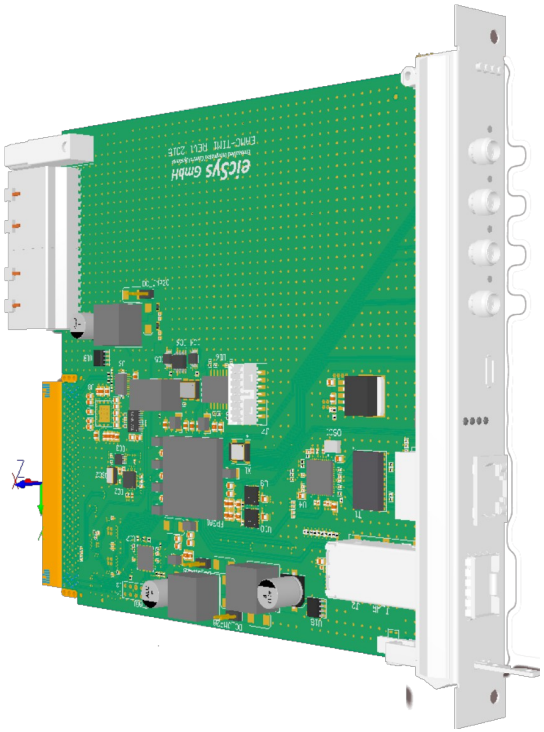
Hardware Development
ERTM-D102



- **Front** Panel
  - 12 x input signal, MMCX, AC or DC
  - 2 x clock signal, MMCX
  - FMC HPC (Artix 7 for MGMT)
- **Zone** 3
  - 12 x analog signal
  - 2 x clock signals
  - 2 x MGT interface
  - Management

Hardware Development
EAMC-TIM1

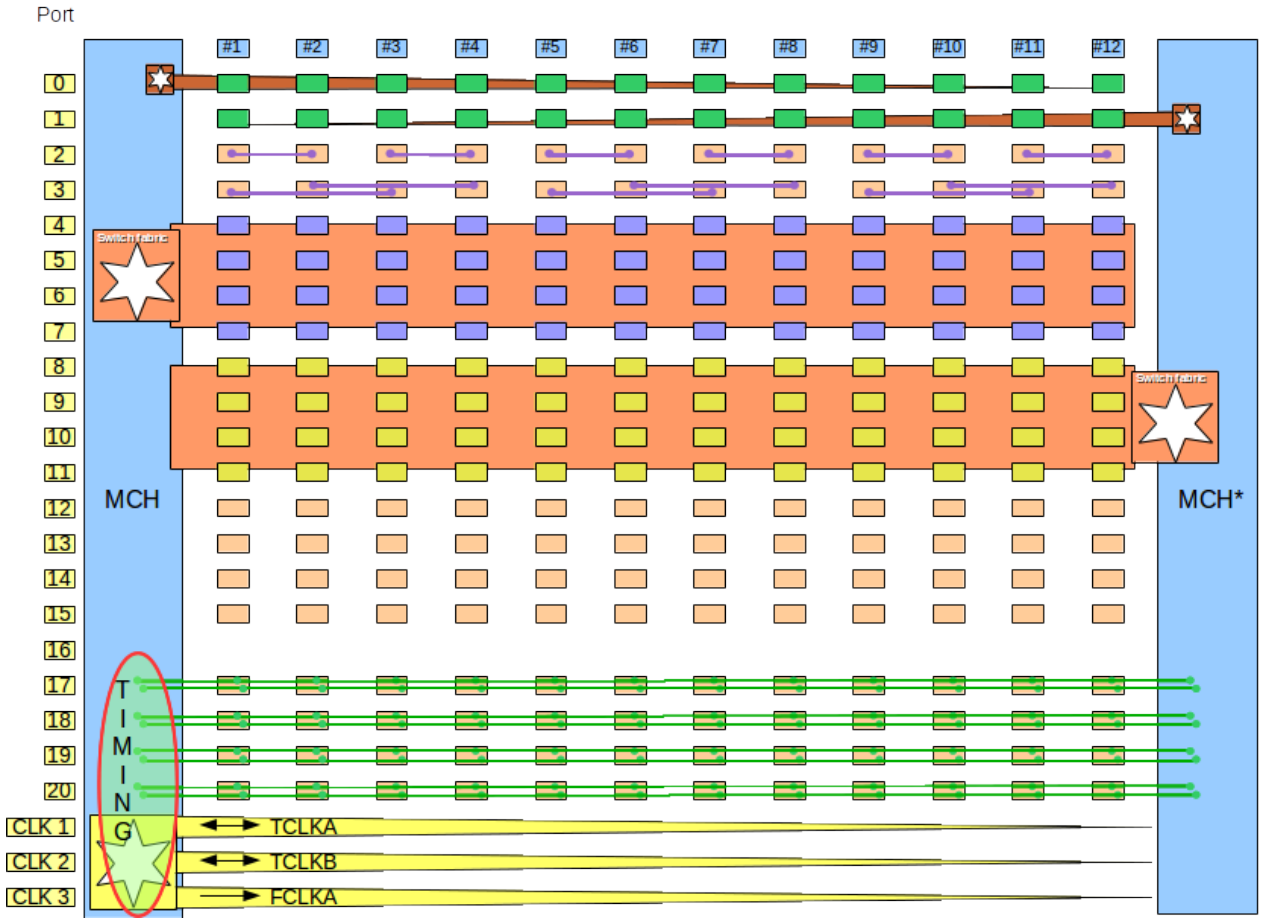




- **IEEE 1588 – PTP**
- **WhiteRabbit** ready

- Front Panel
  - SFP+
  - RJ45
  - USB
  - 3xDIO
  - 1xPPS
- Backplane
  - 1 x PCIe
  - 1x ETH
  - 2 x low jitter clock output
  - Management
  - 8x MLVDS trigger source

Hardware Development
Timing Integration into MCH



Each DAQ/Control System has timing

Clock signal recovered/generate in AMC slot send to MCH and then distributed – added jitter ↑↑↑

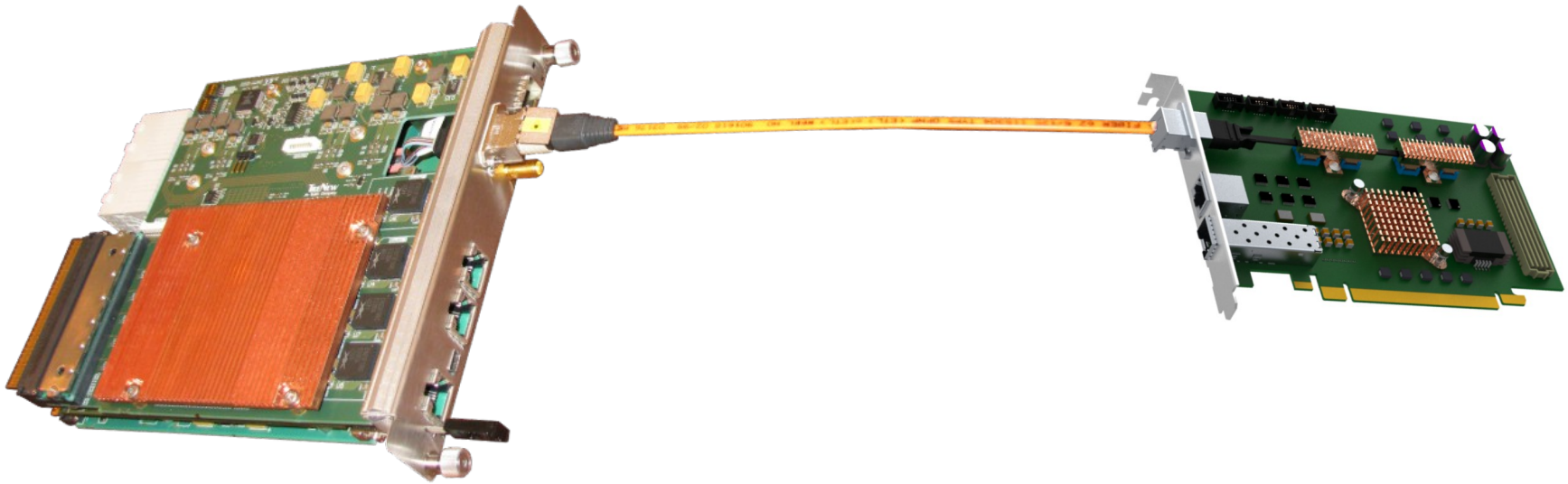
Reduced added jitter

Save slot for application

MTCA.4 Systems Scalability

ELMA Your Solution Partner

- External, powerful PC might be connected to several MTCA.4
- Distance between PC and chassis is up to 150m
- Daisy chain between MTCA.4 system possible



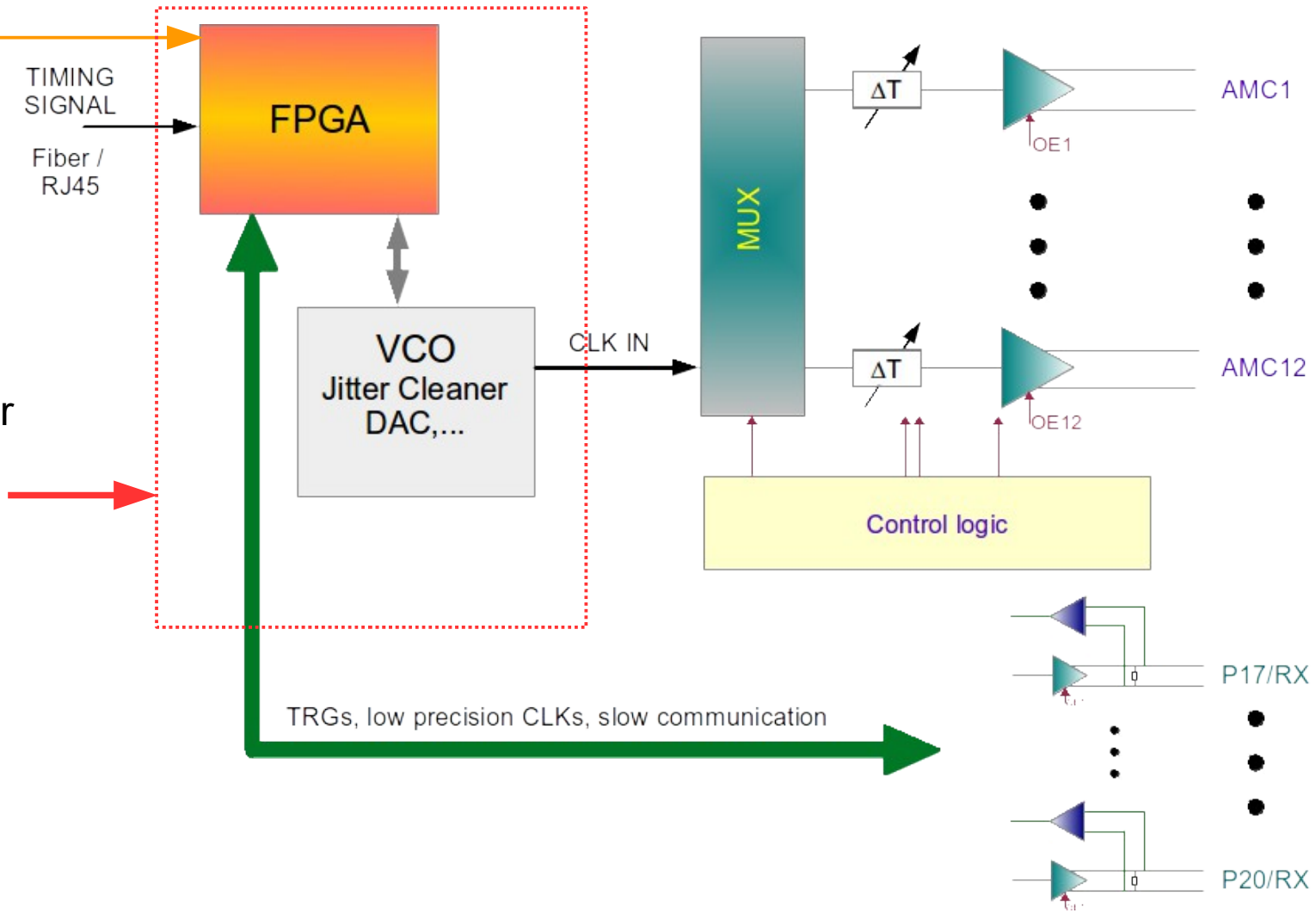
MCH
Timing Module & Trigger Signals

ELMA
Your Solution Partner

PCIe x1
Control interface

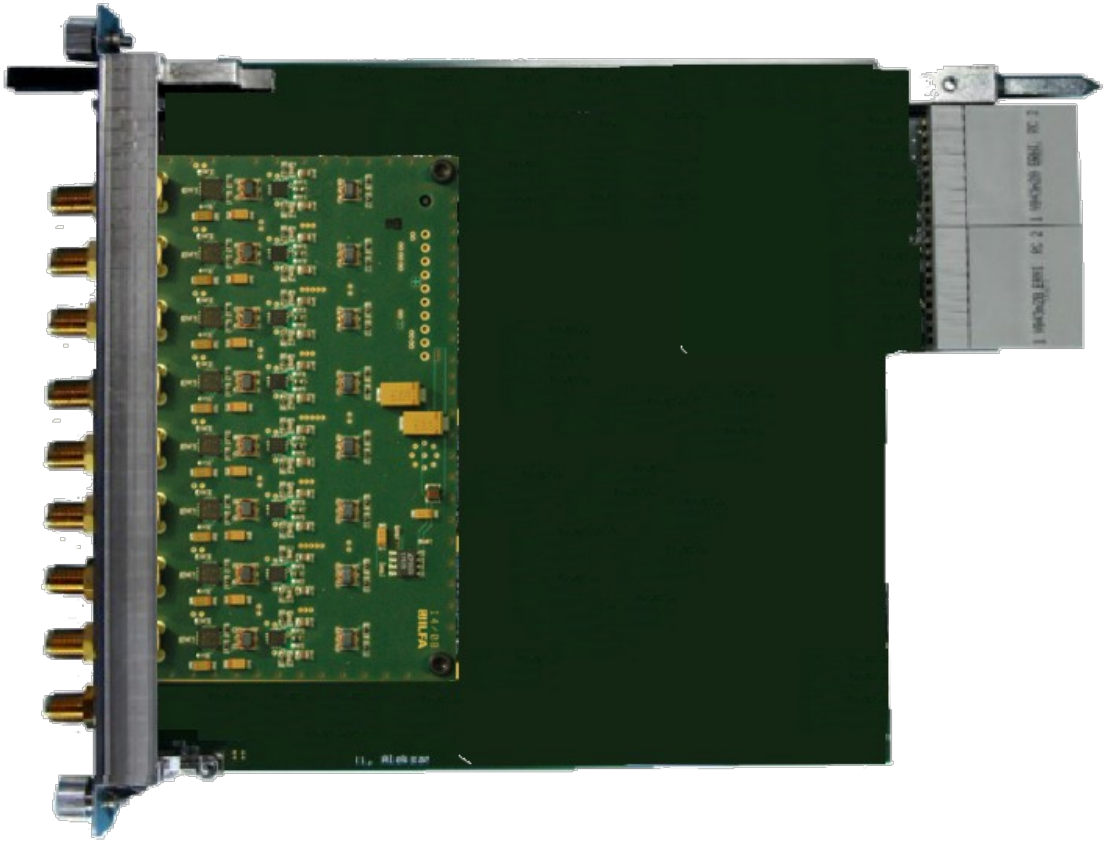
Timing & Event Receiver

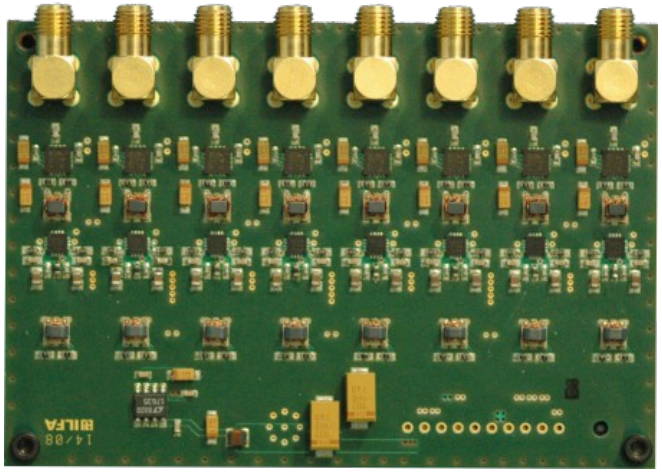
- IEEE1588
- White Rabbit
- … ?



Hardware Development
ERTM-RF081

Cryoelectra





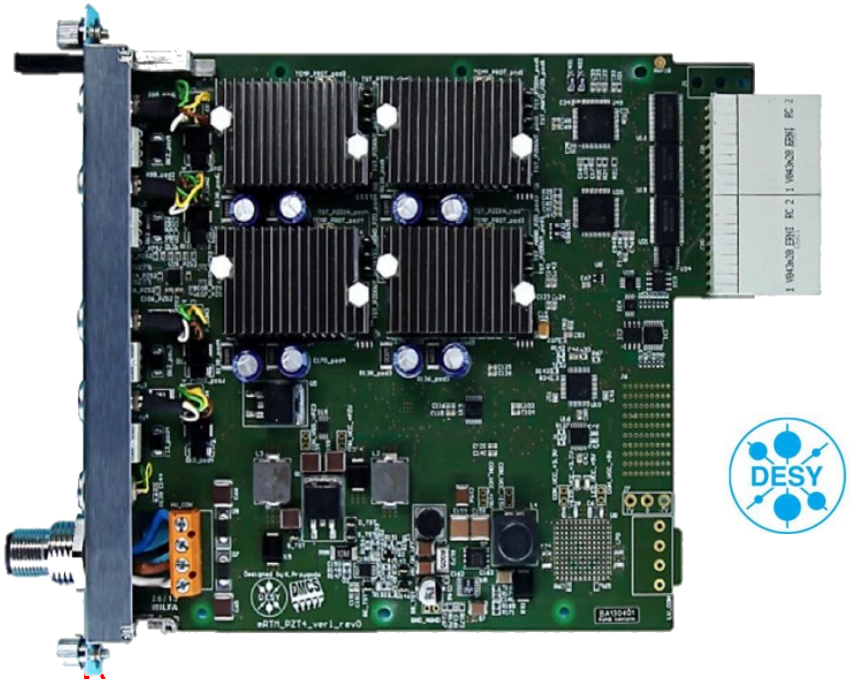
8 ch. down-converter

- LO Frequency - 1250-1350 MHz
- LO Input Power 10dBm
- RF Frequency – 1250-1350MHz
- RF Input Power – 9.5 dBm
- IF Frequency – 1-50 MHz

Hardware Development
Manufactured on DESY license

EAMC-FMC500 –
FMC carrier

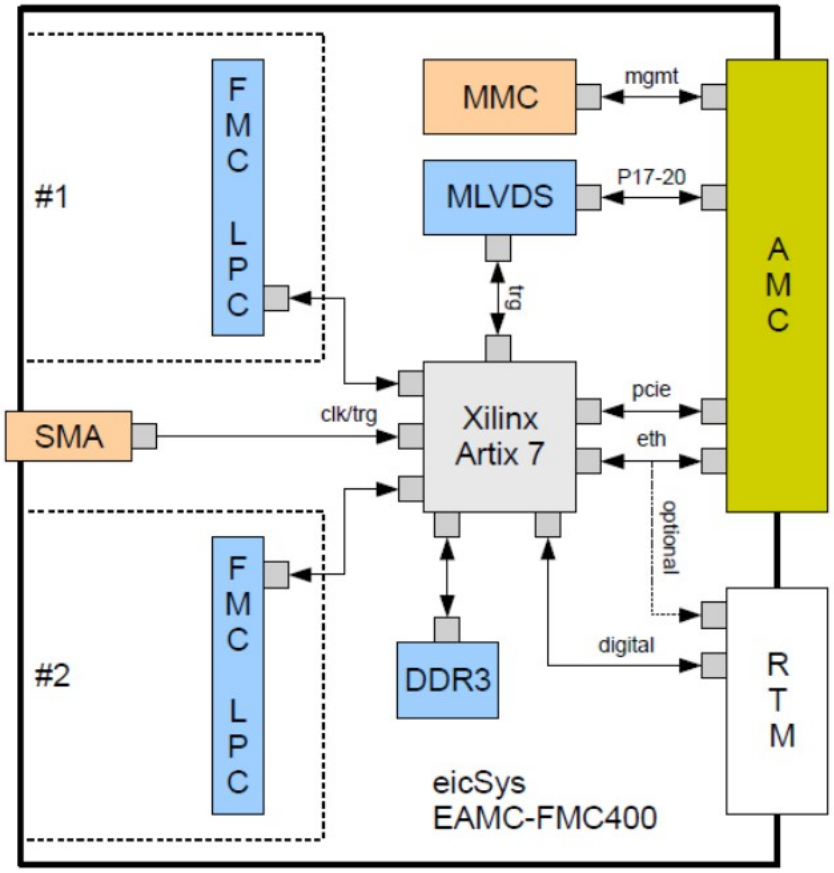
- 1 x HPC
- 1 x LPC
- Rear IO
- MTCA.4
- Spartan 6



ERTM-PZT4 (planned)

- 4 channel Piezo Drivers and Piezo Sensors
- SSBW ~ 50 kHz, CL = 0.1 uF, Vo = 5 Vpp
  Unipolar: 0..+100 V and bipolar: ±100 V
- Interlock signal support

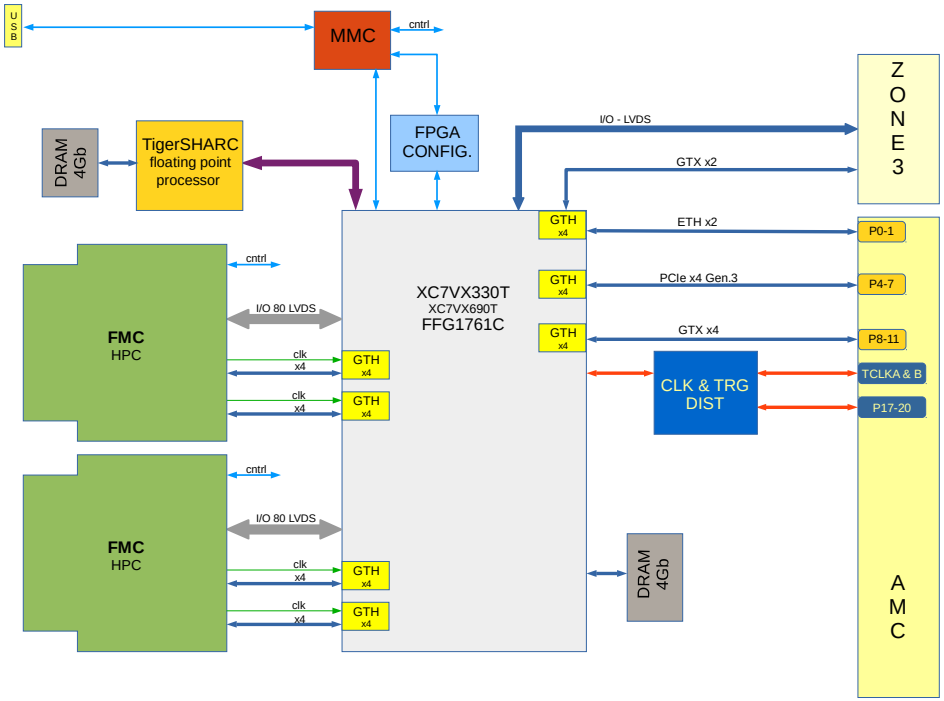
Hardware Development
EAMC-FMC400



- Low performance FMC Carrier with Artix 7
- 2x LPC slots
- Single VADJ for both FMC slots - if the condition is not met, the FMC slots will not power up.
- Due to PCIe Gen1/Gen2 data bandwidth is limited to ~250MB/s
- Low Performance Clock distribution will limit the usage of the board for low clock jitter applications.

Z3 pinout compatible with ERTM-PTZ4

Hardware Development
EAMC-FMC270



- Double width RTM Module compliant to PICMG Specification MTCA.4
- Xilinx Viretx 7, XC7VX330T-2
- Analog Devices TigerSHARC floating point processor
- High Pin Count Connector
  - 8 x GTH Links (10 Gbps)
  - I/O – 80 LVDS
  - control signals (3.3V)
- TCLKA, TCLKB, RTM, FCLK
- Ports 0 and 1 – GbEth
- Ports 4-7 – PCIe x4 Gen.3
- Ports 8-11 - PCIe x4 Gen.3 / fast links 10 Gbps

Hardware Development
EFMC-D081

Texas Instruments ADS5292 ADC:

- Maximum Sample Rate: **80 MSPS**
- Resolution: **12 Bit**

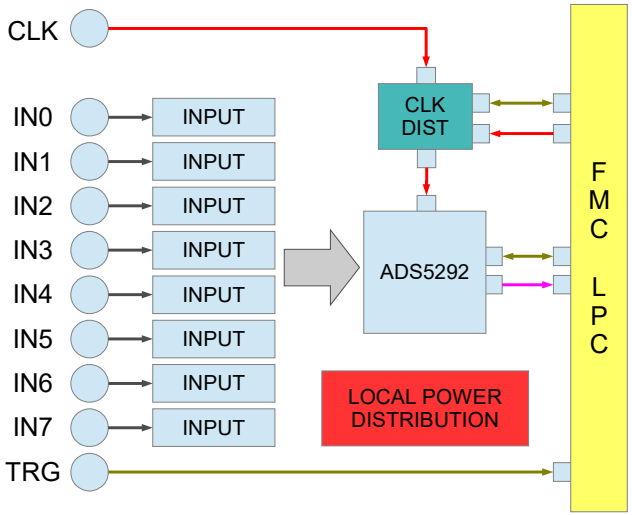
Front panel inputs:

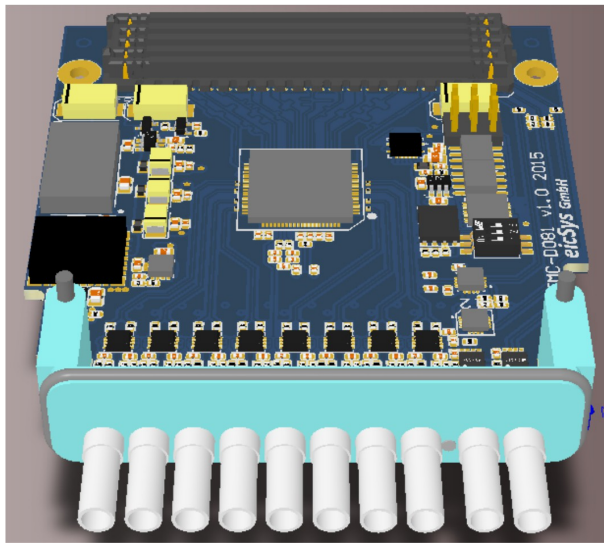
- 8 x analog channels (MMCX or SSMC)
- 1 x clock
- 1 x trigger

Integrated Clock Distribution

Power distribution

LPC module





Integrated Systems
mTCA.4 - 1U

Possible applications:

- small LLRF systems
- electronics for BPMs
- Extension of bigger system - connection via fibre
- Any system which requires small sets of boards distributed over larger area (e.g. electronics close to RF station)

Hardware Development
EFMC-D082

Linear technology LTC2175 ADC:

- Maximum Sample Rate: **125 MSPS**
- Resolution: **14 Bit**

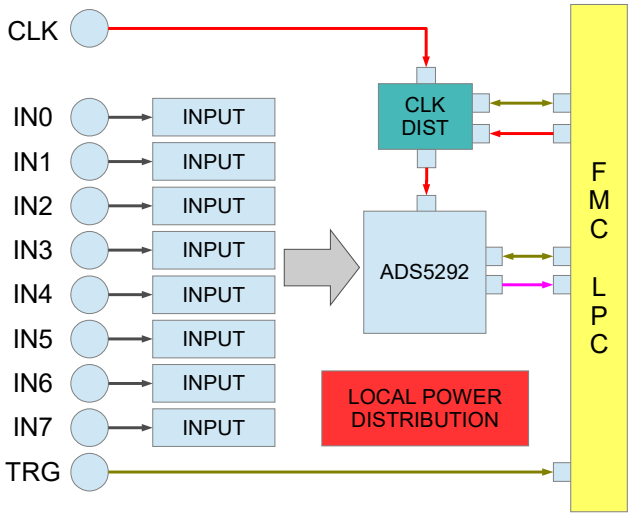
Front panel inputs:

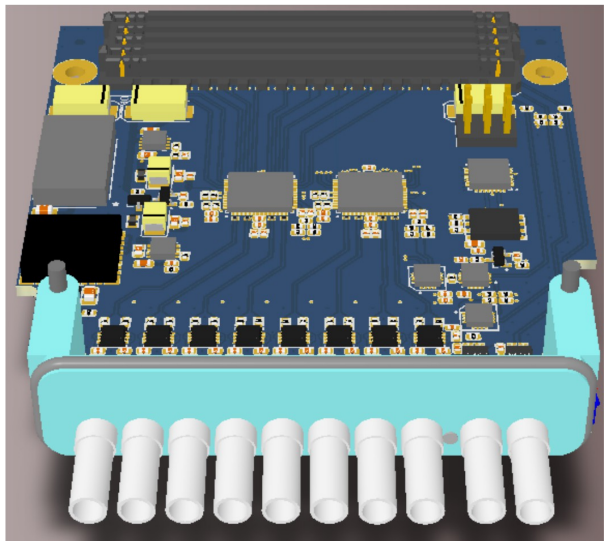
- 8 x analog channels (MMCX or SSMC)
- 1 x clock
- 1 x trigger

Integrated Clock Distribution

Power distribution

LPC module

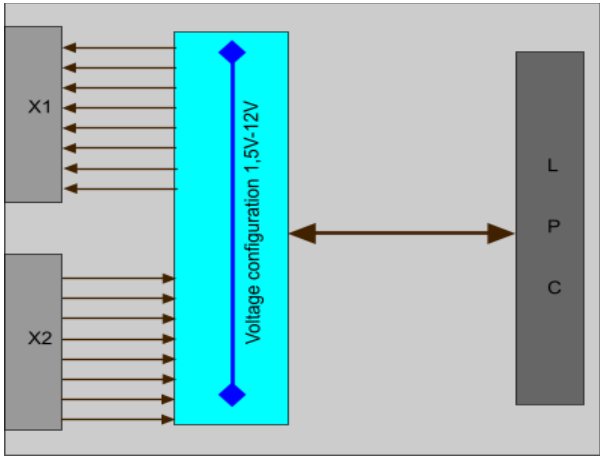




Hardware Development
EFMC-DIO1, EFMC-DST01

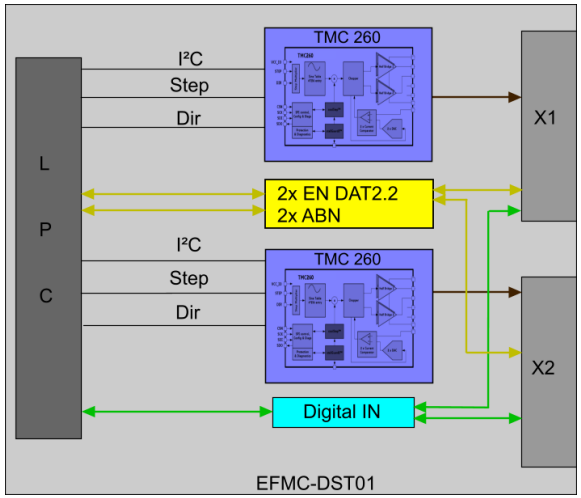
EFMC-DIO1

- 8 digital inputs
- 8 digital outputs
- Optical isolation
- Voltages 3.3V, 5V, 12 V



EFMC-DST01

- Microstepping driver board
- Programmable current slopes
- one power monitor per channel
- Each channel supports EnDat2.2 and ABN-encoder readout
- Compatible products:
  - EAMC-FMC500
  - EAMC-FMC400



Firmware

We are using individual approach to each customer - the offered firmware can be customized for customer needs and extended by additional modules according to presented requirements.

All the available firmware modules are integrated into a modular framework called "UniDAQ firmware framework", which provided standard interface to the wide range of hardware.

Firmware
uni_daq_firmware

Universal firmware framework optimized for:

- eicSys EAMC-D102
- Struck SIS8300, SIS8300L

The framework also supports:

- TEWS TAMC900
- eicSys EAMC-FMC500
- eicSys EAMC-FMC400
- eicSys EAMC-FMC270
- eicSys EATCA-101

Currently it is used at ITER, SLAC, IHEP, Beijing and CERN. Further talks with SINAP are in progress.

Firmware/Software Layers

Firmware

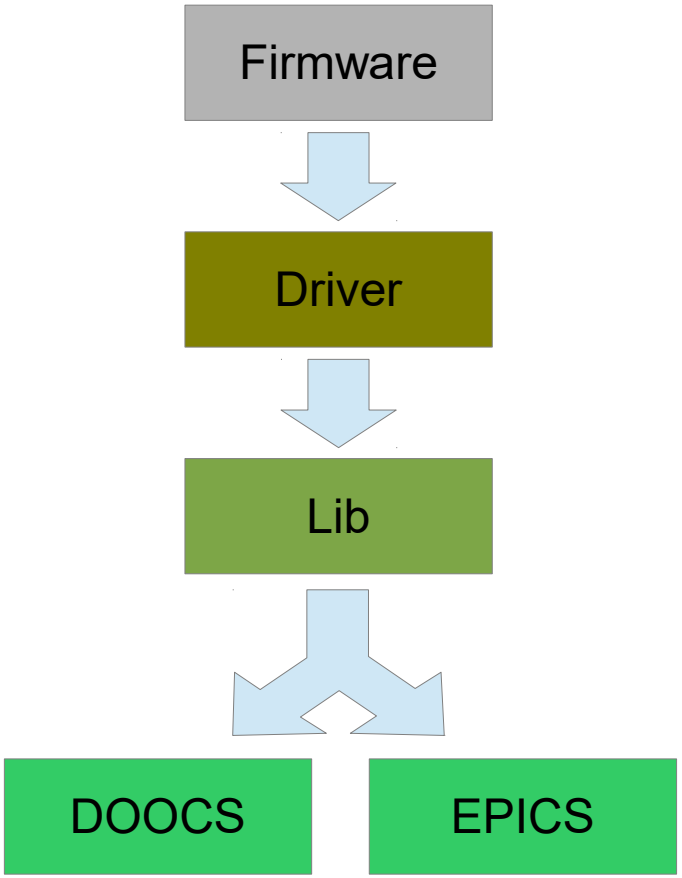
- Modules for peripheral handling (ADC...)
- Communication interfaces (PCIe, ETH...)
- Dedicated place for user modules

Driver

- Interaction with firmware
- Provides hardware independent interface using IOCTL functions for upper layers

Library

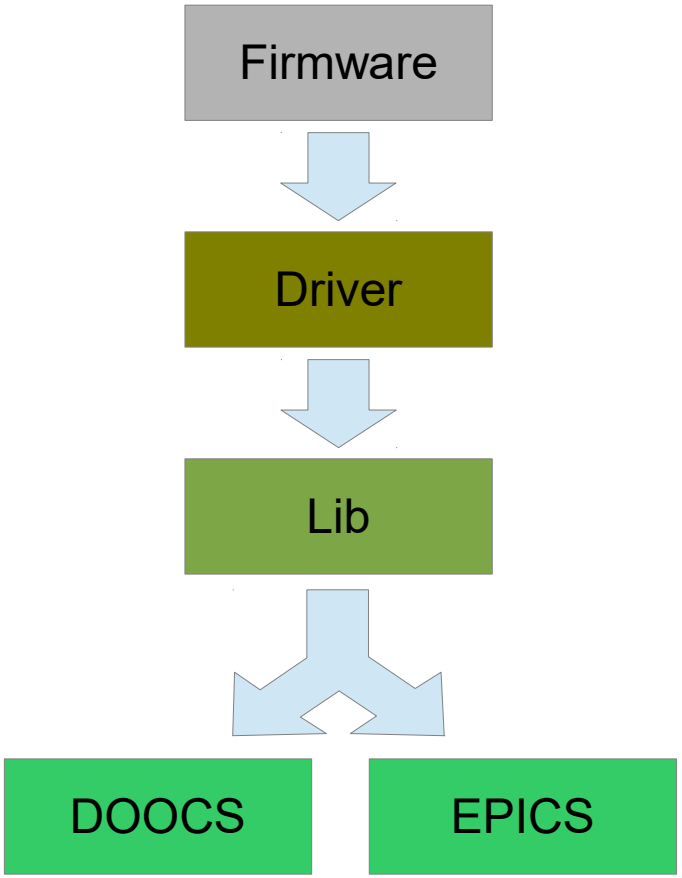
- Additional supporting function



Firmware/Software Features

- GEN1 PCIe transfer rate up to 860 MB/s
- GEN2 PCIe transfer rate up to 1550 MB/s
- Low resource usage

- User firmware does not require any changes when porting to different board
- All features of mTCA.4 available
- Example EPICS and DOOCS implementations



Firmware/Software
Special applications – modules for LLRF

- I-Q measurements from any IF/sampling freq ratio or direct sampling of raw data
- A-P recalculation (low latency or low resource usage)
- Filtering (IIR,FIR, etc.)
- System Generator wrapper blocks for user extension of functionality
- PID controllers - pipelined or lightweight
- non-linearity correctors

Algorithms are numerically optimized for customer's application

Firmware/Software
Special applications – modules for ITER

- Pulse discrimination algorithm – specialized module with processes signals from detector to measure neutron flux.
- Support for dedicated RTM7201 – extension of the framework to support specialized switching amplifier RTM7201 on a firmware/driver level

The framework can be extended on demand
to support custom peripherals and hardware

Thank you