

JTAG Debugging of multiple FPGAs



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Agenda

Simplify JTAG Debugging of multiple FPGAs



- Motivation
- What is needed?
 - Backplane
 - JTAG Switch Module
- Examples
- Summary



JTAG Connections

System with multiple FPGA AMCs



How to do this change remotely?



All JTAG Connections Routed to one Slot (JSM Slot)



Figure 2: Rear View



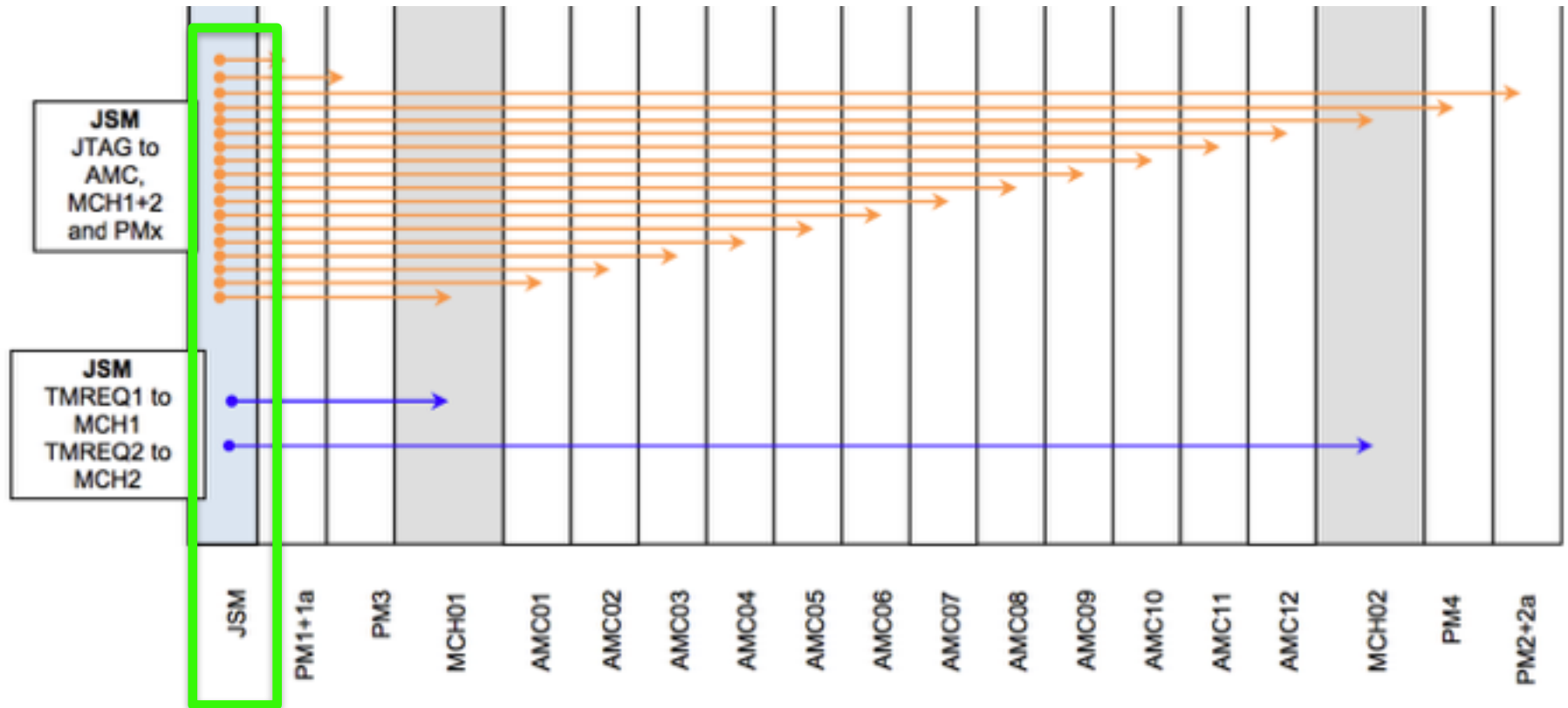
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- | | | | |
|---|--|----|-----------------|
| 8 | Card cage PM and JSM | 10 | Card Cage RTM |
| 9 | Cable Tray (Can be mounted above or below the card cage) | 11 | Ground Terminal |



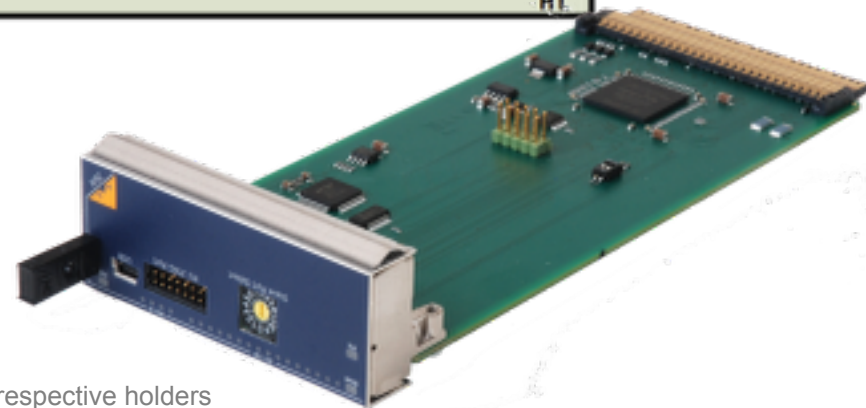
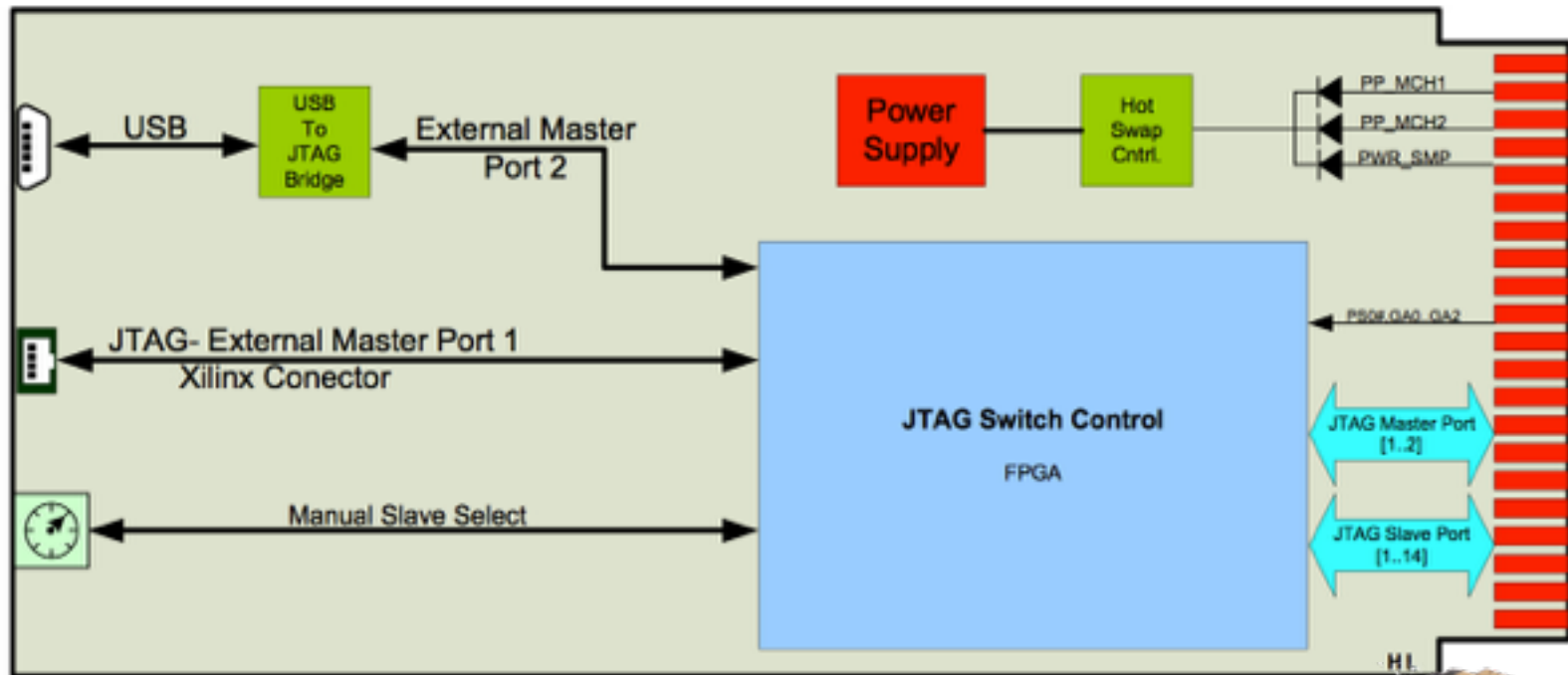
JTAG Interconnection to One Slot

JTAG AMC 1-12, MCH 1+2, PM 1-4



JTAG Switch Module for MTCA

NAT-JSM: single, compact/mid/full-size

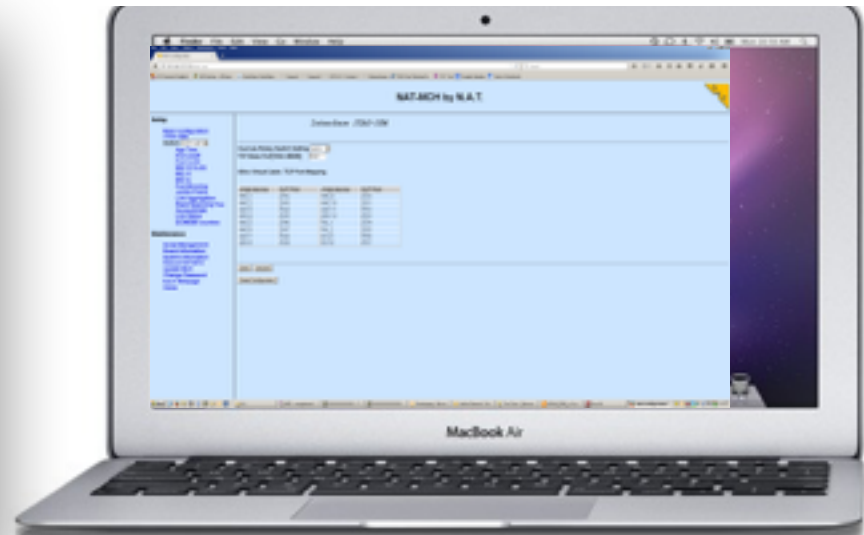


NAT-JSM: JTAG Channel Selection

Rotary Switch and/or Webinterface



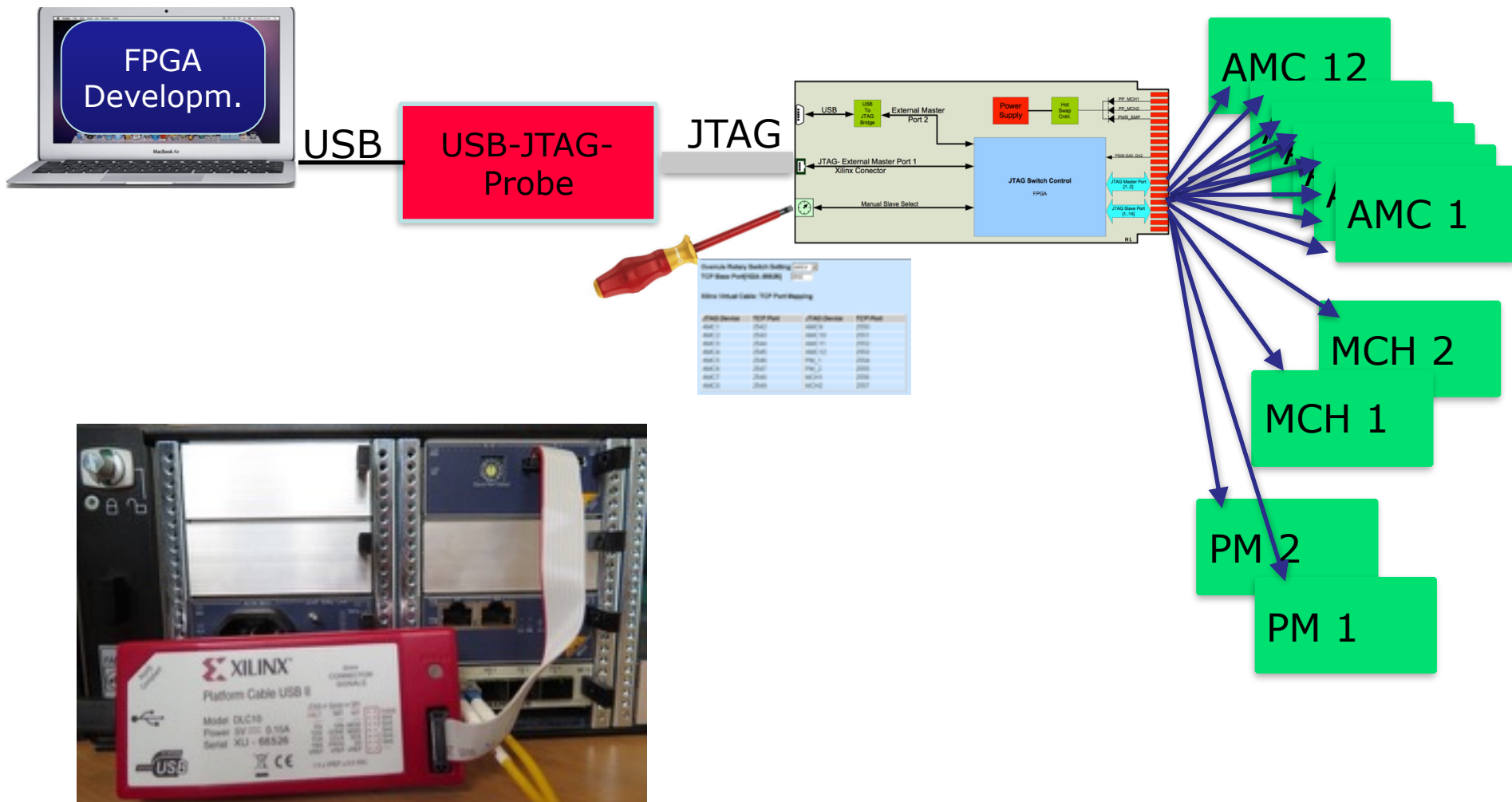
- AMC1-12
- PM 1-2
- MCH 1,2



NAT-MCH

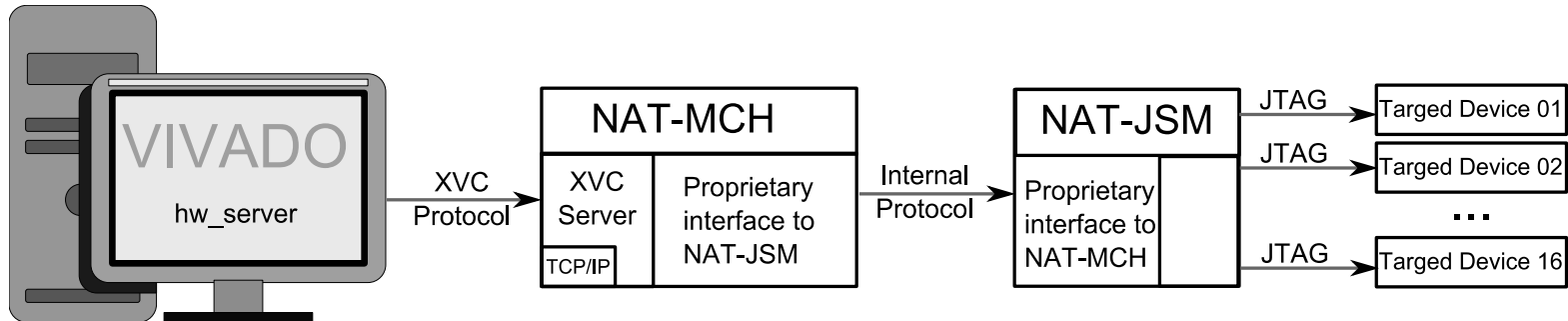
NAT-JSM JTAG Connection

JTAG-Probe of Xilinx, Lattice, Altera etc



Xilinx Connectivity Topology

Xilinx Virtual Cable (XVC) over TCP/IP



Interface JTAG-JSM

Overrule Rotary Switch Setting: AMC1

TCP Base Port[1024..65535]: 2542

Xilinx Virtual Cable: TCP Port Mapping

JTAG Device	TCP Port	JTAG Device	TCP Port
AMC1	2542	AMC9	2550
AMC2	2543	AMC10	2551
AMC3	2544	AMC11	2552
AMC4	2545	AMC12	2553
AMC5	2546	DEV1	2554
AMC6	2547	DEV2	2555
AMC7	2548	DEV3	2556
AMC8	2549	DEV4	2557

Save Discard

Reset Configuration

Interface JTAG-JSM

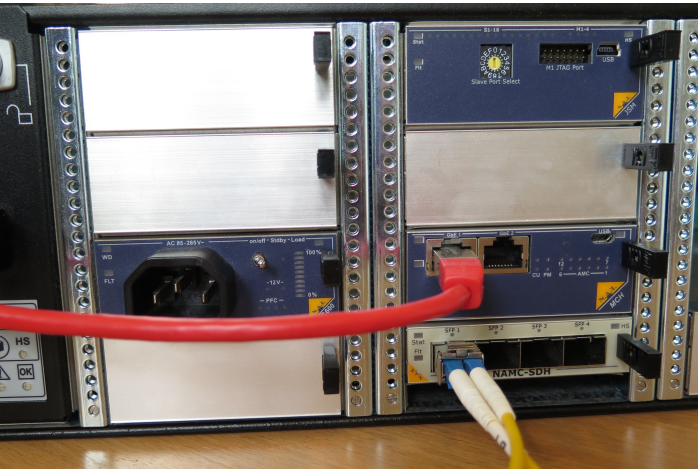
Overrule Rotary Switch Setting: AMC1

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AMC3	2544	AMC11	2552
AMC4	2545	AMC12	2553
AMC5	2546	PM_1	2554
AMC6	2547	PM_2	2555

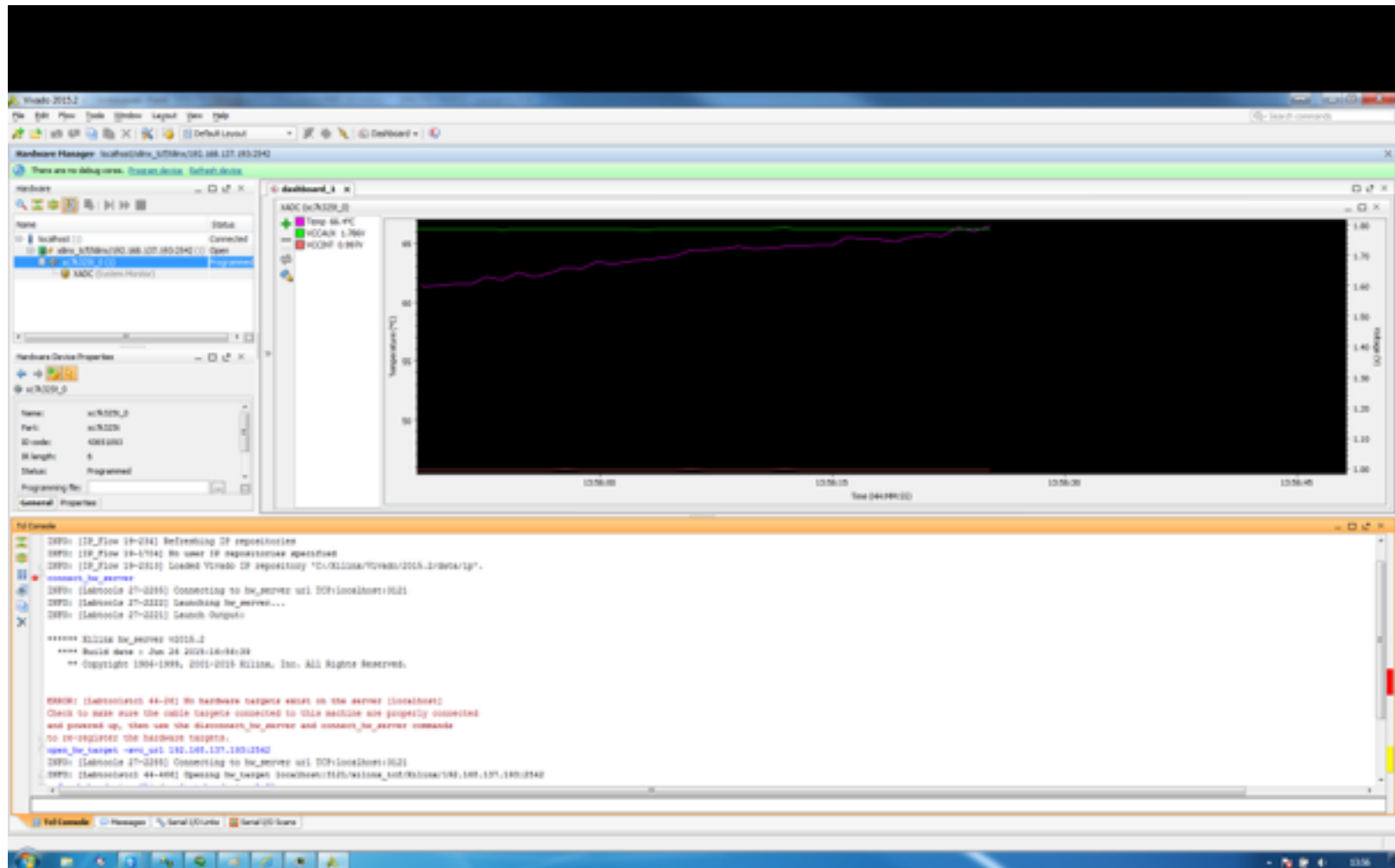

```
open_hw_target -xvc_url 192.168.137.193:2542
```





Xilinx Vivado Software

Hardware-Monitor (live Temp and Voltages)



Tutorial IBERT Tool Live via JTAG Tuning & Analysis of SerDes, Eye-Opening



Project Manager

- Project Settings
- Add Source
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

Program and Debug

- Bitstream Settings
- Generate Bitstream
- Launch HW Manager

IP Catalog

Name	API	Status	License	URL
100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip
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100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip
100K7 F Series GTX		Production	Included	xilinx.com/ip

Details

dynamic reconfiguration part attributes of the GTX transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG Test Access Group (TAG). Run-time interaction with the core requires the use of the Vivado serial I/O analyzer feature.

Status: **Production**

License: **Included**

Change Log: [View Change Log](#)

Vendor: **Xilinx, Inc.**

URL: [xilinx.com/ip/100k7_series_gtx/](#)

Repository: [C:/xilinx/Vivado/2013.2/data/ip](#)

Design Runs

Name	Constraints	Status	Progress	WNS	THS	WHS	THS	THUS	Failed Routes	LU %	LU %	PP %	PP %	BLK %	BLK %	DGP %	DGP %	Start	Elapsed	Strategy
synth_1 (active)	constraint_1	Not started	0%															8/20/13 11:46 AM	00:00:00	Vivado Synthesis Defaults (Vivado Synthesis)
impl_1 (active)	constraint_1	Not started	0%															8/20/13 11:51 AM	00:00:00	Vivado Implementation Defaults (Vivado Implementation)
Out of Context Module Runs																				
ghwizd_1_synth_1	ghwizd_1	synth_design_completed	100%							0.113	230	0.000	244	0.000	0	0.000	0	8/20/13 11:46 AM	00:00:00	Vivado Synthesis Defaults (Vivado Synthesis)
ghwizd_1_impl_1	ghwizd_1	impl_design_completed	100%															8/20/13 11:51 AM	00:00:00	Vivado Implementation Defaults (Vivado Implementation)

NAT-JSM Backplane Connector

Adaptable Pin Configuration (FPGA)

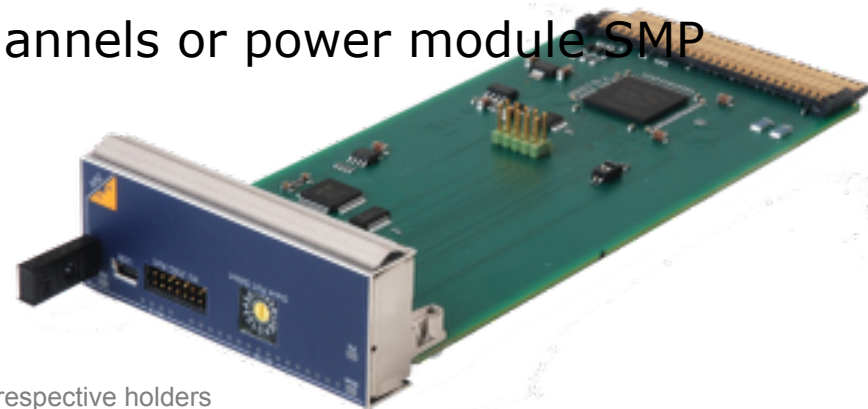


Pin #	JSM-Signal	JSM-Signal	Pin #
1	GND	GND	170
2	PP_MCH1	STCK1	169
3	IO_1 (PS1#) (*)	STMS1	168
4	3.3V (MP)	STDI1	167
5	GA0	STDO1	166
6	IO_2 (ETH) (*)	STRST#1	165
7	GND	GND	164
8	IO_3 (ETH) (*)	STCK2	163
9	PP_MCH1	STMS2	162
10	GND	GND	161
11	TCK1	STDI2	160
12	TMS1	STDO2	159
13	GND	GND	158
14	TDI1	STRST#2	157
15	TDO1	STCK3	156
16	GND	GND	155
17	GA1	STMS3	154
18	NC (PWR)	STDI3	153
19	GND	GND	152
20	TRST#1	STDO3	151
21	TMREQ#1	STRST#3	150
22	GND	GND	149
23	TCK2	STCK4	148
24	TMS2	STMS4	147
25	GND	GND	146
26	GA2	STDI4	145
27	PWR_SMP	STDO4	144
28	GND	GND	143
29	TDI2	STRST#4	142
30	TDO2	STCK5	141
31	GND	GND	140
32	TRST#2	STMS5	139

NAT-JSM compatible with most of today's MTCA chassis providing a JSM slot



- Automatic arbitration between JTAG Masters
 - JTAG download from MCH via WEB Interface
 - JTAG programming connector at front panel
 - JTAG to USB interface at front panel
- Target selection through JTAG information
- Overrule of automatic operation and dedicated selection of JTAG target by front panel elements
- Multiple JSM Pinout configurations via FPGA
 - output drivers are turned on if JSM slot is detected
- Power supply through MCH power channels or power module SMP power
- Minimal power consumption



Thank you very much!

Questions?



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