# JTAG Debugging of multiple FPGAs


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# Agenda
## Simplify JTAG Debugging of multiple FPGAs

- Motivation
- What is needed?
  - Backplane
  - JTAG Switch Module
- Examples
- Summary

# JTAG Connections

## System with multiple FPGA AMCs


How to do this change remotely?

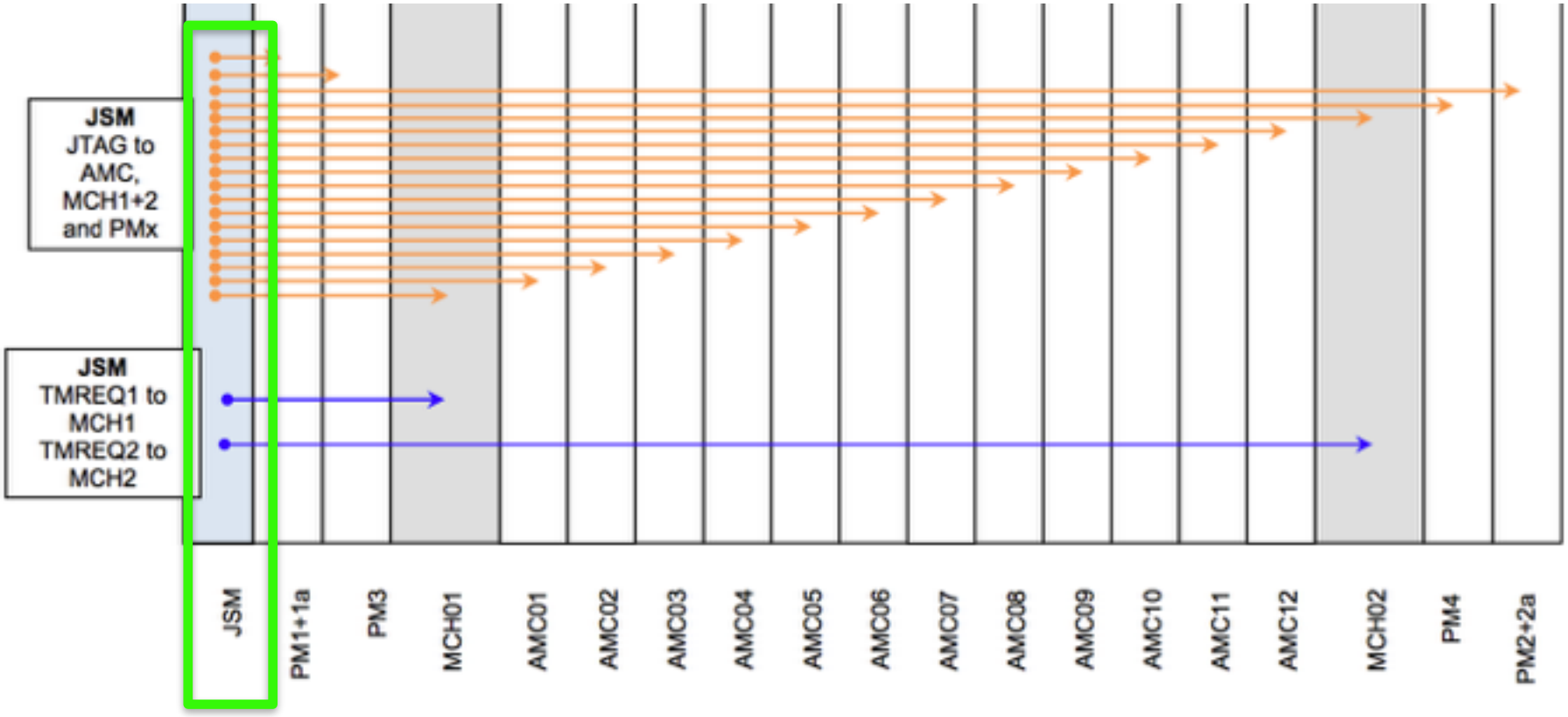
# All JTAG Connections Routed
## to one Slot (JSM Slot)

**Figure 2: Rear View**


| | | | |
|---|---|---|---|
| 8 | Card cage PM and JSM | 10 | Card Cage RTM |
| 9 | Cable Tray (Can be mounted above or below the card cage) | 11 | Ground Terminal |

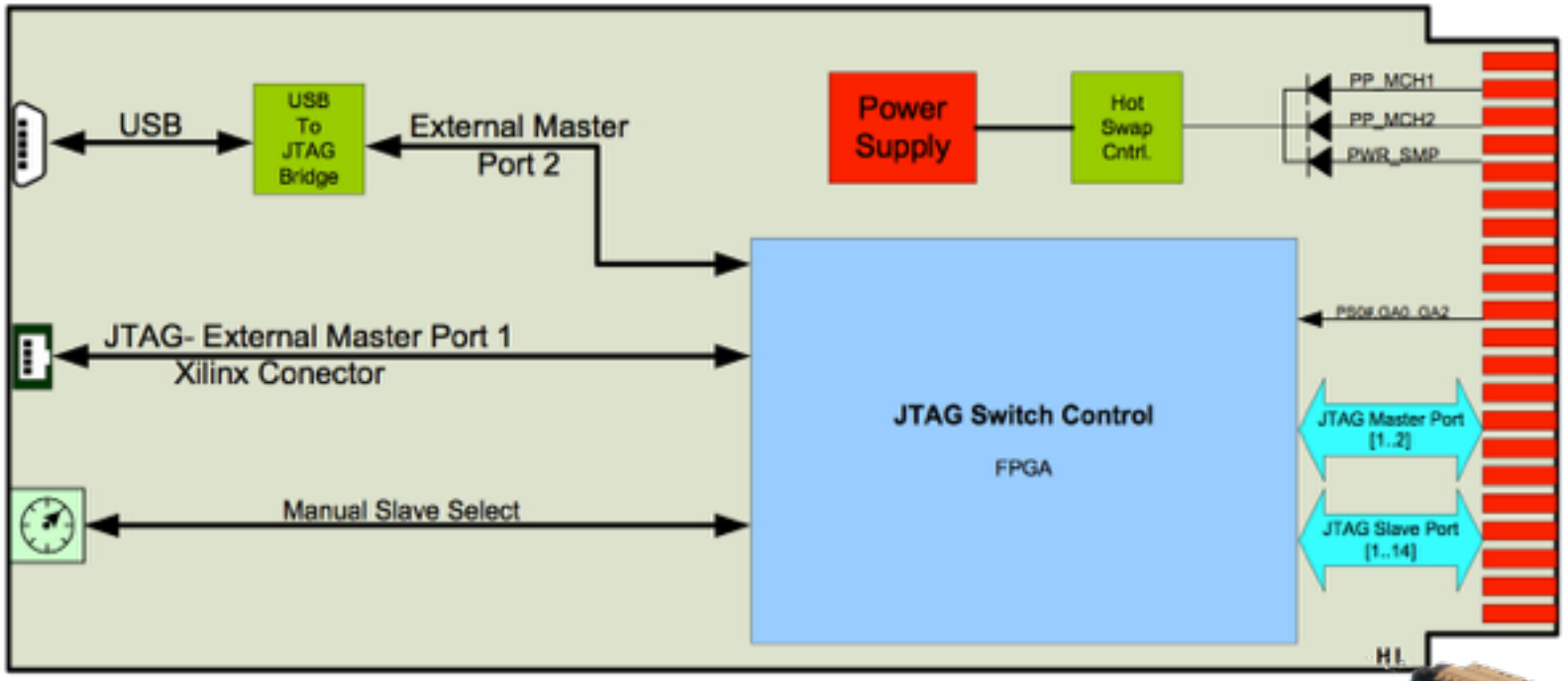
# JTAG Interconnection to One Slot
## JTAG AMC 1-12, MCH 1+2, PM 1-4

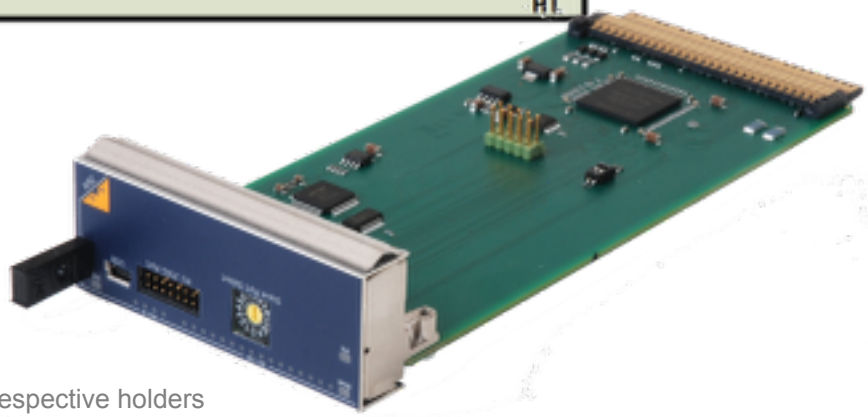


# JTAG Switch Module for MTCA

## NAT-JSM: single, compact/mid/full-size

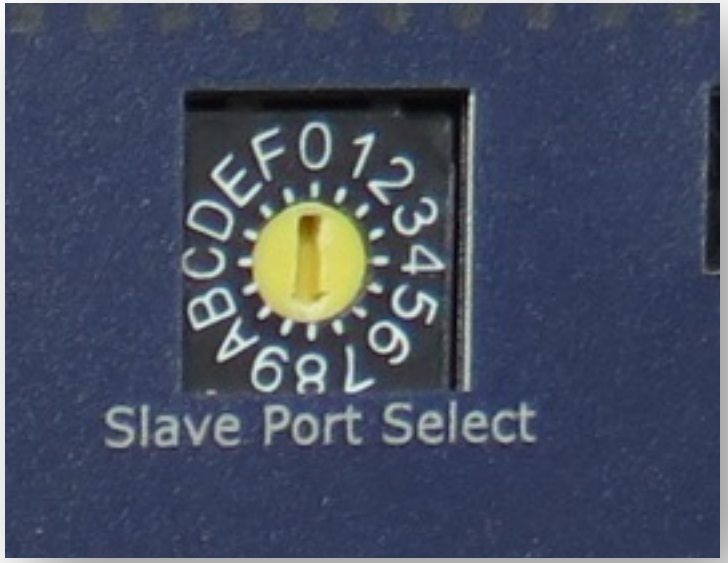


# NAT-JSM: JTAG Channel Selection
## Rotary Switch and/or Webinterface

- AMC1-12
- PM 1-2
- MCH 1,2

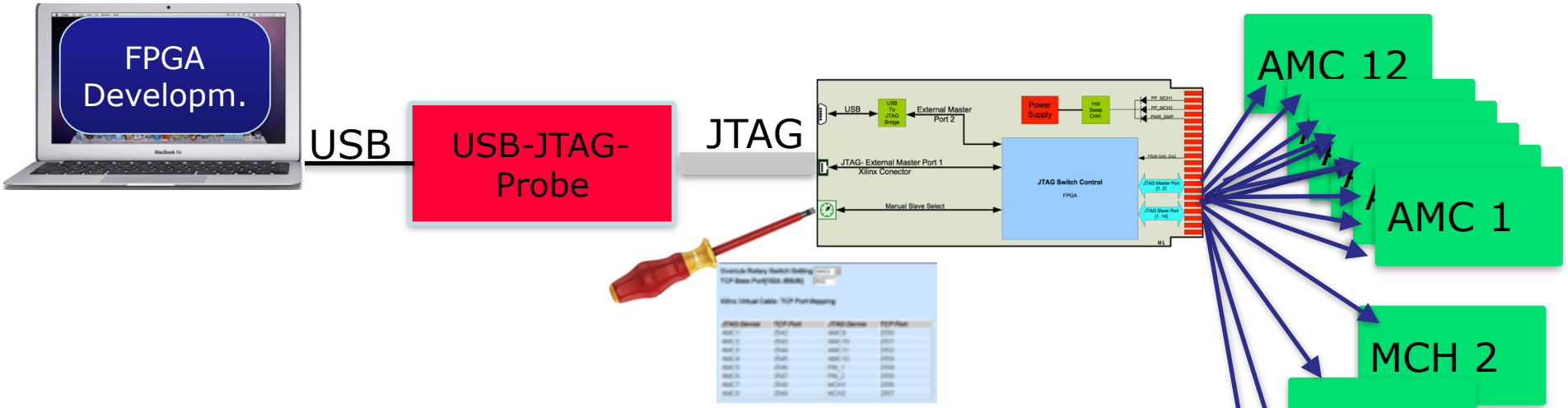




NAT-MCH

# NAT-JSM JTAG Connection
## JTAG-Probe of Xilinx, Lattice, Altera etc

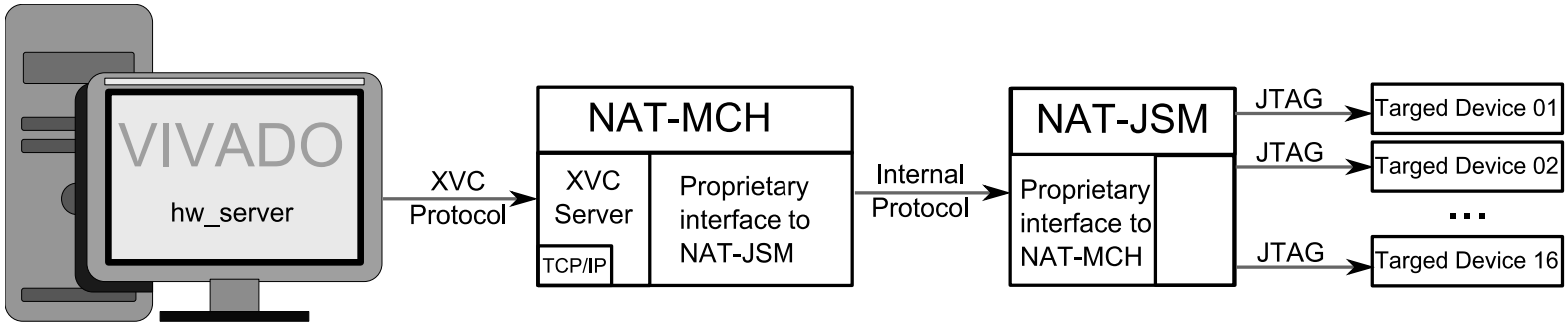


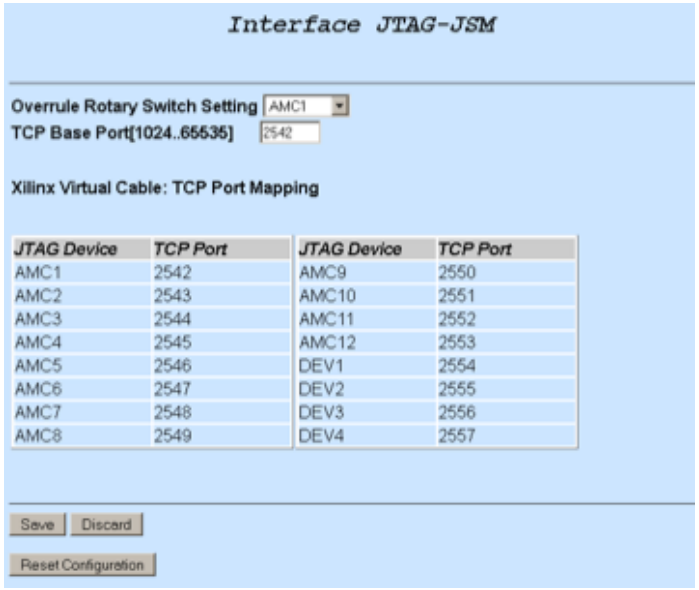


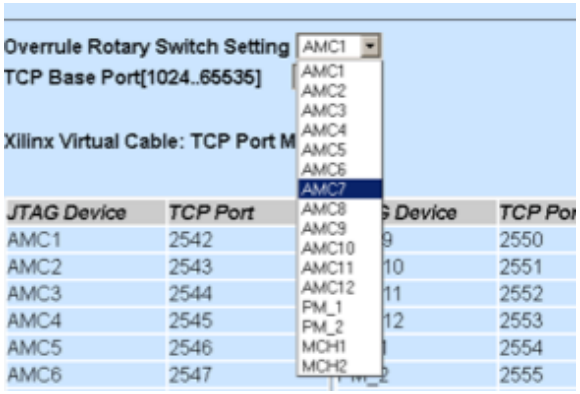
 

# Xilinx Connectivity Topology

## Xilinx Virtual Cable (XVC) over TCP/IP



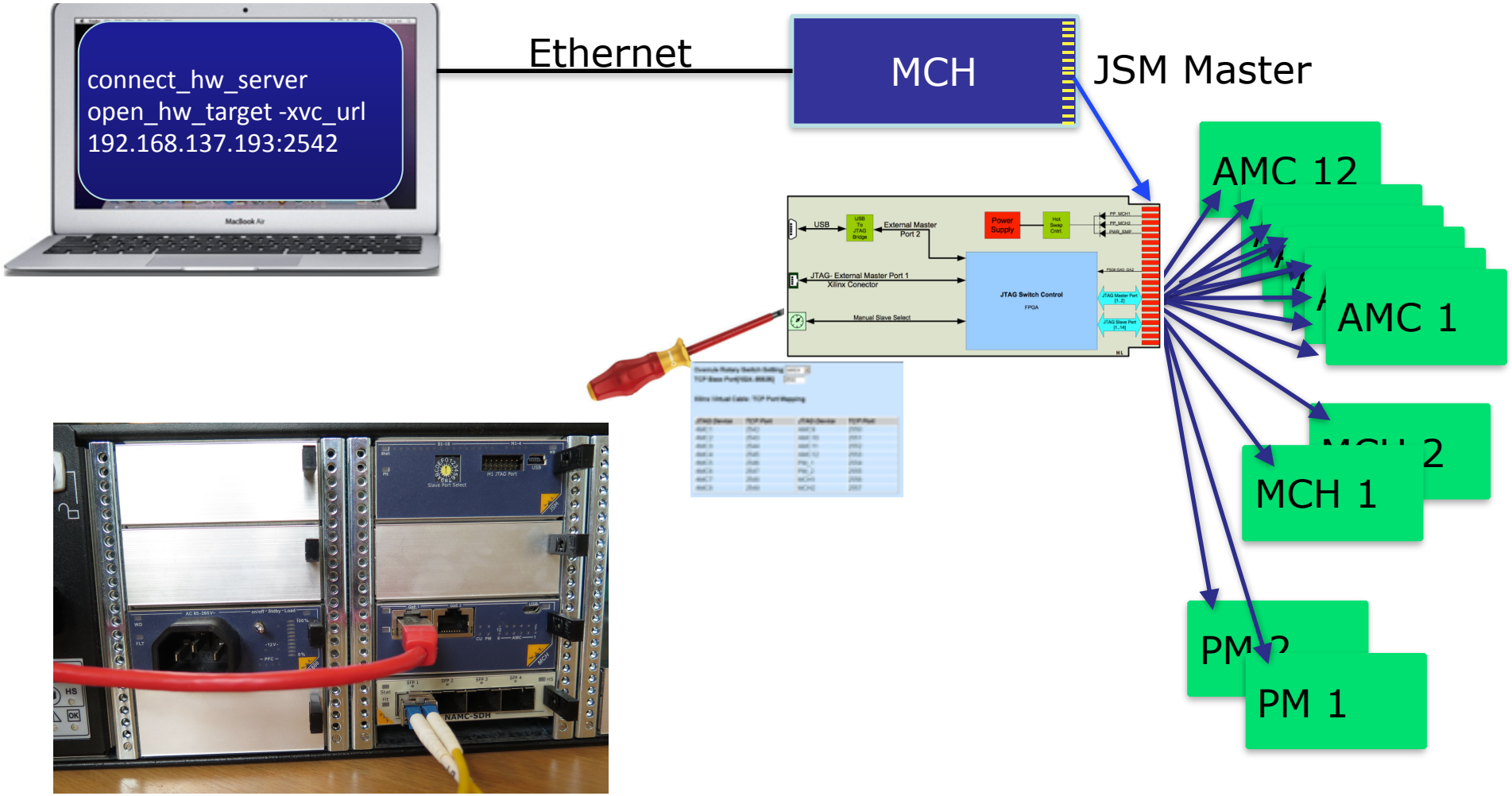



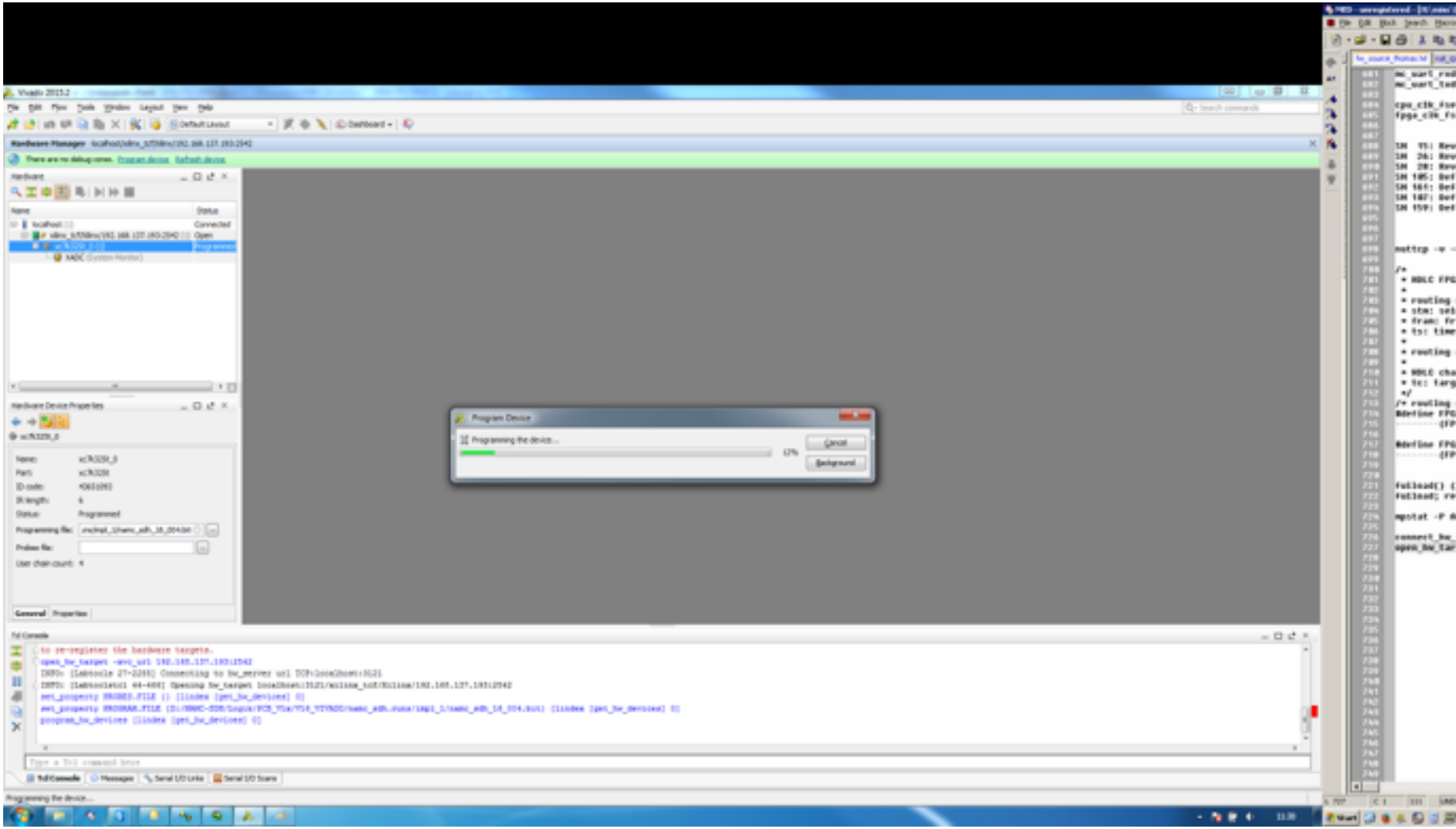
# NAT-JSM Ethernet to Xilinx HW Manager

## connect_hw_server
## open_hw_target -xvc_url 192.168.137.193:2542



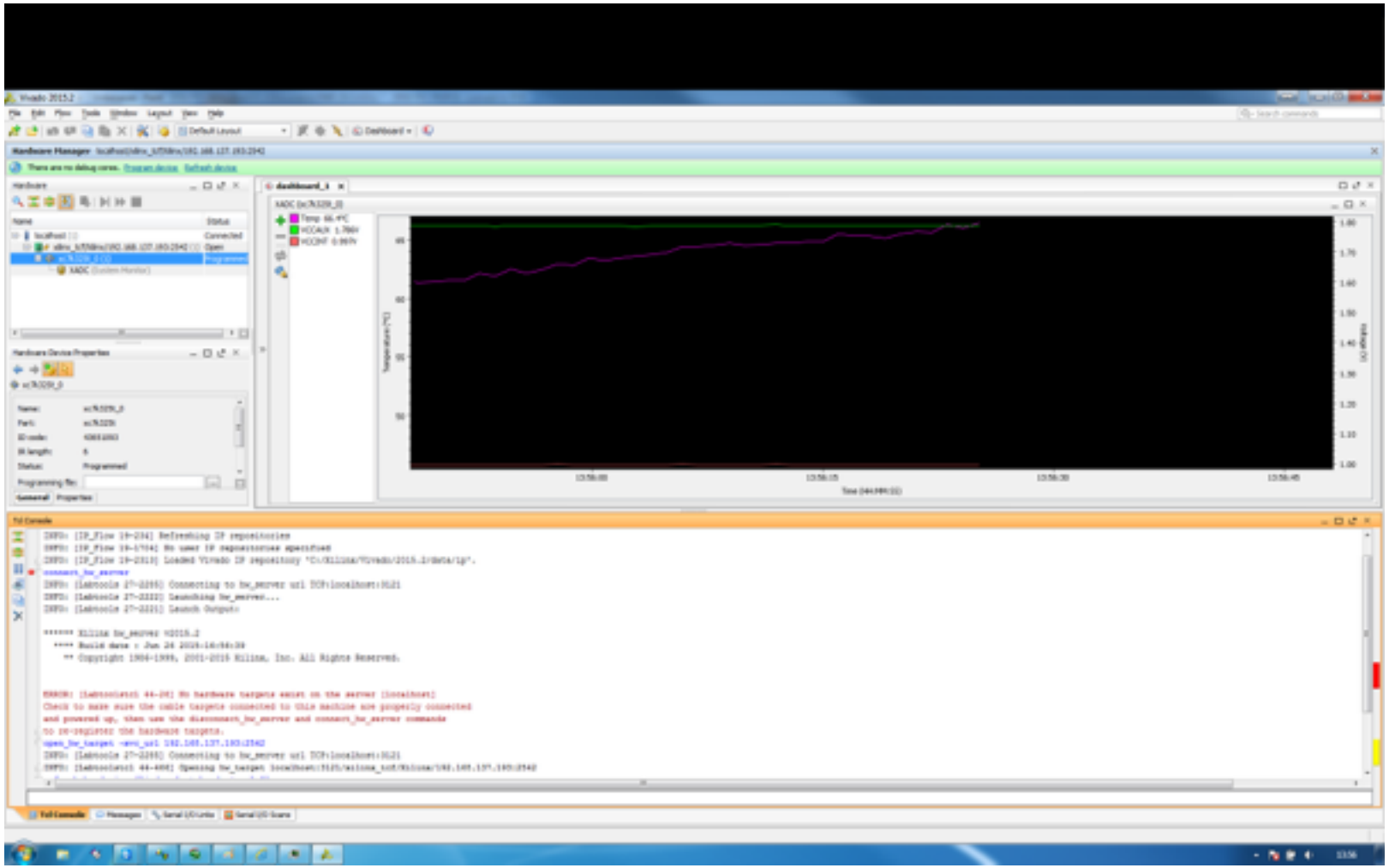

 

# Xilinx-Vivado Tool
## Running development



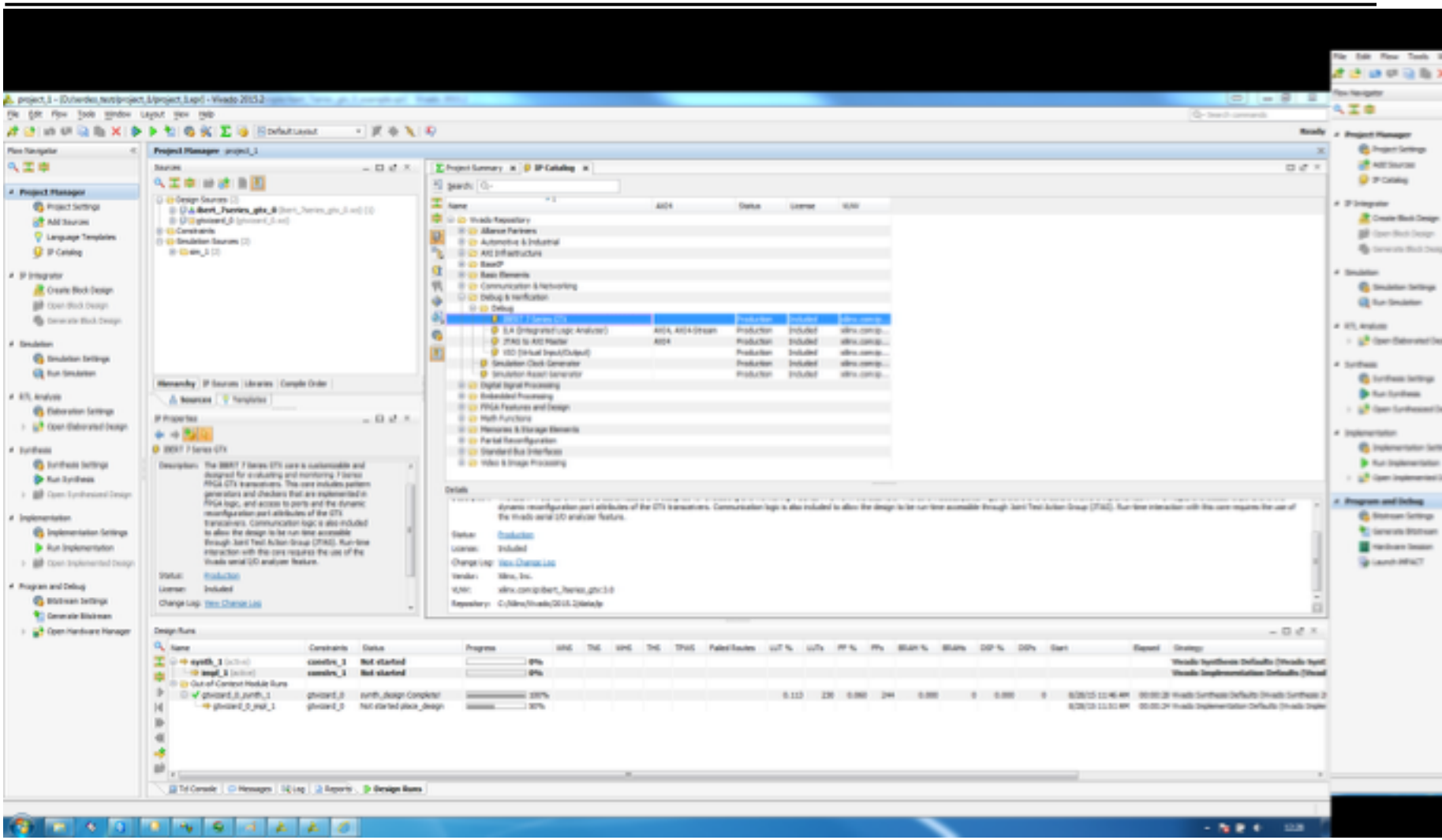

 

# Xilinx Vivado Software
## Hardware-Monitor (live Temp and Voltages)



# Tutorial IBERT Tool Live via
## JTAG Tuning & Analysis of SerDes, Eye-Opening



# NAT-JSM Backplane Connector
## Adaptable Pin Configuration (FPGA)

| Pin # | JSM-Signal | JSM-Signal | Pin # |
|---|---|---|---|
| 1 | GND | GND | 170 |
| 2 | PP_MCH1 | STCK1 | 169 |
| 3 | IO_1 (PS1#) (*) | STMS1 | 168 |
| 4 | 3.3V (MP) | STDI1 | 167 |
| 5 | GA0 | STDO1 | 166 |
| 6 | IO_2 (ETH) (*) | STRST#1 | 165 |
| 7 | GND | GND | 164 |
| 8 | IO_3 (ETH) (*) | STCK2 | 163 |
| 9 | PP_MCH1 | STMS2 | 162 |
| 10 | GND | GND | 161 |
| 11 | TCK1 | STDI2 | 160 |
| 12 | TMS1 | STDO2 | 159 |
| 13 | GND | GND | 158 |
| 14 | TDI1 | STRST#2 | 157 |
| 15 | TDO1 | STCK3 | 156 |
| 16 | GND | GND | 155 |
| 17 | GA1 | STMS3 | 154 |
| 18 | NC (PWR) | STDI3 | 153 |
| 19 | GND | GND | 152 |
| 20 | TRST#1 | STDO3 | 151 |
| 21 | TMREQ#1 | STRST#3 | 150 |
| 22 | GND | GND | 149 |
| 23 | TCK2 | STCK4 | 148 |
| 24 | TMS2 | STMS4 | 147 |
| 25 | GND | GND | 146 |
| 26 | GA2 | STDI4 | 145 |
| 27 | PWR_SMP | STDO4 | 144 |
| 28 | GND | GND | 143 |
| 29 | TDI2 | STRST#4 | 142 |
| 30 | TDO2 | STCK5 | 141 |
| 31 | GND | GND | 140 |
| 32 | TRST#2 | STMS5 | 139 |

# NAT-JSM compatible with most
## of todays MTCA chassis providing a JSM slot

- Automatic arbitration between JTAG Masters
  - JTAG download from MCH via WEB Interface
  - JTAG programming connector at front panel
  - JTAG to USB interface at front panel
- Target selection through JTAG information
- Overrule of automatic operation and dedicated selection of JTAG target by front panel elements
- Multiple JSM Pinout configurations via FPGA
  - output drivers are turned on if JSM slot is detected
- Power supply through MCH power channels or power module SMP power
- Minimal power consumption

# Thank you very much!
## Questions?

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