struck innovative systeme

The SIS8800 Multi Purpose MTCA.4 Scaler AMC and the SIS8980 Discriminator RTM

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Counter/Scaler Application Examples

Voltage to Frequency Converter V/F readout of ion chamber
(classical Synchrotron Radiation beamline approach)

Pulse Counting from detectors after discriminator
- Beam Loss Monitors
- Astro-/Particle Physics

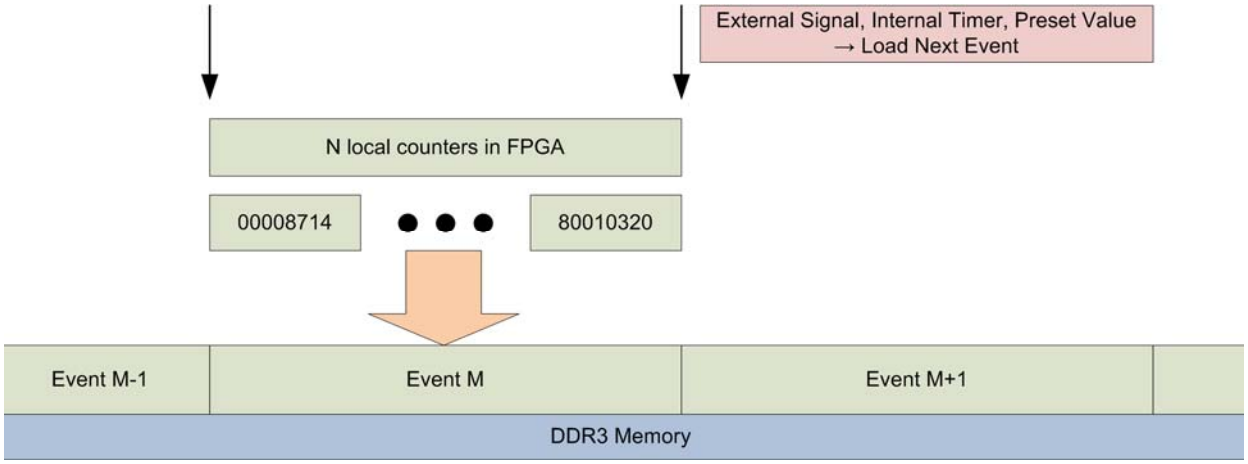
Counting of (angular) encoder ticks (w. 12 o´ clock reset)
- rotating crystal method in Synchrotron Radiation
- chopper wheel position in Neutron Scattering
- machine position in industrial applications

Deadtime/trigger type/event counters in digitizer firmware

Multi Purpose Scaler
What Scaler Modes/Flavors are out there?

- Scaler/Counter
- Latching Scaler
- Preset Scaler
- Multi Channel Scaler/Multiscaler (MCS)
  Dwell time defines time resolution
  Memory required
  MTCA.4 bandwidth → shorter sustained dwell times
- Histogramming Scaler
  Repetitive measurement (e.g laser activation of sample)
  read-modify-write cycles → FPGA block RAM prefetch
  like MCS

Multi Channel Scaling (MCS)



Dwell time: time between of two Events (LNE signals)

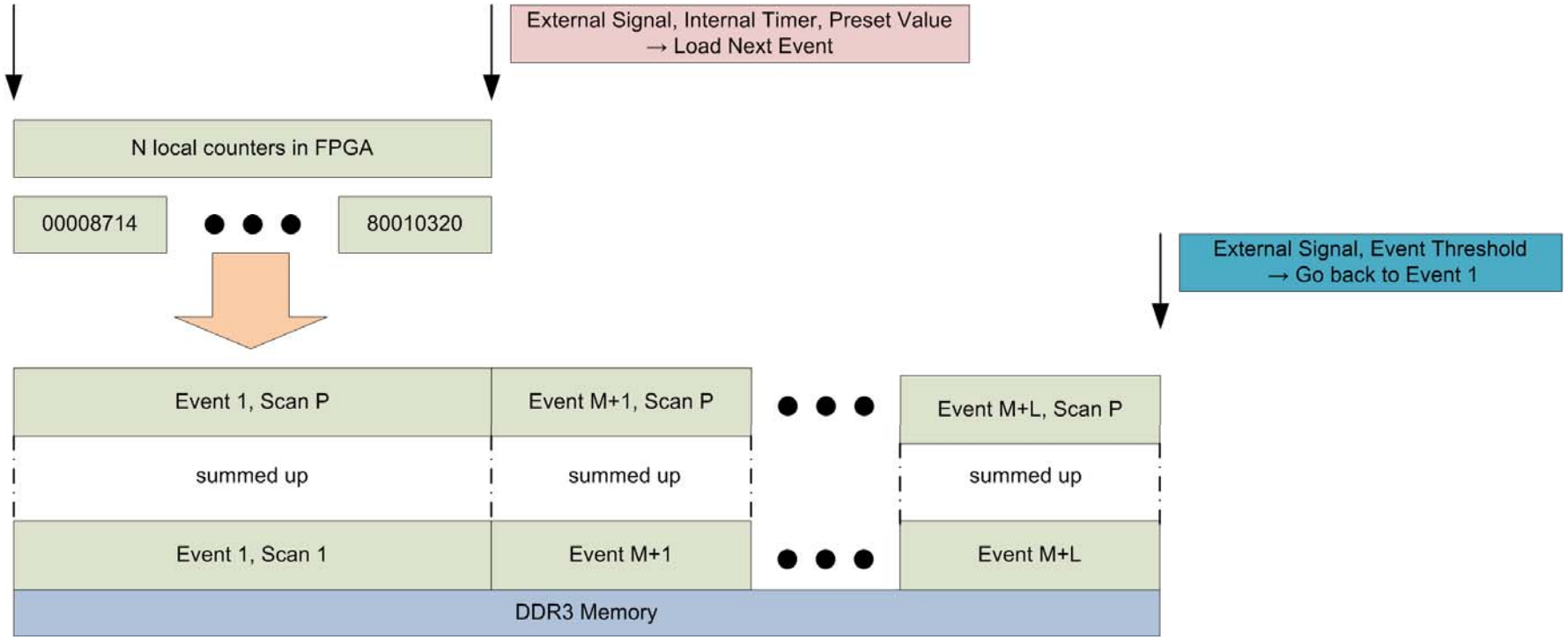
minimum dwell time defines resolution in time

limited by memory (short term) and readout speed (long term)

short dwell times → 16-bit or 8-bit counter depth sufficient

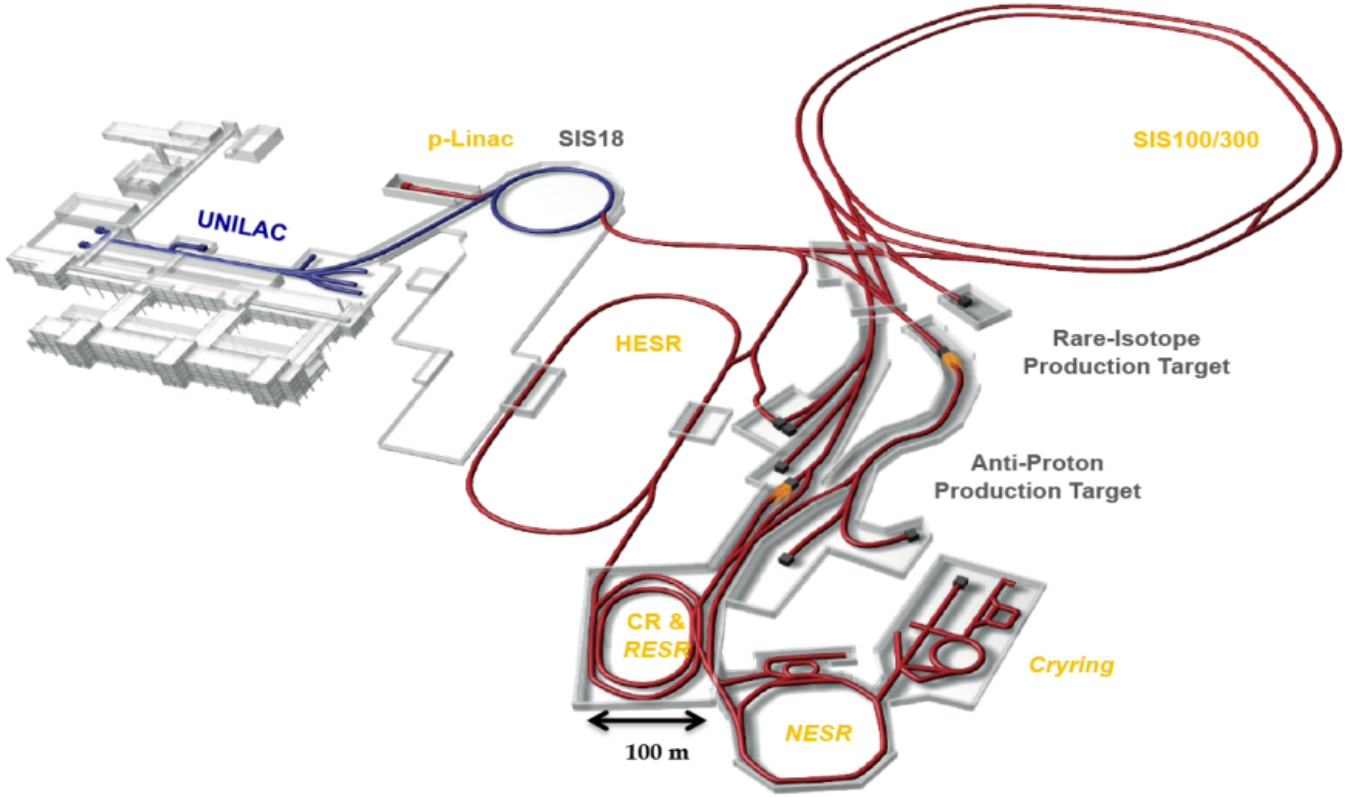
32 channels x 8-bit x 125 MHz (8 ns dwell time) → 4000 MByte/s

Histogramming Scaling



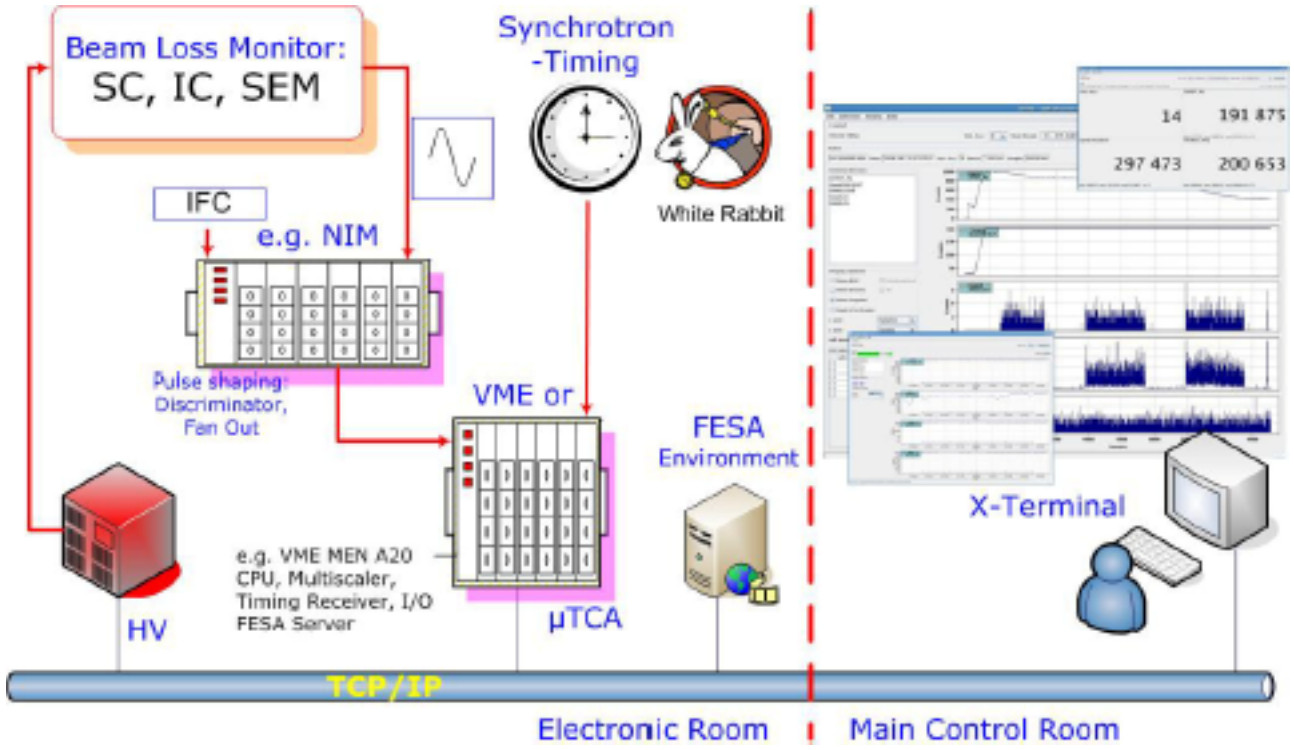
FAIR

Facility for Antiproton and Ion Research



1,3 GEUR → One of the larger accelerator projects in the world
Modularized Start Version with 2022 timeframe and full operation in 2025

GSI FAIR
Large Analogue Signal and Scaling Information Environment (LASSIE)

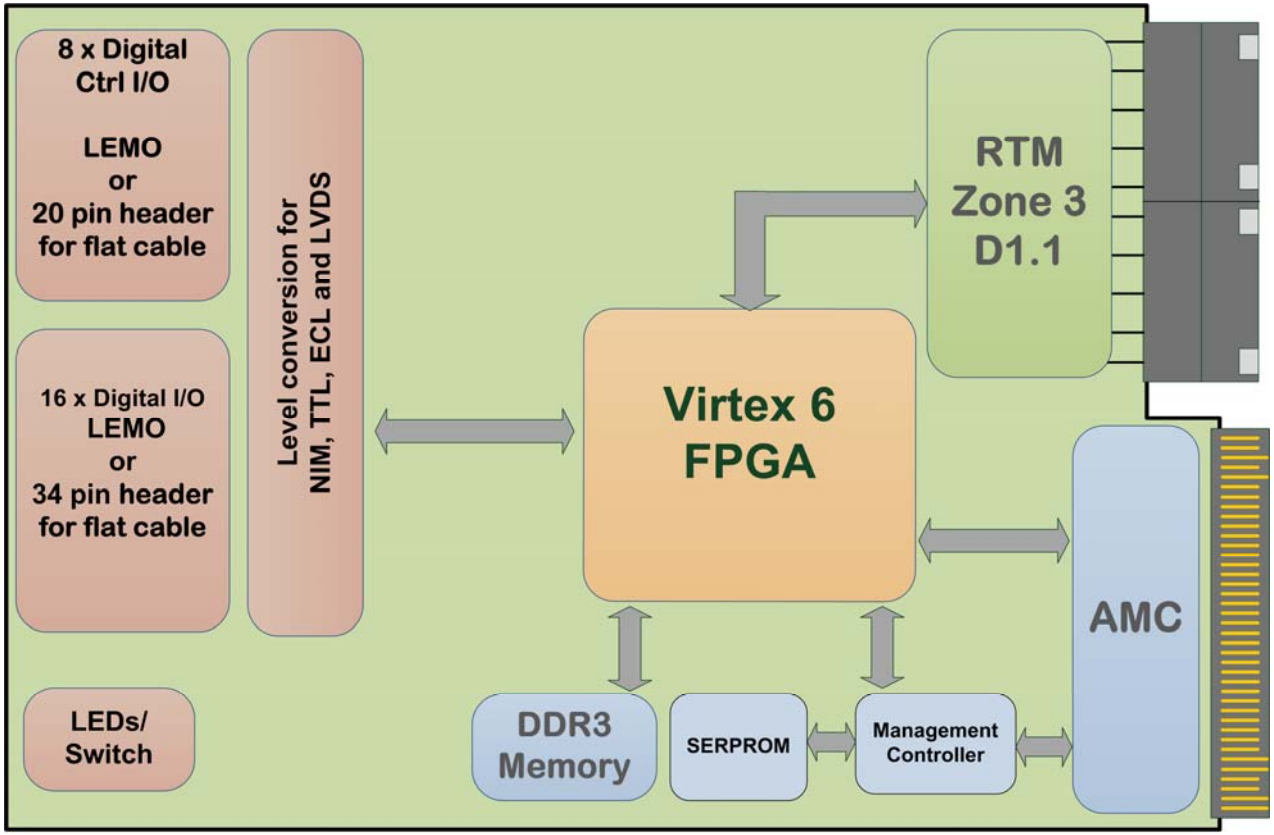


SIS8800 Multi Purpose Scaler

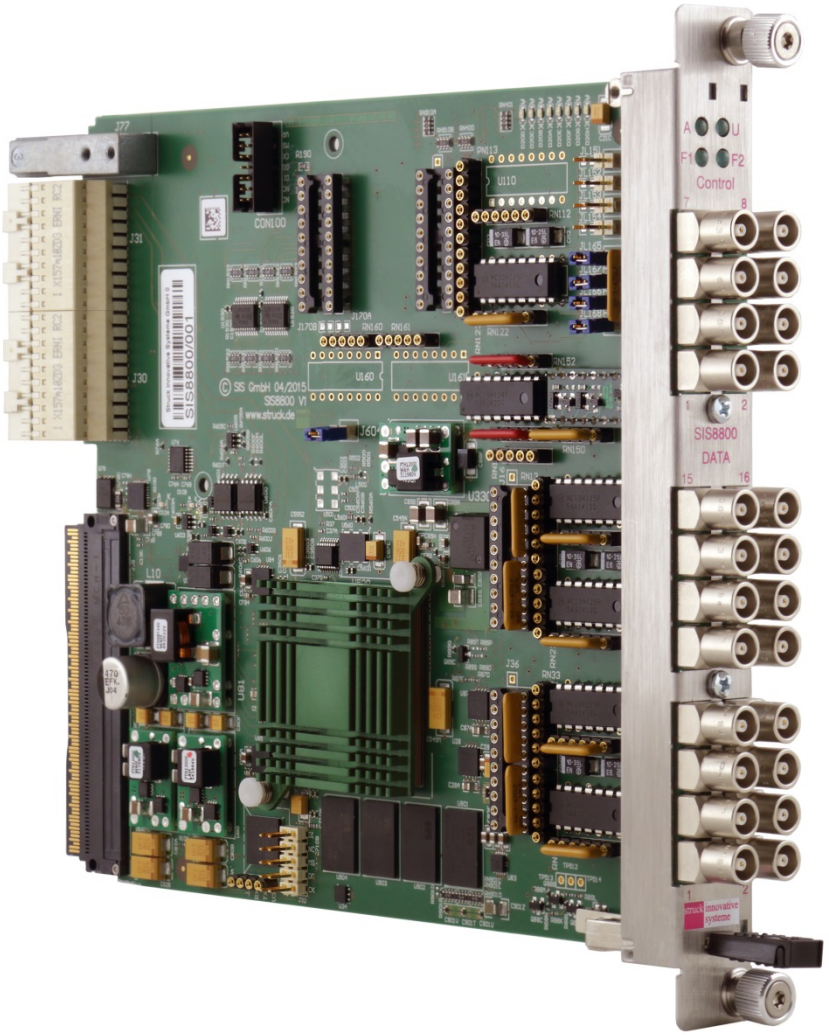
Functionality

- MTCA.4 AMC
- 4 Lane PCI Express connectivity
- XC6VLX130T-2FFG1156C Xilinx
- Dual boot
- Redundant PCIe implementation
- 2 GByte DDR3 memory
- 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
- 250 MHz count rate (NIM/ECL)
- 4 control in-/4 control front outputs
- Zone 3 Class D1.1 compatible
- MMC 1.0 under DESY license LV91

SIS8800 Block Diagram



SIS8800 in NIM/LEMO Configuration



Why does the input part of the SIS8800 look so olf-fashioned?

a.) accomodate LEMO and Pin header inputs

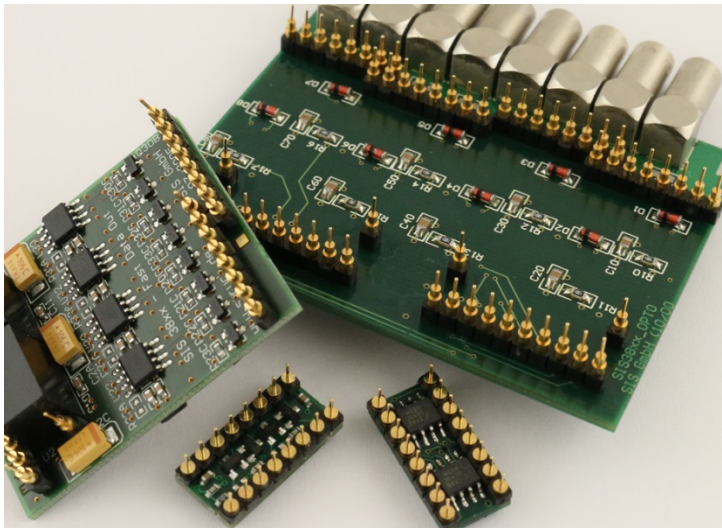
b.) reuse 15 years worth of legacy level adapter boards and DIL components (MC10H12x, 74ALS640,…)

LEMO

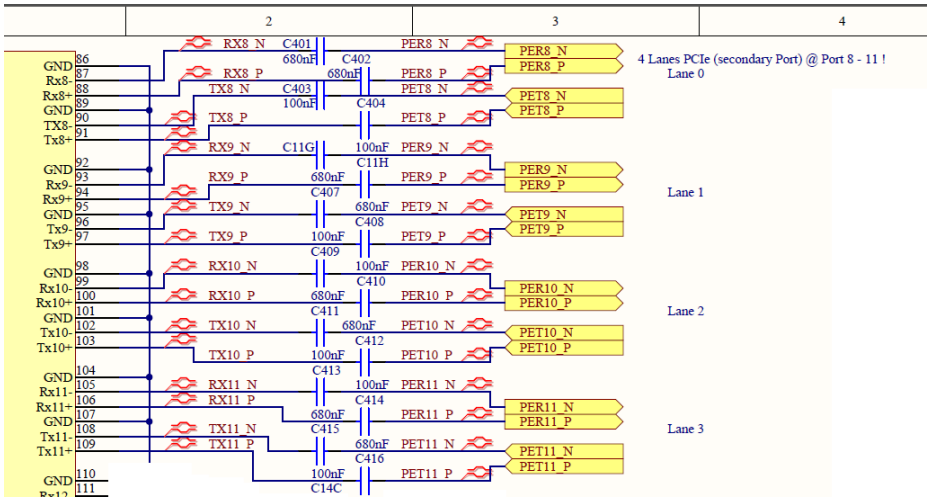
NIM,TTL 50Ω, TTL high impedance, RS485 Opto

Flat Cable

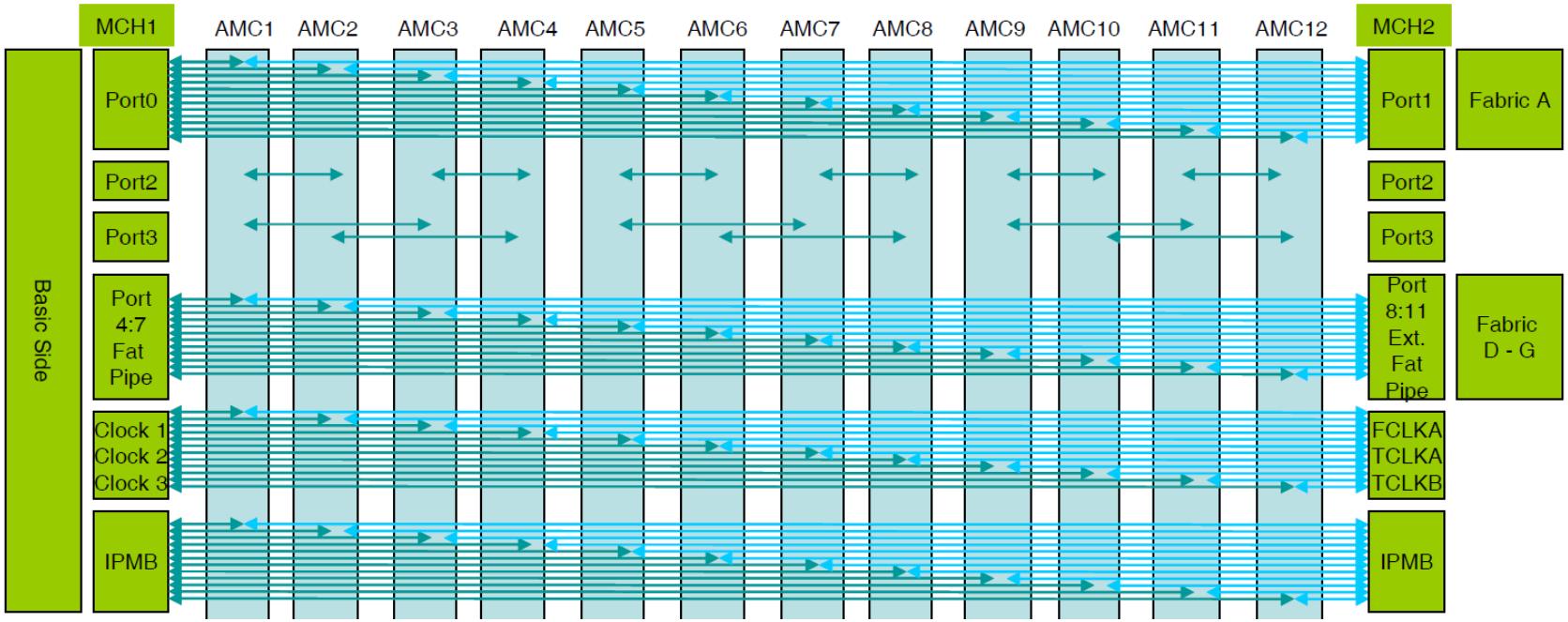
ECL, LVDS, TTL high impedance



SIS8800
First Redundant
PCIe Testbed



use of 8 MGT‘s



Source: ELMA **xTCA-12 Operating Manual**

AMC Connector Excursion
(first time use of Yamaichi on SIS8800)

1.) Card egde

2.) ITB (former Harting) 16211701303000

3.) Yamaichi CN084-170-1000-1000-0

Solution 1.) hardest on backplane and no repair option.

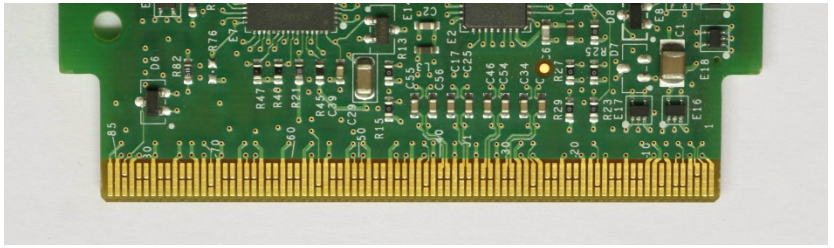
ITB and Yamaichi comparable in price. Replacement of ITB is labor intensive (3 man hours). Installation of Yamaichi requires tooling (2000 € ballpark), replacement is a no brainer.

→ SIS8800 first Struck card with Yamaichi (substantial impact on layout)

AMC Connector Options

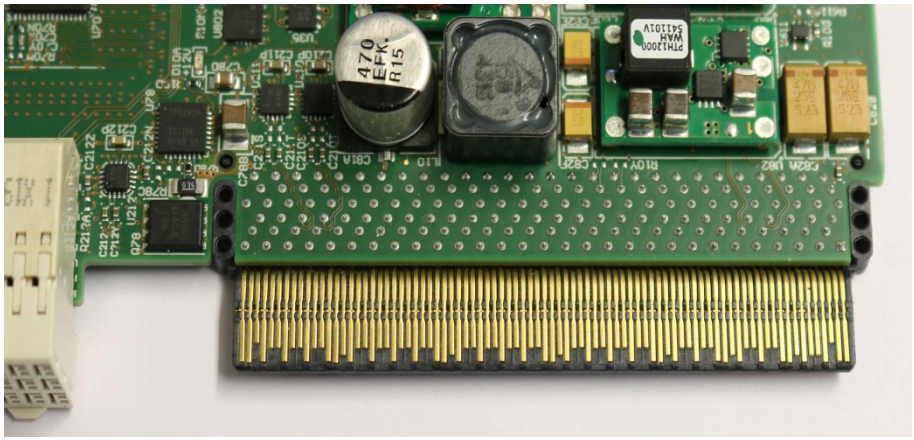
Card Edge/PCB Solution

- lowest board real estate
- hardest on backplane
- no repair



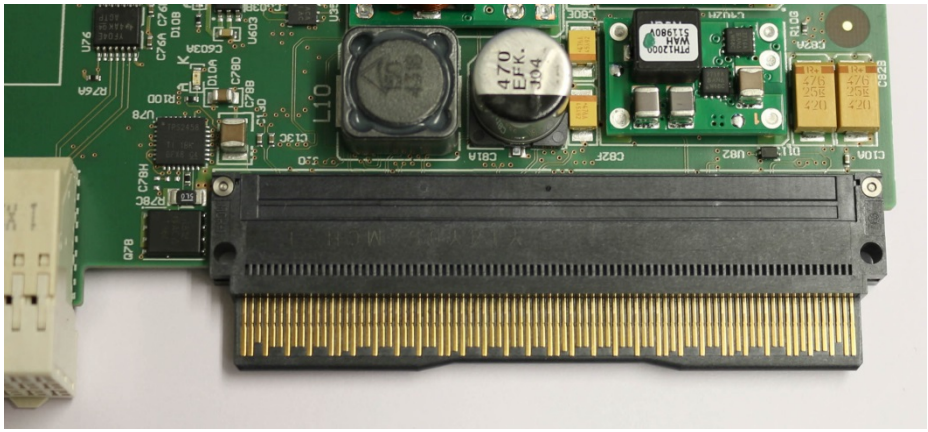
ITB (Harting) Solution

- tedious repair



Yamaichi Solution

- solderless repair



Firmware

64-bit wide DDR3 memory interface

256 Bit/4ns write

Readout in parallel to acquisition

→ Minimum dwell time 8 ns

32 channels x 8-bit wide

Standard counter depth 32-bit

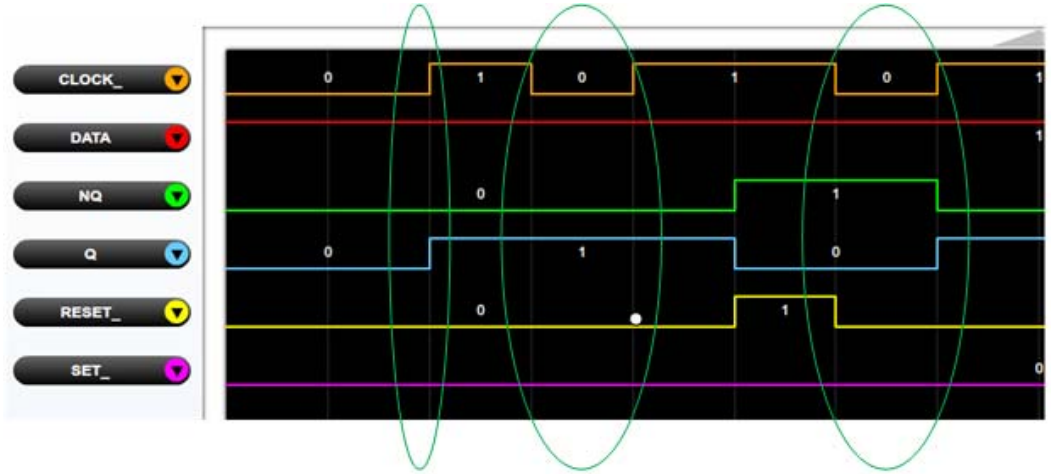
SIS8800 Zone 3 Resources (Digital Class D1.1 Compatible)

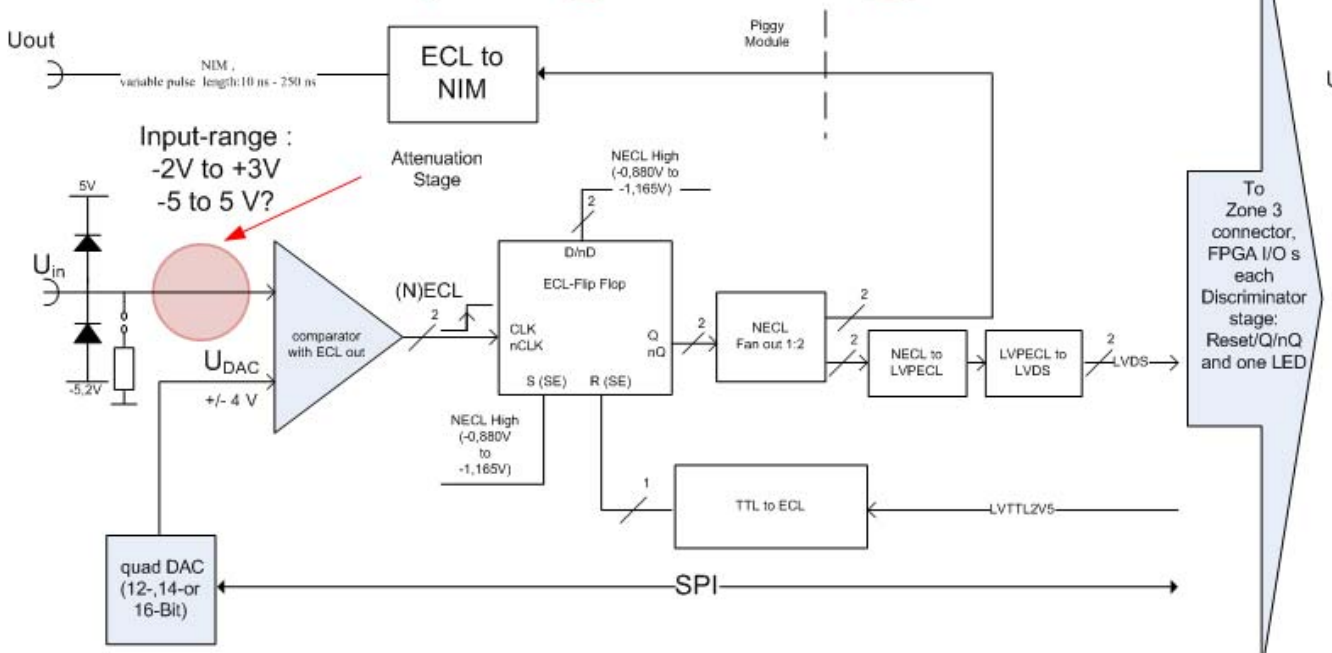
- 2 MGTs
- 42 LDVS I/Os
- 3 fixed LVDS Out
- JTAG
- I2C
- RTM LVDS CLK In

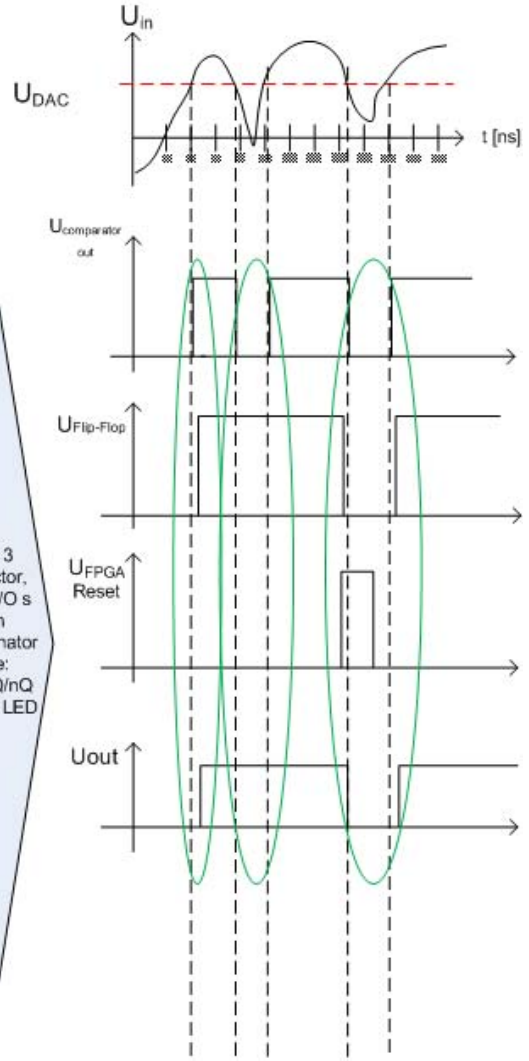
SIS8980 Leading Edge Discriminator

- MTCA.4 RTM
- 16 Discriminator Inputs
- 16 Digital NIM Outputs to FP
- Commercial comparator chip with ECL out
- Input range to be finalized (user input welcome)
- 12, 14 or 16-bit Threshold DACs
- MMCX connectors
- FP Activity LED for channel above threshold
- Input protection
- Zone 3 class D1.1 compatible
- DESY MMC 1.0 w/o microcontroller

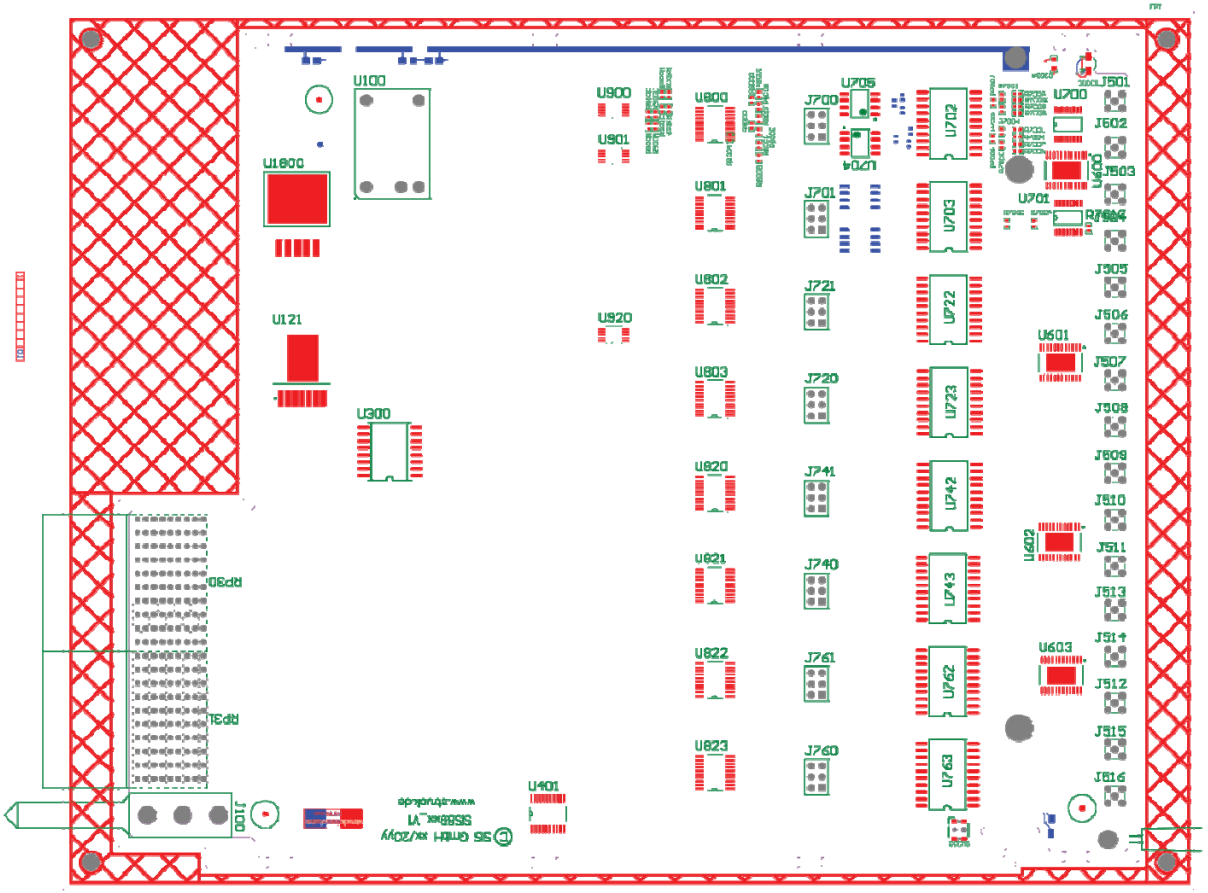
SIS8980 Design





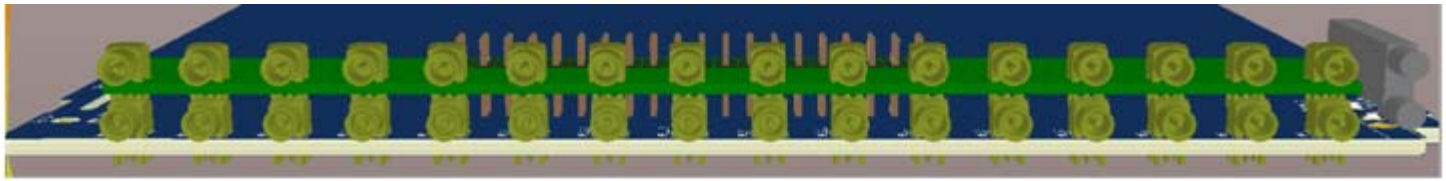


SIS8980 Single channel and coarse placement

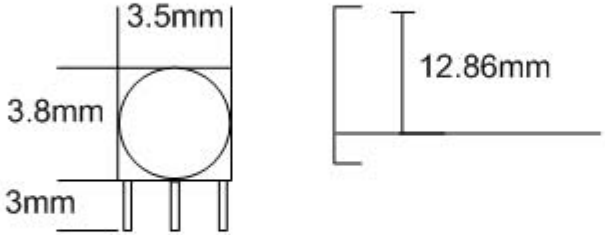


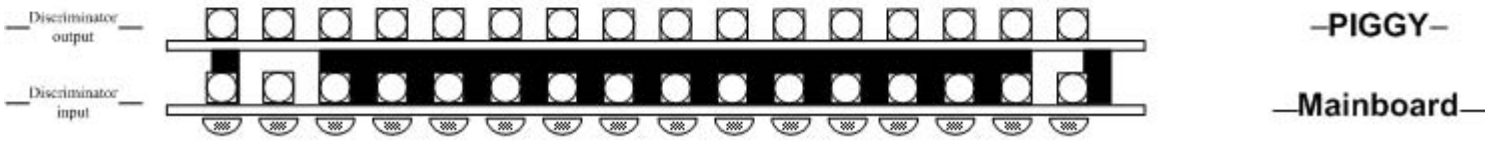
Output connectors on piggy card

SIS8980 Front Panel Arrangement



Mid-size Module





32 MMCX

Possible Future RTMs for SIS8800

- LEMO/Pin header based digital I/O
  → 32 to 48 LEMO channels per AMC slot
  → 576 channels in a single crate
- higher density digital I/O → covered by existing other designs
- Synchrotron Beamline Infrastructure like Monochromator Stabilizer (moderate demand), Encoder Interface,…
- Optical Link Interface to non V/F Beamline Frontends

MTCA.4 Relevance I

As of Dec. 2015 Struck users have in field

> 870 MTCA.4 AMCs

> 670 MTCA.4 RTMs

MTCA.4 Relevance II
current Struck user base

CN	IHEP Beijing, SINAP
CZ	ELI (Inst of Physics, Praha)
DE	DESY, HZDR, PTB, MPG, KIT, HZB, GSI, DESY Zeuthen
FR	ITER
IN	TIFR
JP	KEK, SPring8
KR	PAL
SE	ESS, Lund University
US	SLAC, NSCL/FRIB, ANL

expected to join shortly: TR TARLA

Demonstration at Struck „Booth“

- MTCA.4 Desktop System

with

- SIS8800 Scaler
- SIS8300-L2 100 MSPS 16-bit Digitizer with SIS8900 RTM

Questions/Discussion

GL ISO 9001

GL Systems Certification